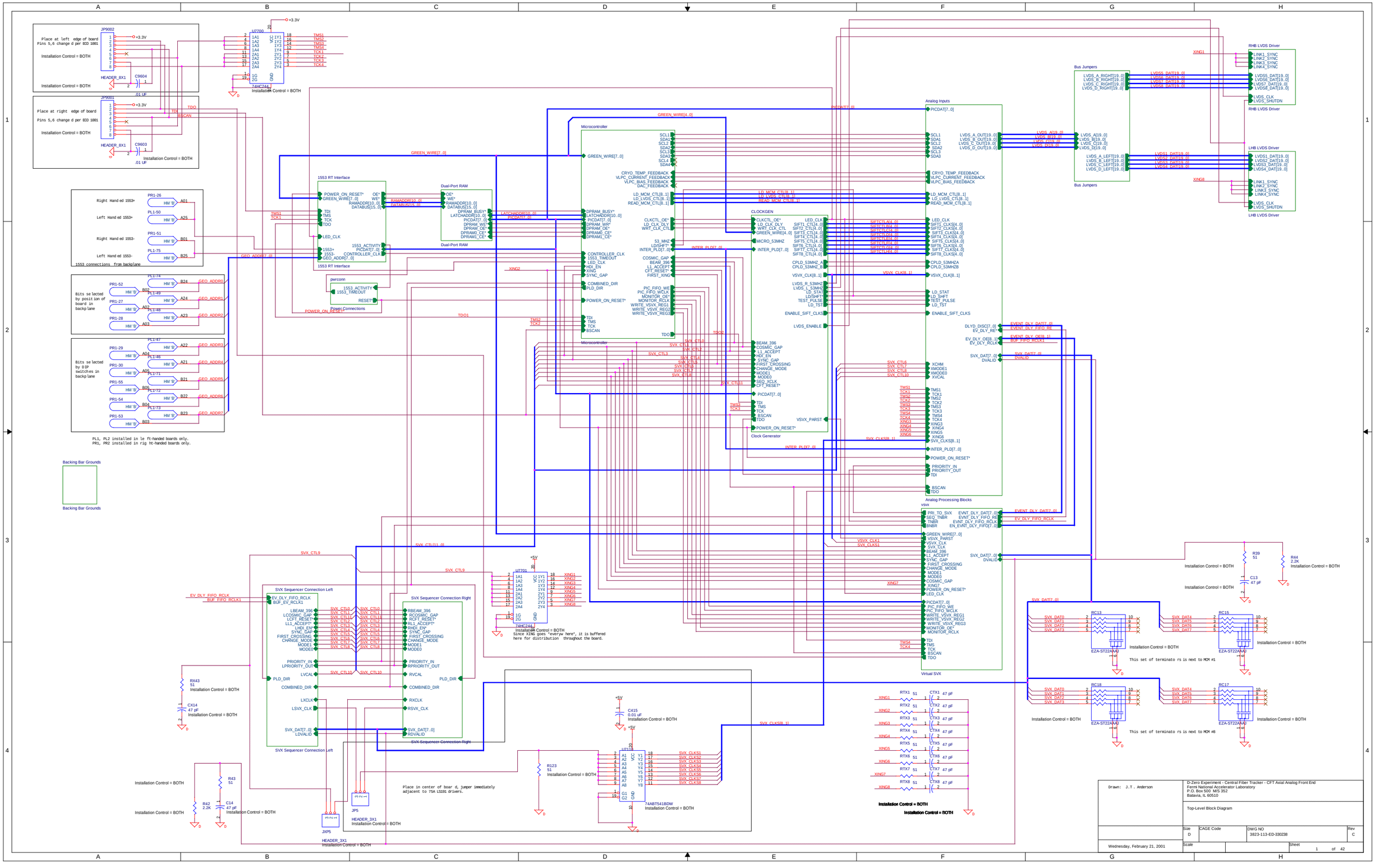
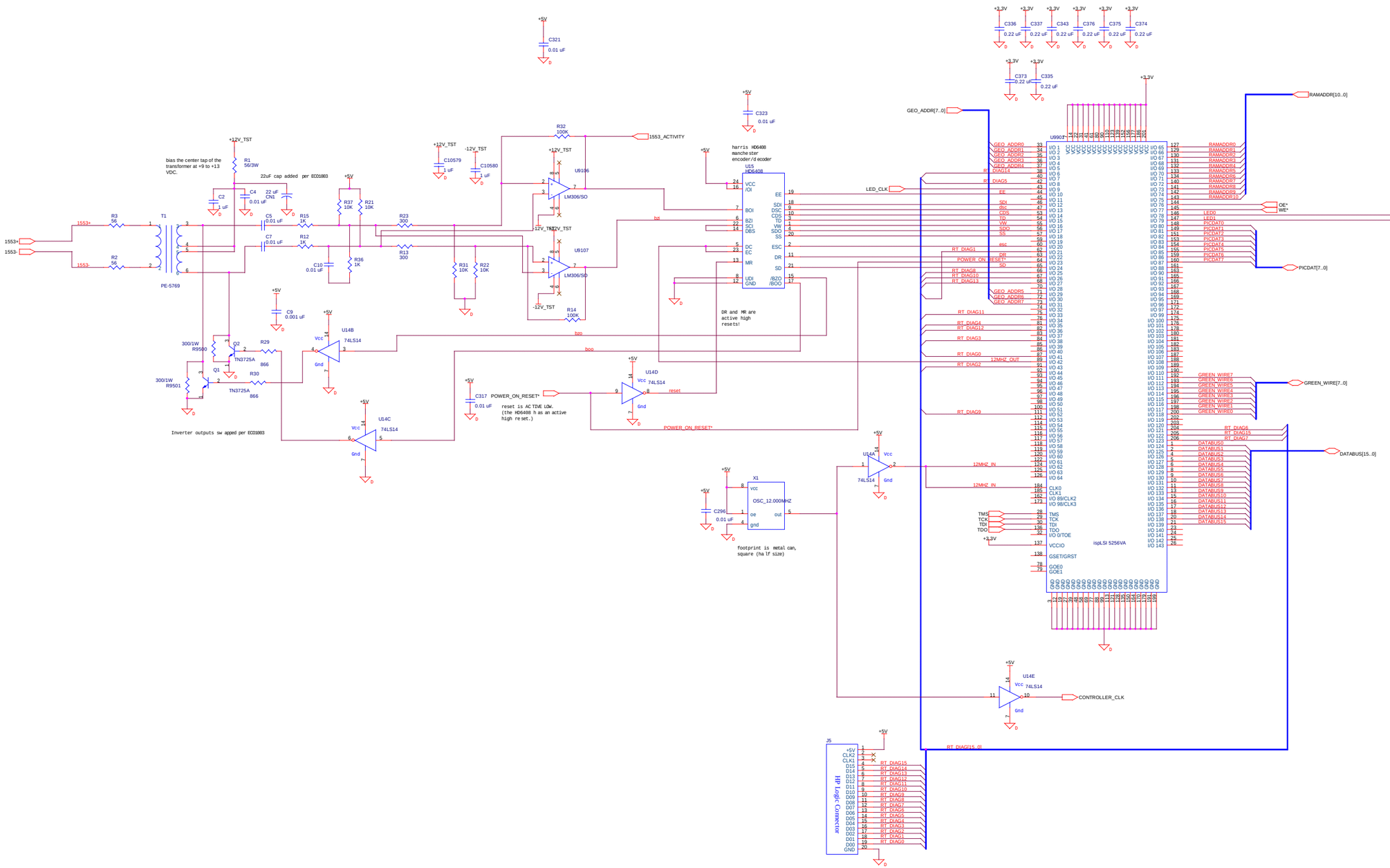

JP9002
Place at left edge of board
Pins 5,6 change d per ECO 1001
Installation Control = BOTH
HEADER_8X1
C9604
.01 UF
JP9001
Place at right edge of board
Pins 5,6 change d per ECO 1001
C9603
U7700
74HC244
U7701
U7118
74ABT541BDW
1553 RT Interface
Dual-Port RAM
Microcontroller
CLOCKGEN
Clock Generator
Analog Inputs
Analog Processing Blocks
Virtual SVX
Bus Jumpers
RHB LVDS Driver
LHB LVDS Driver
SVX Sequencer Connection Left
SVX Sequencer Connection Right
Right Hand ed 1553+
Left Hand ed 1553+
Right Hand ed 1553-
Left Hand ed 1553-
1553 connections from backplane
Bits se lected by position of board in backp lane
Bits se lected by DIP switches in backp lane
PL1, PL2 installed in le ft-handed boards only.
PR1, PR2 installed in rig ht-handed boards only.
Backing Bar Grounds
Since XING goes "everyw here", it is buffered here for distribution throughout the board.
Place in center of boar d, jumper immediately adjacent to 75A LS191 drivers.
Installation Control = BOTH
This set of terminato rs is next to MCM #1
This set of terminato rs is next to MCM #8
Drawn: J.T. Anderson
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 MS 352
Batavia, IL 60510
Top-Level Block Diagram
Size D
CAGE Code
DWG NO 3823-113-ED-330238
Rev C
Wednesday, February 21, 2001
Scale
Sheet 1 of 42

All parts on t his page, if installed, are in stalled in both left-handed and rig ht-handed boards.



D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
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P.O. Box 500 M/S 352
Batavia, IL 60510

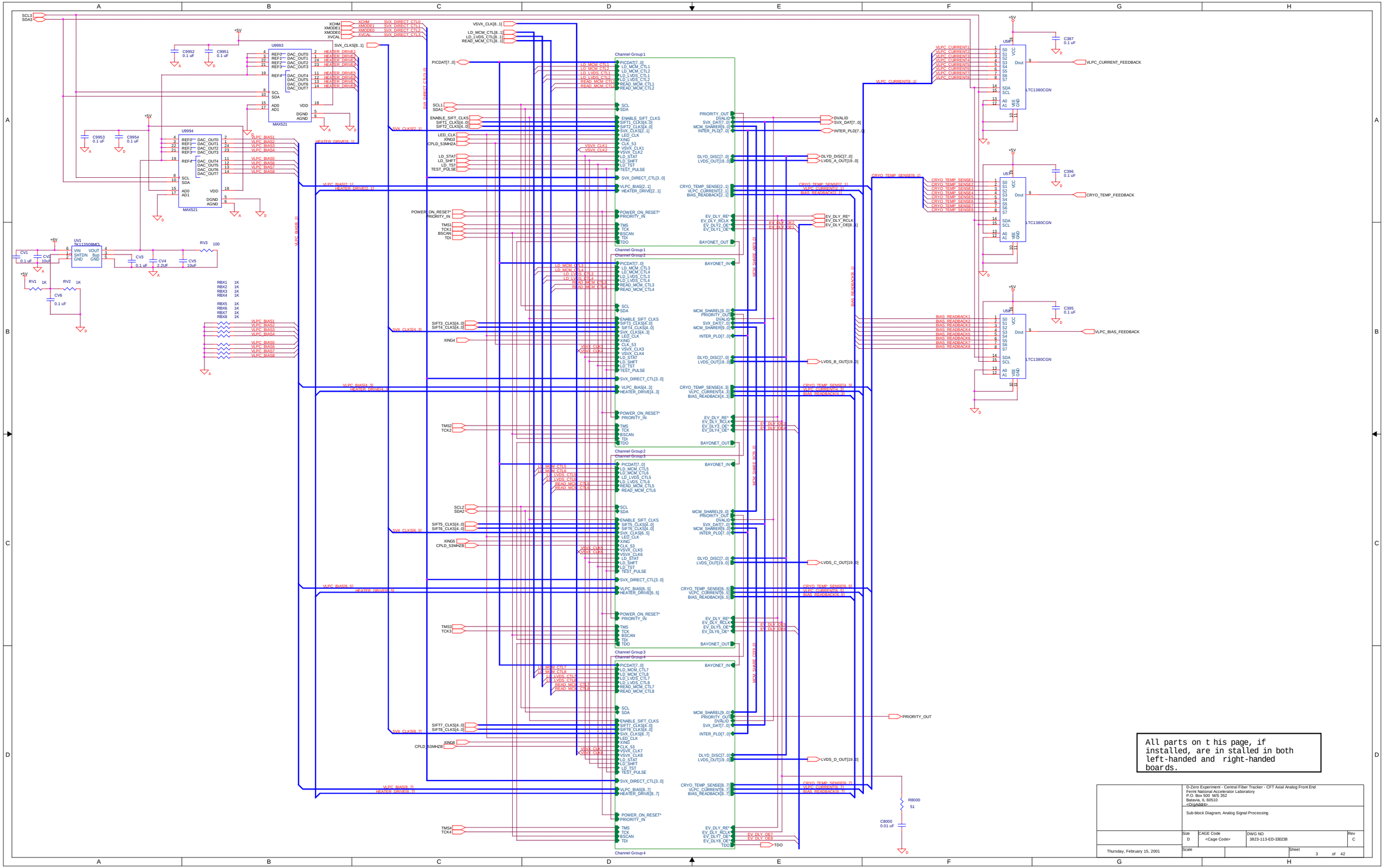
1553 Interface / Remote Terminal

Size	CAGE Code	DWG NO	Rev
D		3823-113-ED-330238	C

Thursday, February 15, 2001

Scale

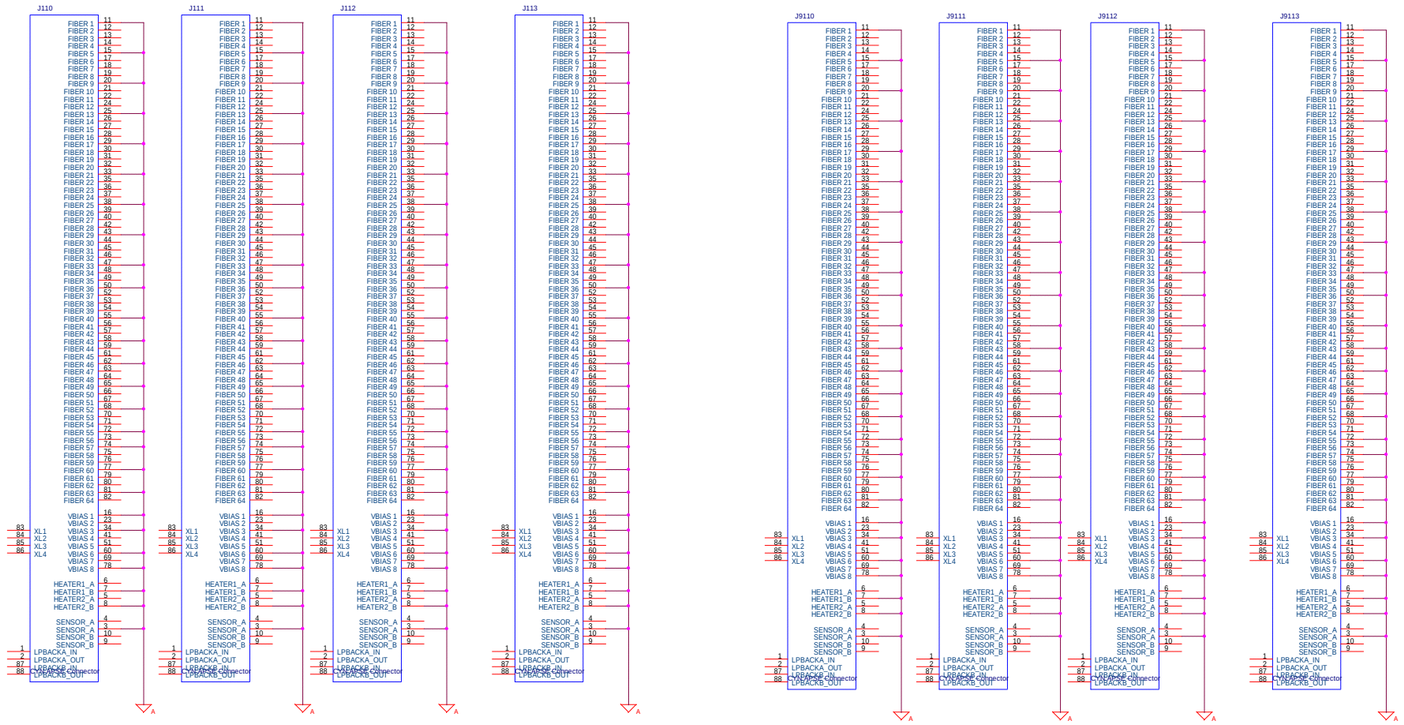
Sheet 2 of 42

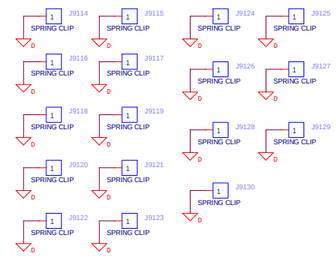


All parts on t his page, if installed, are in stalled in both left-handed and right-handed boar ds.

	D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End Fermi National Accelerator Laboratory P.O. Box 500 M/S 352 Batavia, IL 60510 <OrgAddr4>		
	Sub-block Diagram, Analog Signal Processing		
	Size D	CAGE Code <Cage Code>	DWG NO 3823-113-ED-330238	Rev C
Thursday, February 15, 2001	Scale		Sheet 3 of 42

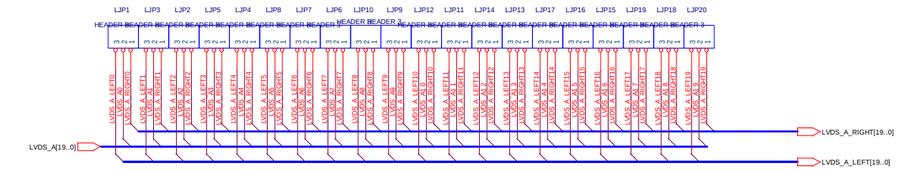
Grounding connections for b acking bar. Tie all pins together using TOP SIDE TRACES ONLY. Connect trace sets to AGND using via s at each end of connector only. Do not put any vias inside connector body or along long edges, so as to minimally obstruct charge signals passin g underneath.

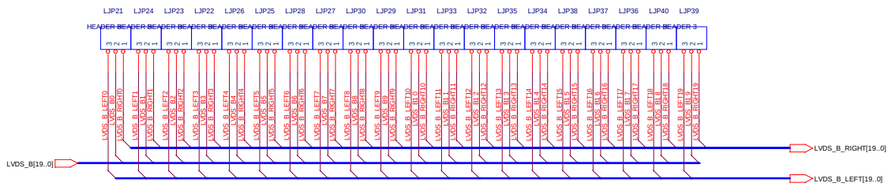


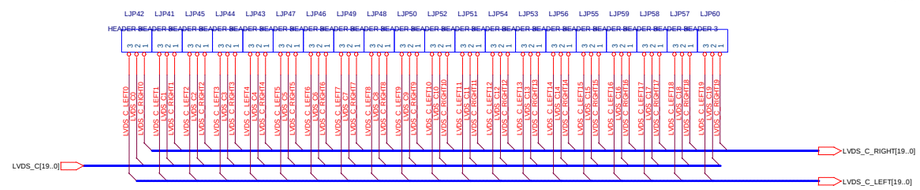


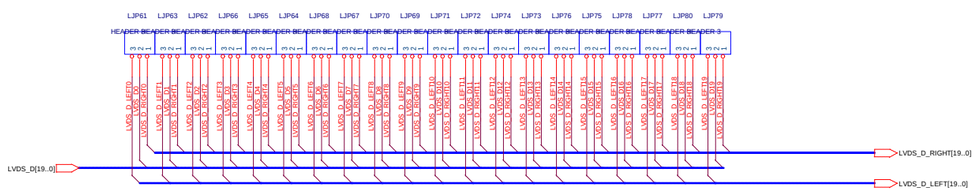
No installable par ts on this page; all components are bare-board copper features only.

	D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End Fermi National Accelerator Laboratory P.O. Box 500 M/S 352 Batavia, IL 60510 <OrgAddr4>
	Grounding patterns for backing bar
	Size D · CAGE Code <Cage Code> · DWG NO 3823-113-ED-330238 · Rev C
Thursday, February 15, 2001	Scale · Sheet 4 of 42

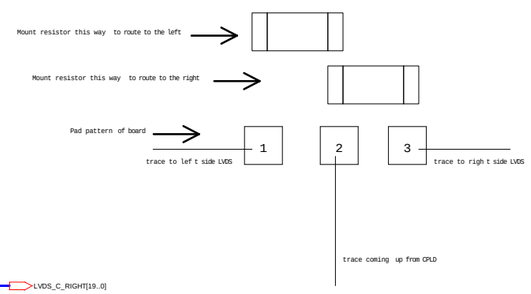








Blowup sketch of how this works



All jumpers are actually 3-pin pad arrays designed to allow installation of a low-resistance 0402 resistor either between pads 1 and 2 or pads 3 and 4, manually routing all eighty bits of the bus to the left-side LDVS drivers or to the right side LVDS drivers. This break removes the long stubs to the unused side allowing the unused side to be unstuffed and eliminating reflection possibilities.

Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board

All parts on this page installed in both left-handed and right-handed boards. POSITIO N OF COMPONENTS VARIES WITH BOAR D HANDEDNESS.

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<OrgAddr4>

Left/Right bus direction selectors

Size	CAGE Code	DWG NO	Rev
D	<Cage Code>	3823-113-ED-330238	C

Thursday, February 15, 2001

Scale

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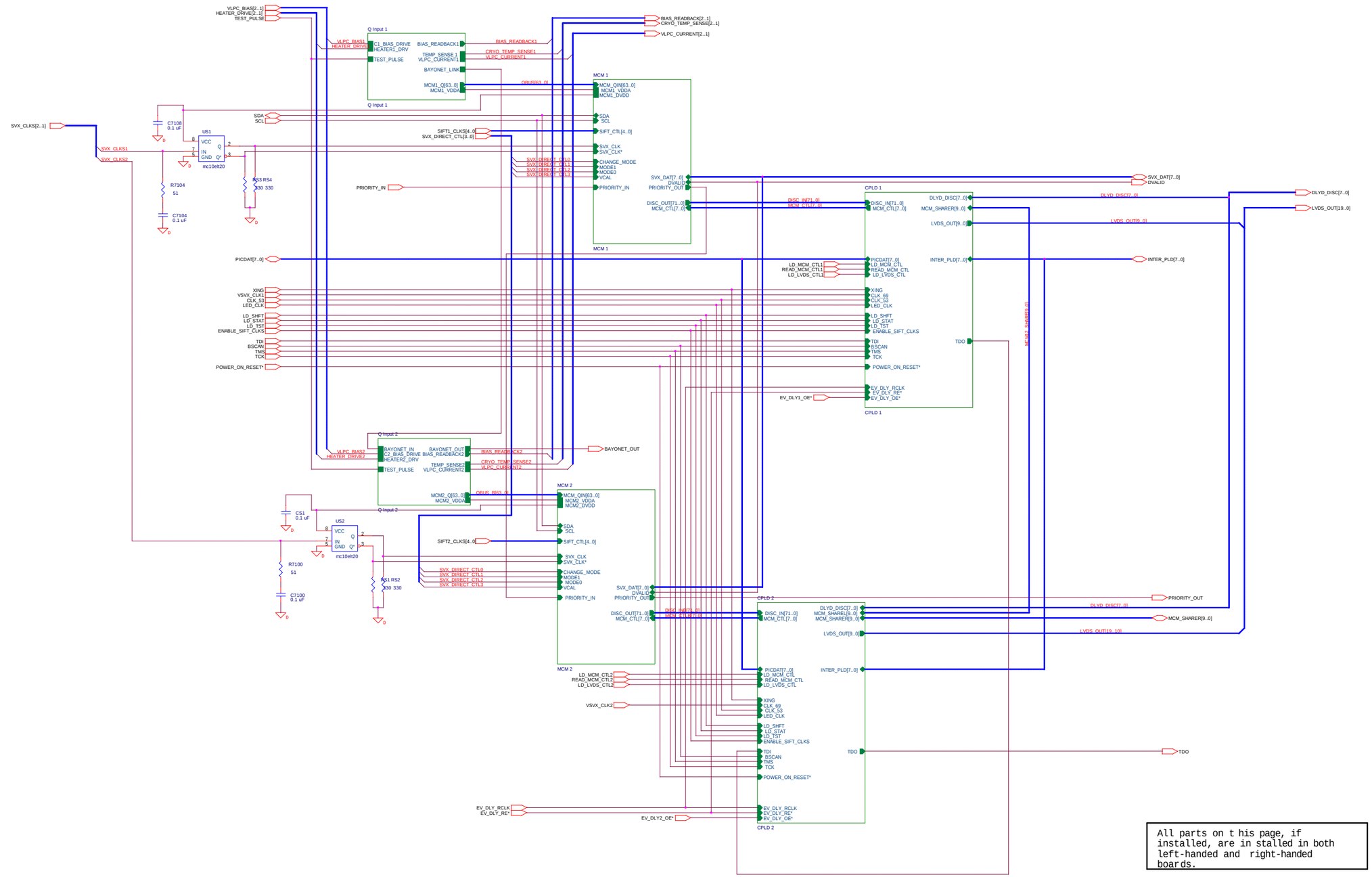


All parts on t his page, if installed, are in stalled in both left-handed and right-handed boards.

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
<OrgAdd4>

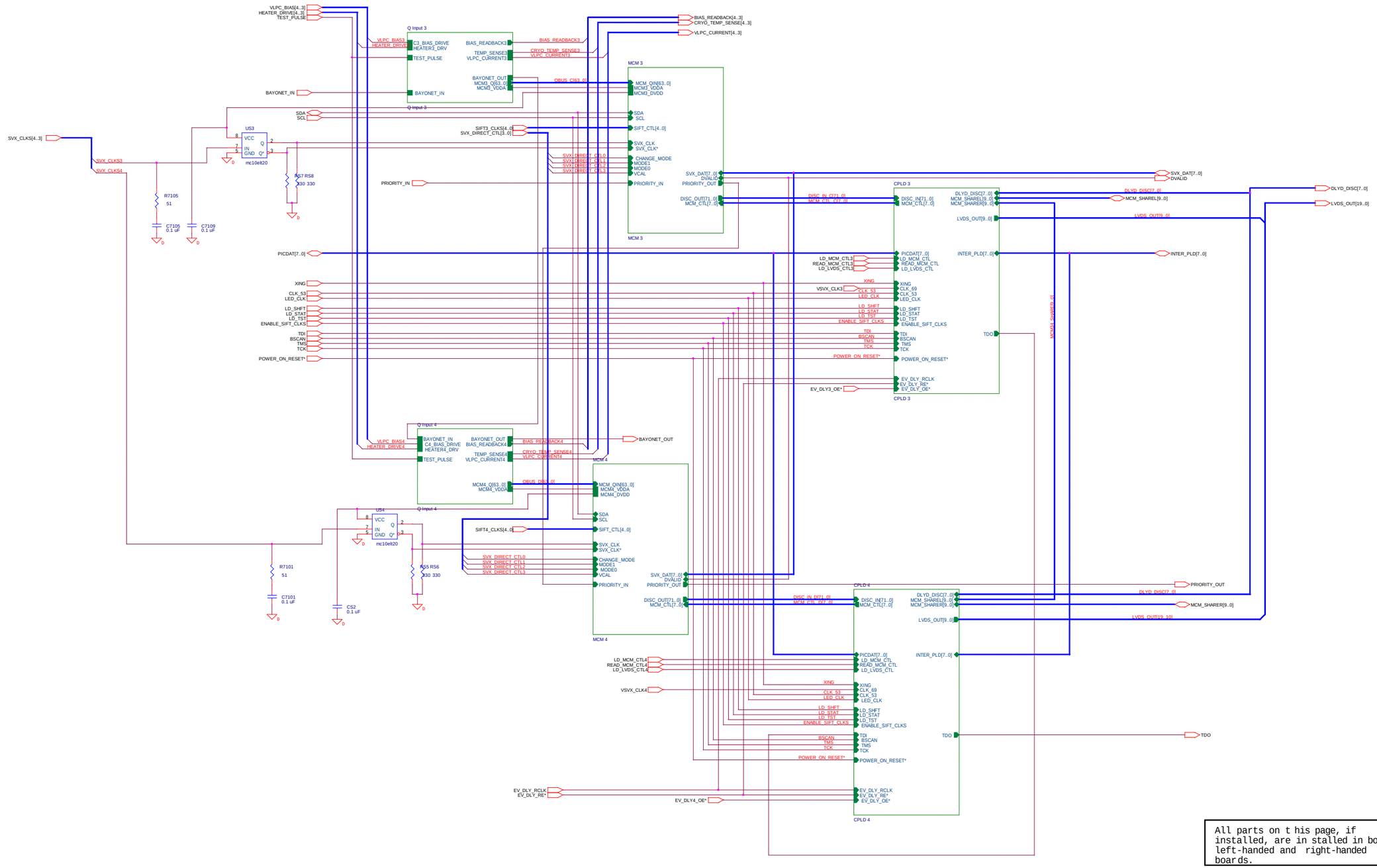
Sub-block Diagram, Qin,MCM,CPLD, #1, #2

Size	CAGE Code	DWG NO	Rev
D	<Cage Code>	3823-113-ED-330238	C

Thursday, February 15, 2001

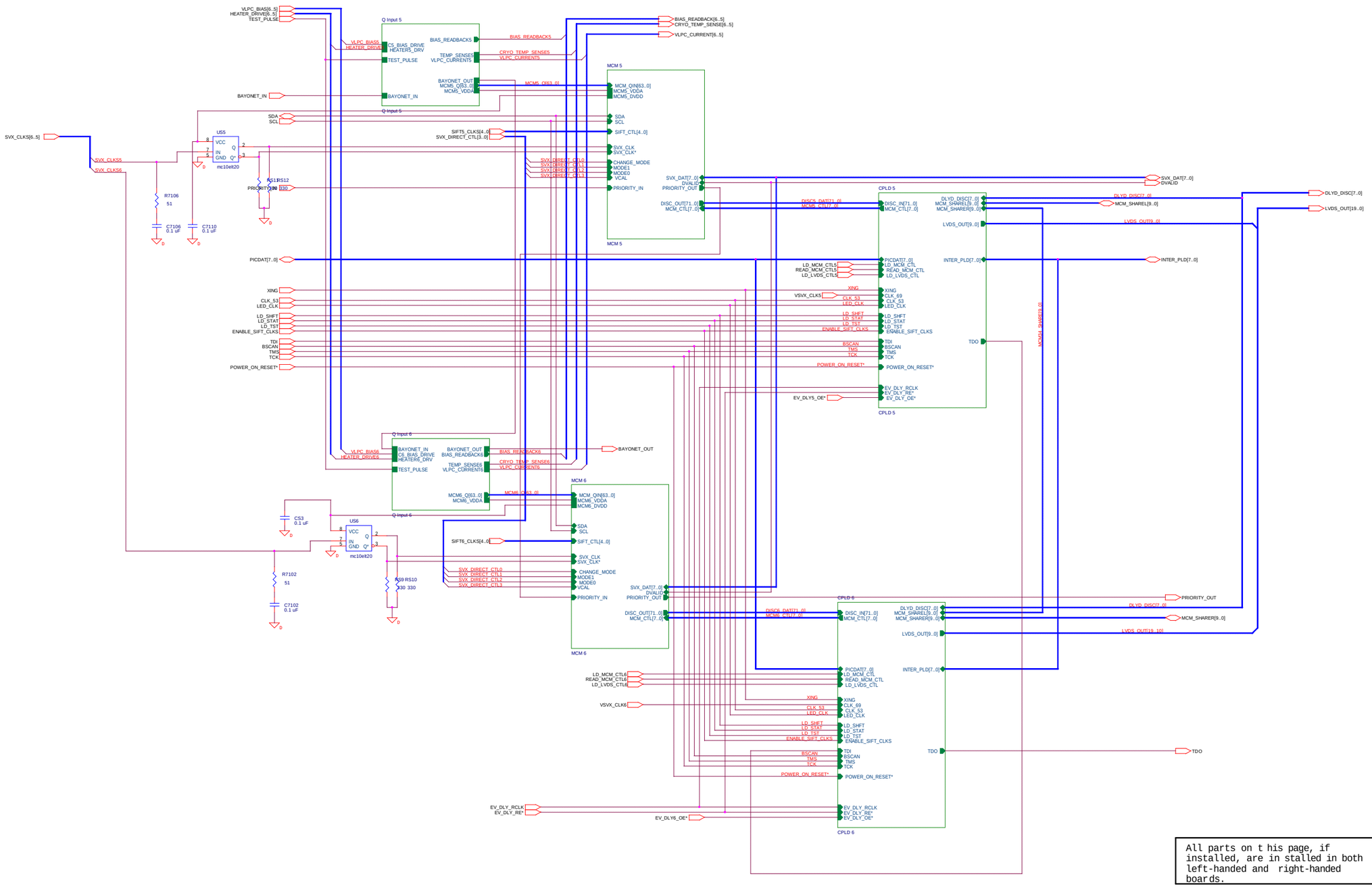
Scale

Sheet 6 of 42



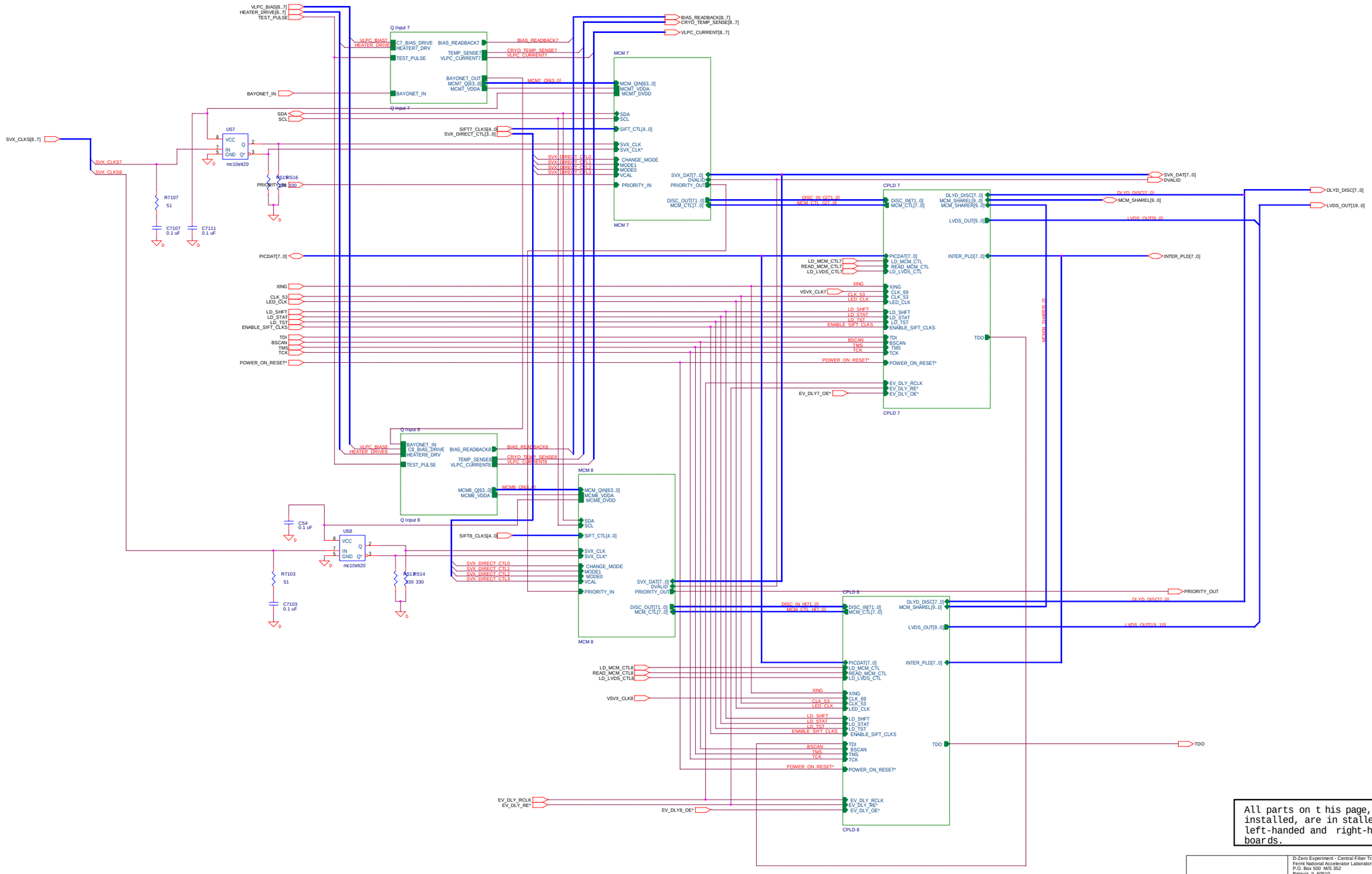
All parts on t his page, if installed, are in stalled in both left-handed and right-handed boards.

	D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End Fermi National Accelerator Laboratory P.O. Box 500 M/S 352 Batavia, IL 60510 <OrgAddd>			
	Sub-block Diagram, Qin,MCM,CPLD, #3,#4			
	Size D	CAGE Code <Cage Code>	DWG NO 3823-113-ED-330238	Rev C
Thursday, February 15, 2001	Scale		Sheet 7 of 42	



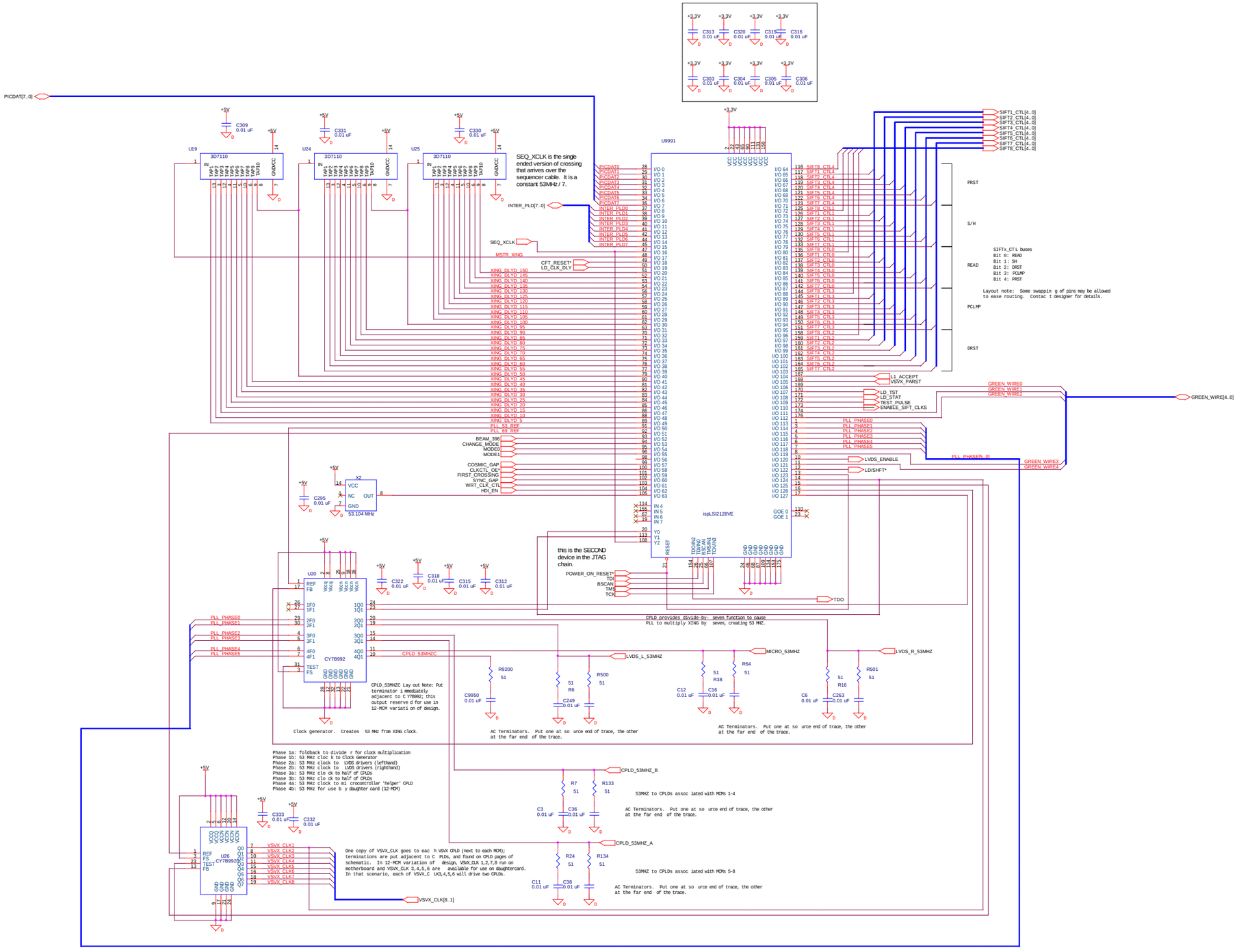
All parts on t his page, if installed, are in stalled in both left-handed and right-handed boards.

	D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End Fermi National Accelerator Laboratory P.O. Box 500 M/S 352 Batavia, IL 60510 <OrgAddr4>			
	Sub-block Diagram, Qin,MCM,CPLD, #5, #6			
	Size D	CAGE Code <Cage Code>	DWG NO 3823-113-ED-330238	Rev C
Thursday, February 15, 2001	Scale		Sheet 8 of 42	



All parts on t his page, if installed, are in stalled in both left-handed and right-handed boards.

	D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End Fermi National Accelerator Laboratory P.O. Box 500 M/S 352 Batavia, IL 60510 <OrgAddr4>			
	Sub-block Diagram, Qin,MCM,CPLD, #7, #8			
	Size D	CAGE Code <Cage Code>	DWG NO 3823-113-ED-330238	Rev C
Thursday, February 15, 2001	Scale		Sheet 9 of 42	



All parts on t his page, if installed, are in stalled in both left-handed and right-handed boards.

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510

Clock Generator

Size	CAGE Code	DWG NO	Rev
D		3823-113-ED-330238	C

Friday, February 16, 2001

Scale

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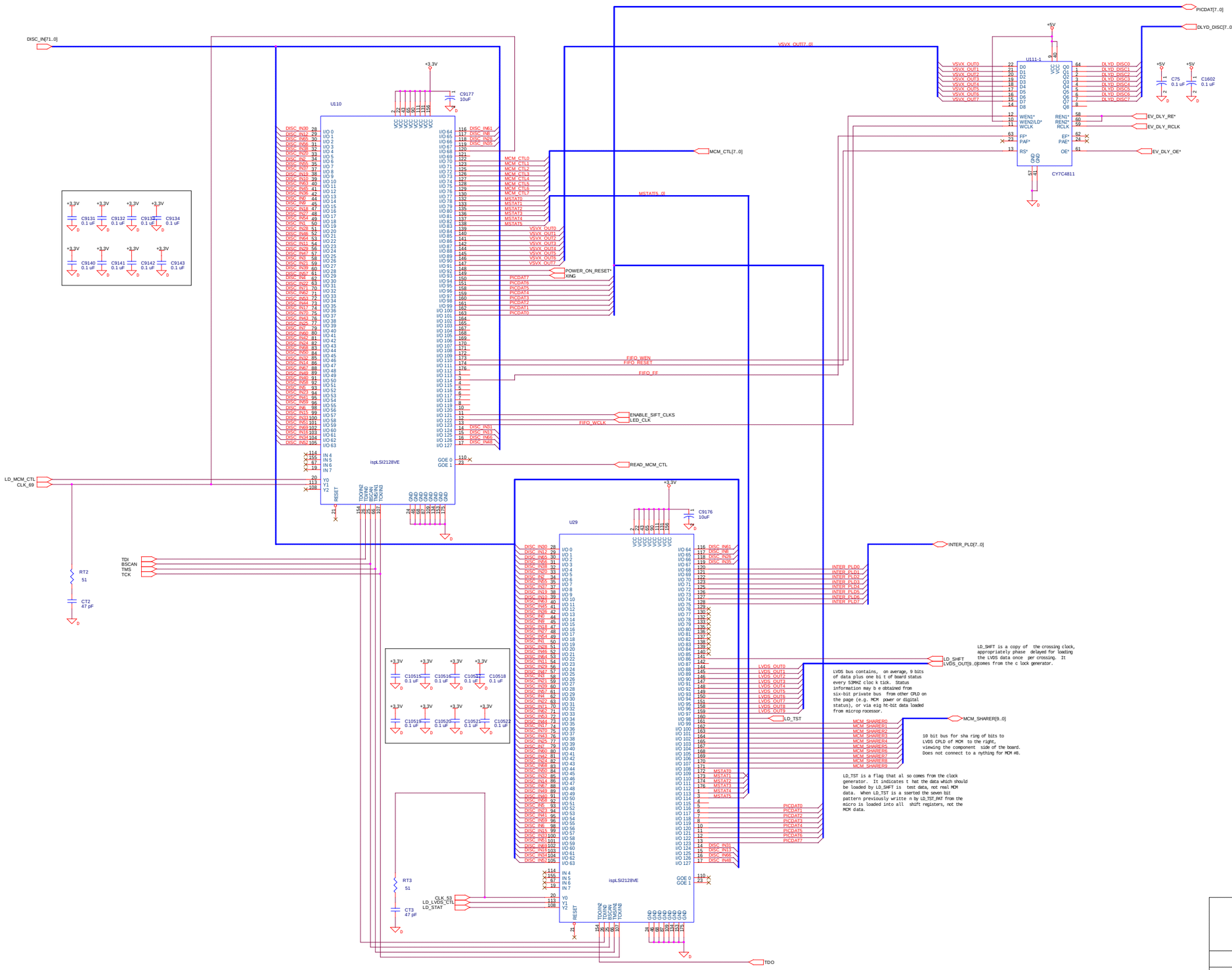
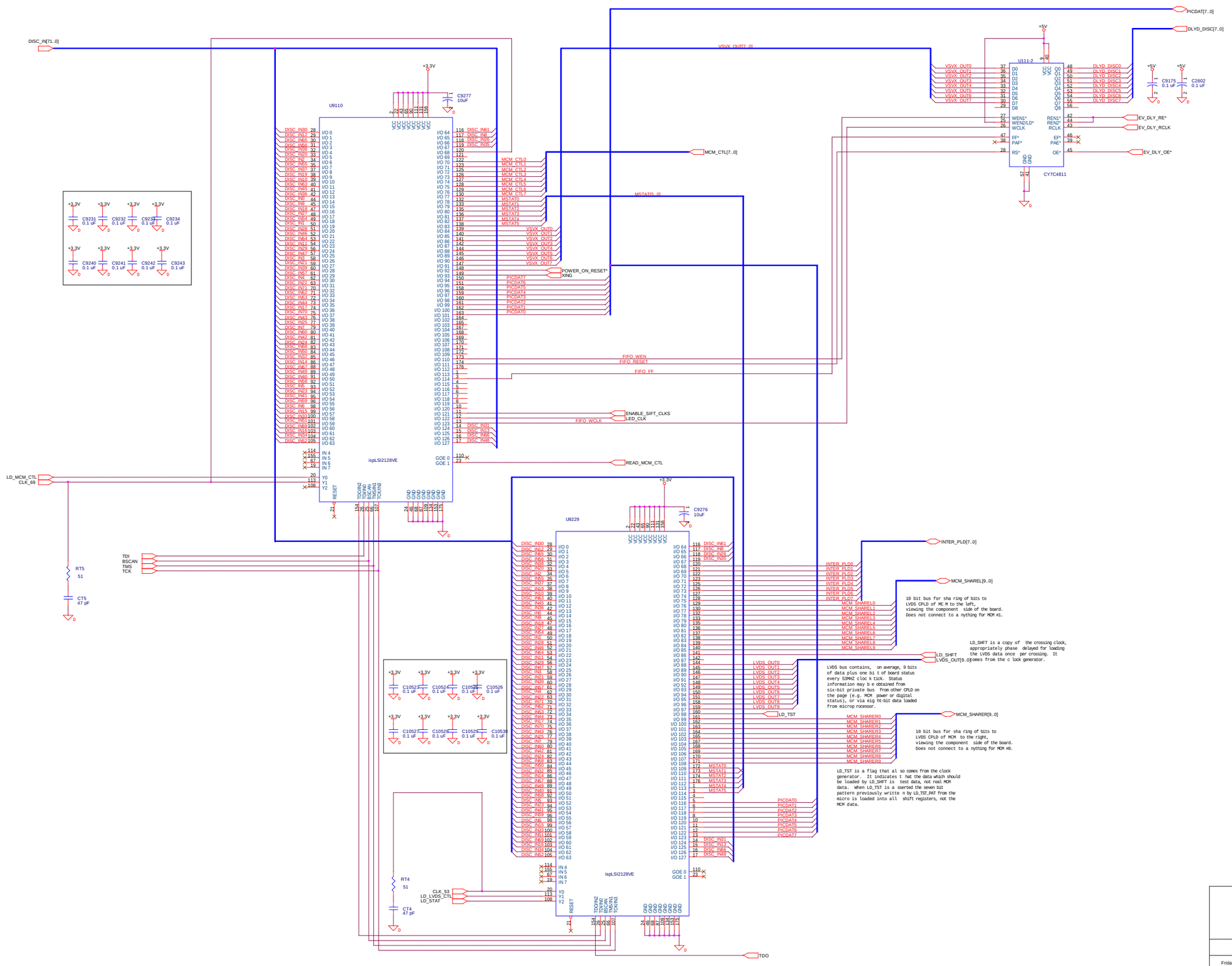
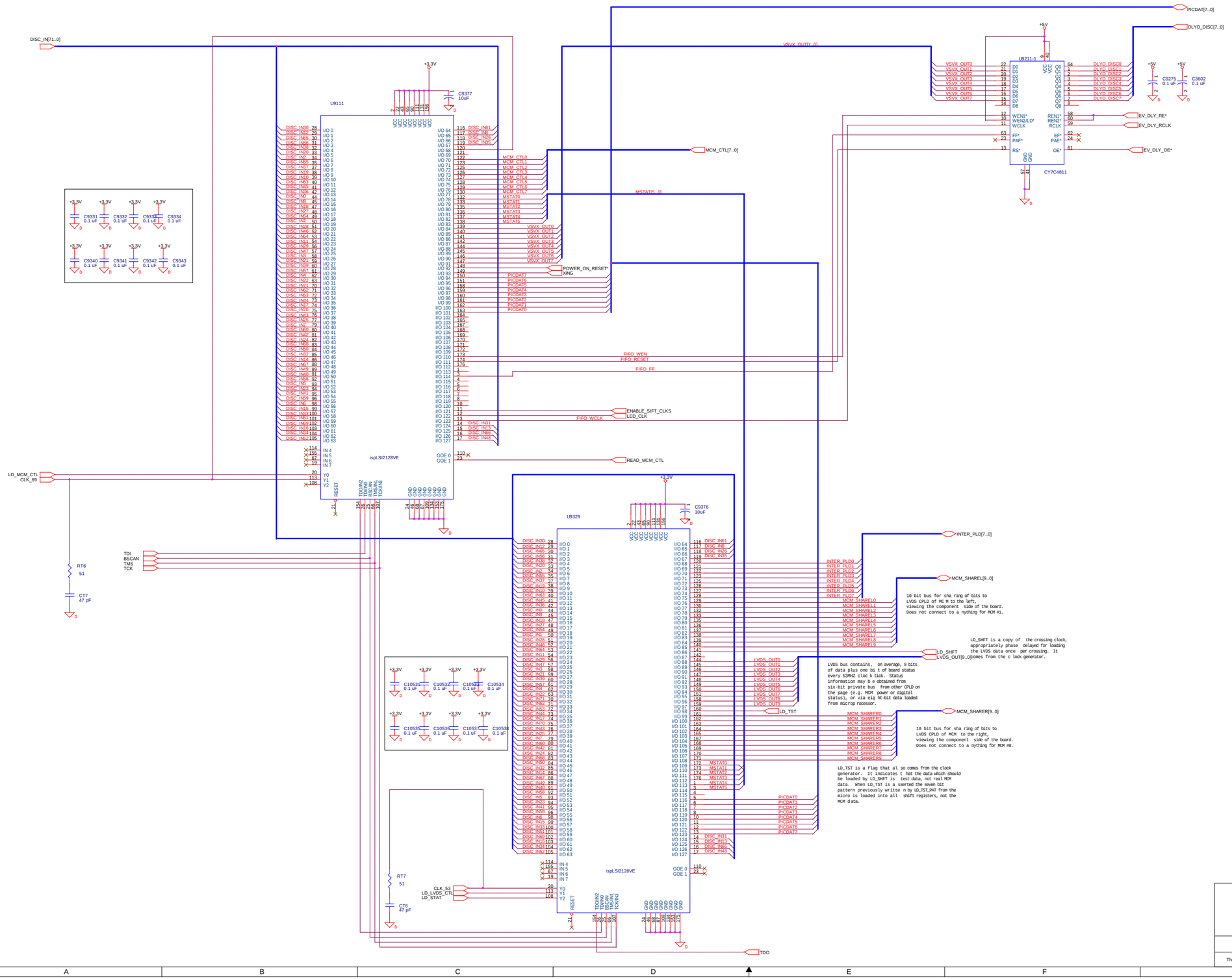

DISC_IN[71..0]
PICDAT[7..0]
DLYD_DISC[7..0]
VSVX_OUT[7..0]
U110
ispLSI2128VE
U29
U111-1
CY7C4811
MCM_CTL[7..0]
MSTAT[5..0]
POWER_ON_RESET*
XING
FIFO_WEN
FIFO_RESET
FIFO_FF
ENABLE_SIFT_CLKS
LED_CLK
FIFO_WCLK
READ_MCM_CTL
LD_MCM_CTL
CLK_69
TDI
BSCAN
TMS
TCK
RT2
51
CT2
47 pF
RT3
51
CT3
47 pF
CLK_53
LD_LVDS_CTL
LD_STAT
INTER_PLD[7..0]
EV_DLY_RE*
EV_DLY_RCLK
EV_DLY_OE*
LD_SHFT
LVDS_OUT[9..0]
LD_TST
MCM_SHARER[9..0]
TDO
LD_SHFT is a copy of the crossing clock, appropriately phase delayed for loading the LVDS data once per crossing. It comes from the c lock generator.
LVDS bus contains, on average, 9 bits of data plus one bi t of board status every 53MHZ cloc k tick. Status information may b e obtained from six-bit private bus from other CPLD on the page (e.g. MCM power or digital status), or via eig ht-bit data loaded from microp rocessor.
10 bit bus for sha ring of bits to LVDS CPLD of MCM to the right, viewing the component side of the board. Does not connect to a nything for MCM #8.
LD_TST is a flag that al so comes from the clock generator. It indicates t hat the data which should be loaded by LD_SHFT is test data, not real MCM data. When LD_TST is a sserted the seven bit pattern previously writte n by LD_TST_PAT from the micro is loaded into all shift registers, not the MCM data.
All parts on t his page, if installed, are in stalled in both left-handed and right-handed boar ds.
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 MS 352
Batavia, IL 60510
<Organization>
VSVX and LVDS data serializers, MCM #1
Size D
CAGE Code <Cage Code>
DWG NO 3823-113-ED-330238
Rev C
Scale
Friday, February 16, 2001
Sheet 11 of 42



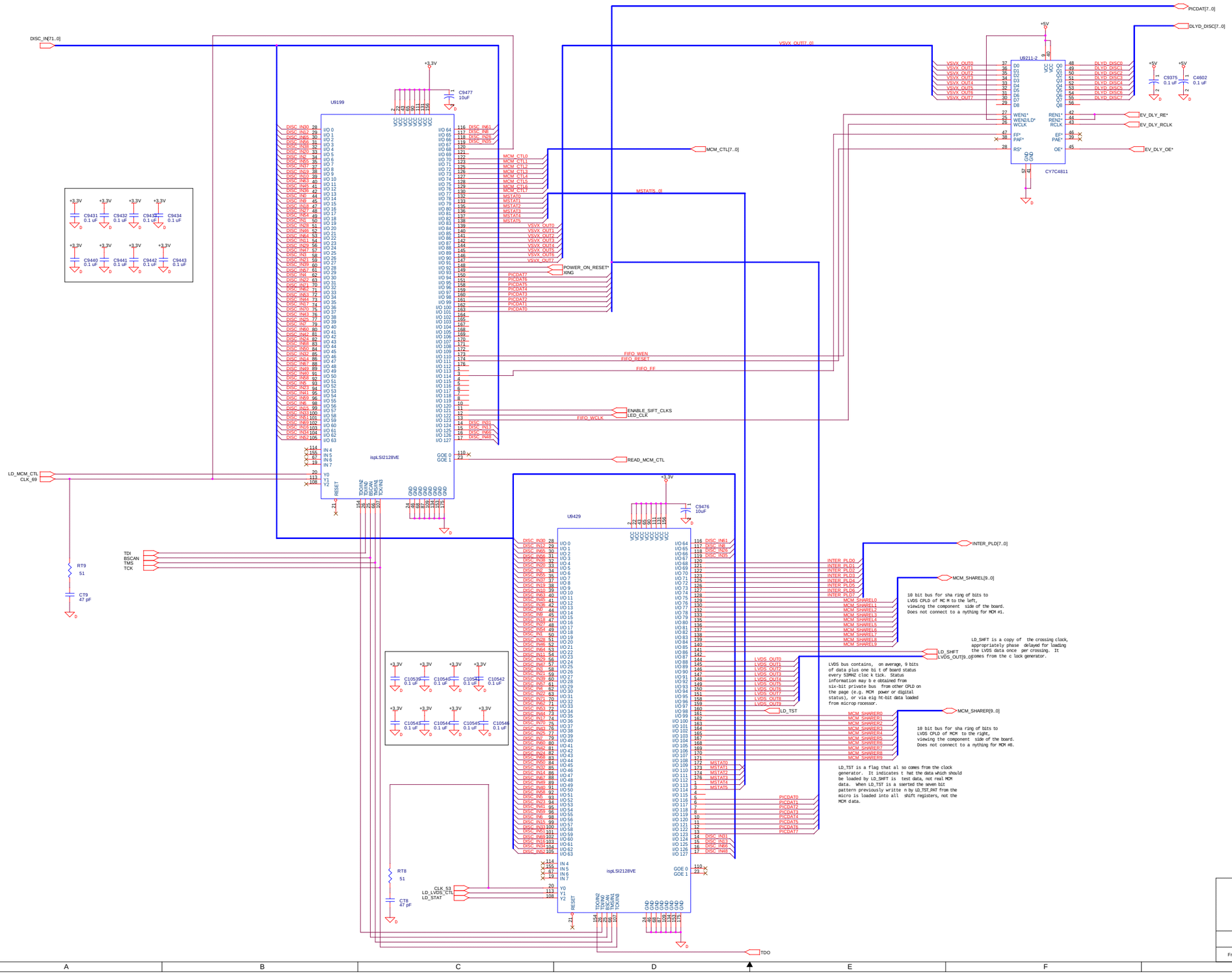
All parts on t his page, if installed, are in stalled in both left-handed and right-handed boar ds.

	D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End Fermi National Accelerator Laboratory P.O. Box 500 M/S 352 Batavia, IL 60510 <OrgAddr4>			
	VSVX and LVDS data serializers, MCM #2			
	Size D	CAGE Code <Cage Code>	DWG NO 3823-113-ED-330238	Rev C
Friday, February 16, 2001	Scale		Sheet 12 of 42	



All parts on t his page, if installed, are in stalled in both left-handed and right-handed boar ds.

	D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End Fermi National Accelerator Laboratory P.O. Box 500 M/S 352 Batavia, IL 60510 <OrgAddd4>			
	VSVX and LVDS data serializers, MCM #3			
	Size D	CAGE Code <Cage Code>	DWG NO 3823-113-ED-330238	Rev C
Thursday, February 15, 2001	Scale		Sheet 13 of 42	



10 bit bus for sha ring of bits to LVDS CPLD of MC M to the left, viewing the component side of the board. Does not connect to a nything for MCM #1.

LD_SHFT is a copy of the crossing clock, appropriately phase delayed for loading the LVDS data once per crossing. It comes from the c lock generator.

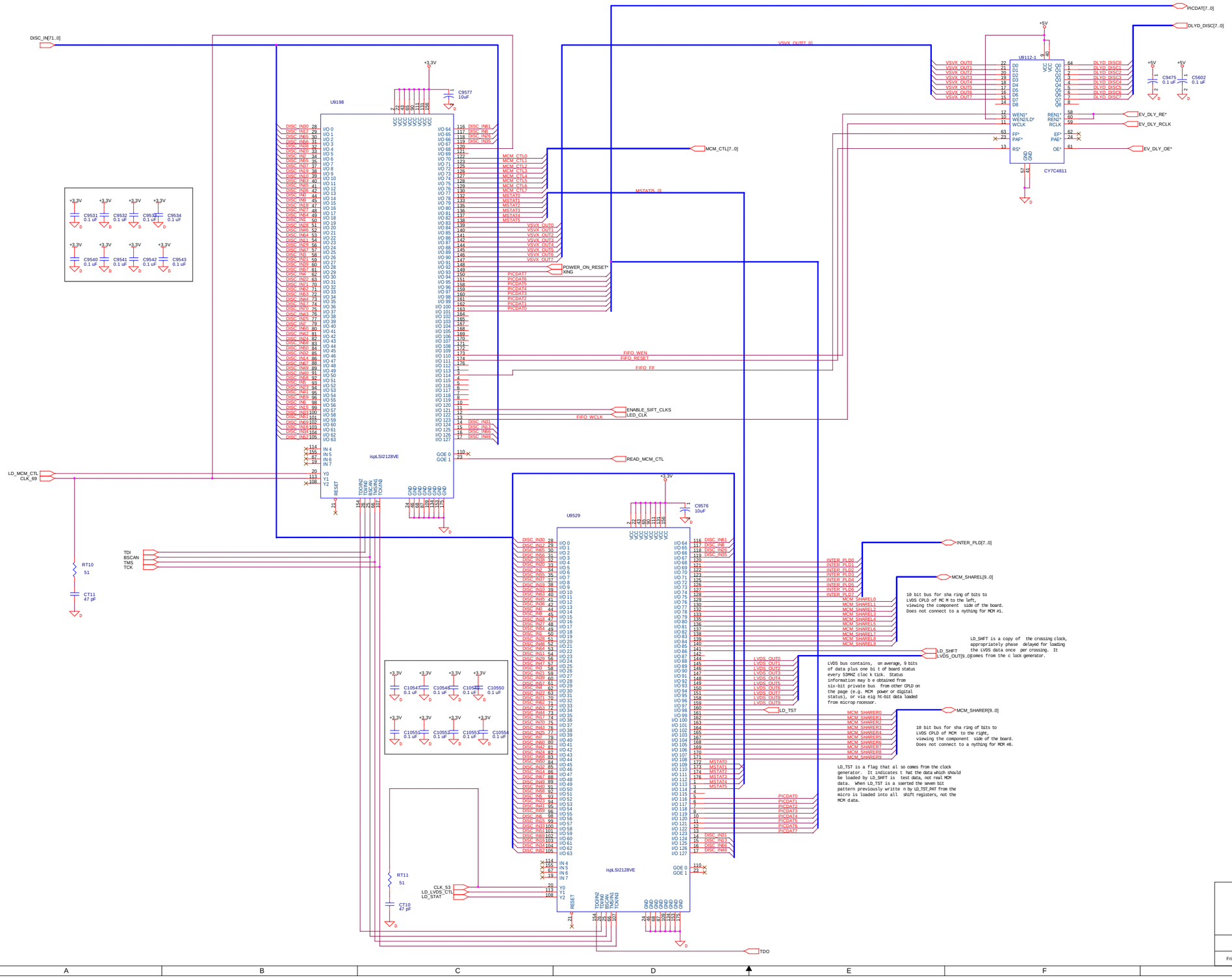
LVDS bus contains, on average, 9 bits of data plus one bi t of board status every 53MHZ cloc k tick. Status information may b e obtained from six-bit private bus from other CPLD on the page (e.g. MCM power or digital status), or via eig ht-bit data loaded from microp rocessor.

10 bit bus for sha ring of bits to LVDS CPLD of MCM to the right, viewing the component side of the board. Does not connect to a nything for MCM #6.

LD_TST is a flag that al so comes from the clock generator. It indicates t hat the data which should be loaded by LD_SHFT is test data, not real MCM data. When LD_TST is a sserted the seven bit pattern previously writte n by LD_TST_PAT from the micro is loaded into all shift registers, not the MCM data.

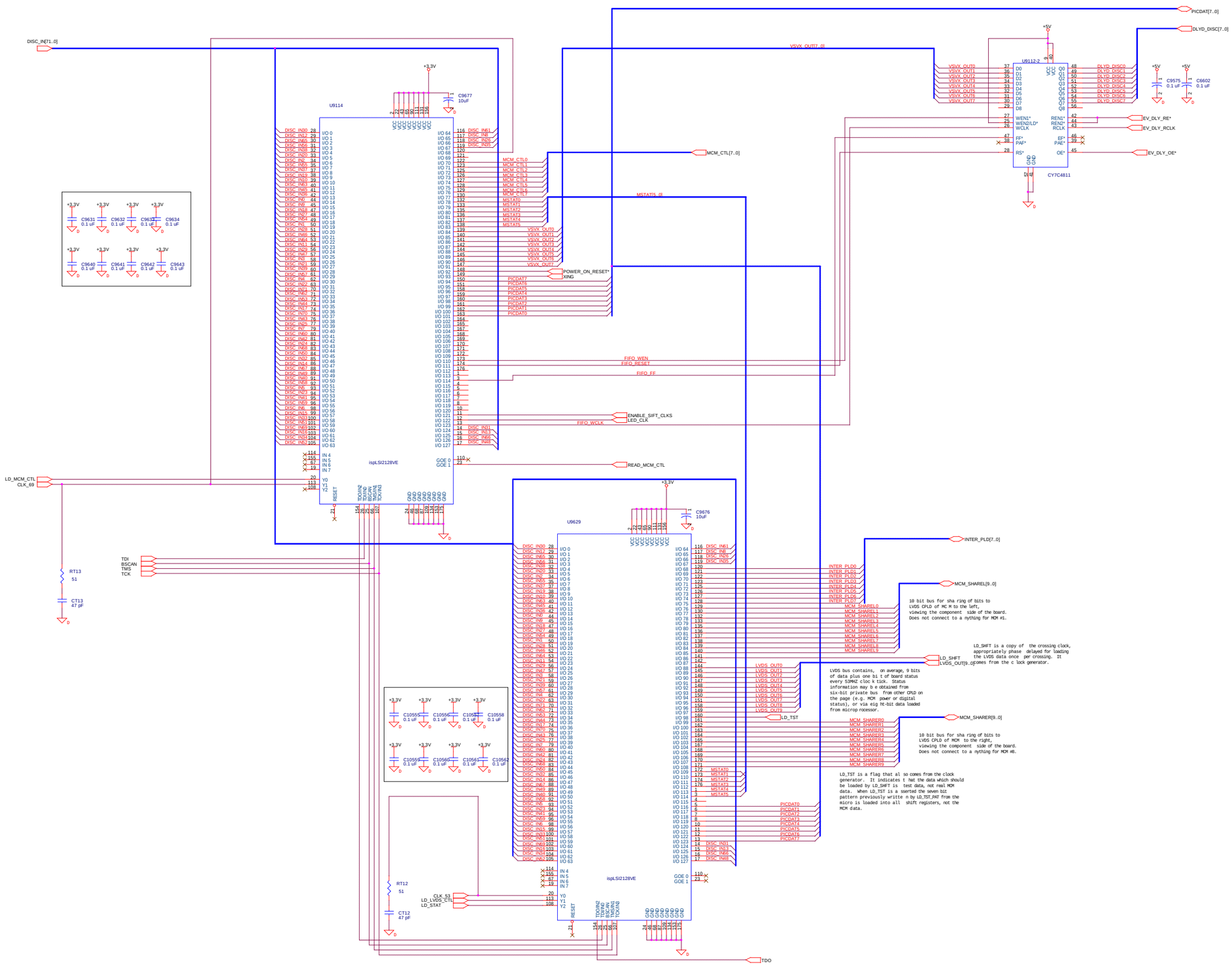
All parts on t his page, if installed, are in stalled in both left-handed and right-handed boar ds.

	D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End Fermi National Accelerator Laboratory P.O. Box 500 M/S 352 Batavia, IL 60510 <OrgAddr3>			
	VSVX and LVDS data serializers, MCM #4			
Friday, February 16, 2001	Size D	CAGE Code <Cage Code>	DWG NO 3823-113-ED-330238	Rev C
	Scale		Sheet 14 of 42	



All parts on t his page, if installed, are in stalled in both left-handed and right-handed boards.

	D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End Fermi National Accelerator Laboratory P.O. Box 500 M/S 352 Batavia, IL 60510 <OrgAddr4>		
	VSVX and LVDS data serializers, MCM #5		
	Size: D	CAGE Code: <Cage Code>	DWG NO: 3823-113-ED-330238	Rev: C
Friday, February 16, 2001	Scale		Sheet 15 of 42



All parts on t his page, if installed, are in stalled in both left-handed and right-handed boar ds.

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
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Batavia, IL 60510
<OrgAddr2>

VSVX and LVDS data serializers, MCM #6

Size	CAGE Code	DWG NO	Rev
D	<Cage Code>	3823-113-ED-330238	C

Thursday, February 15, 2001

Scale

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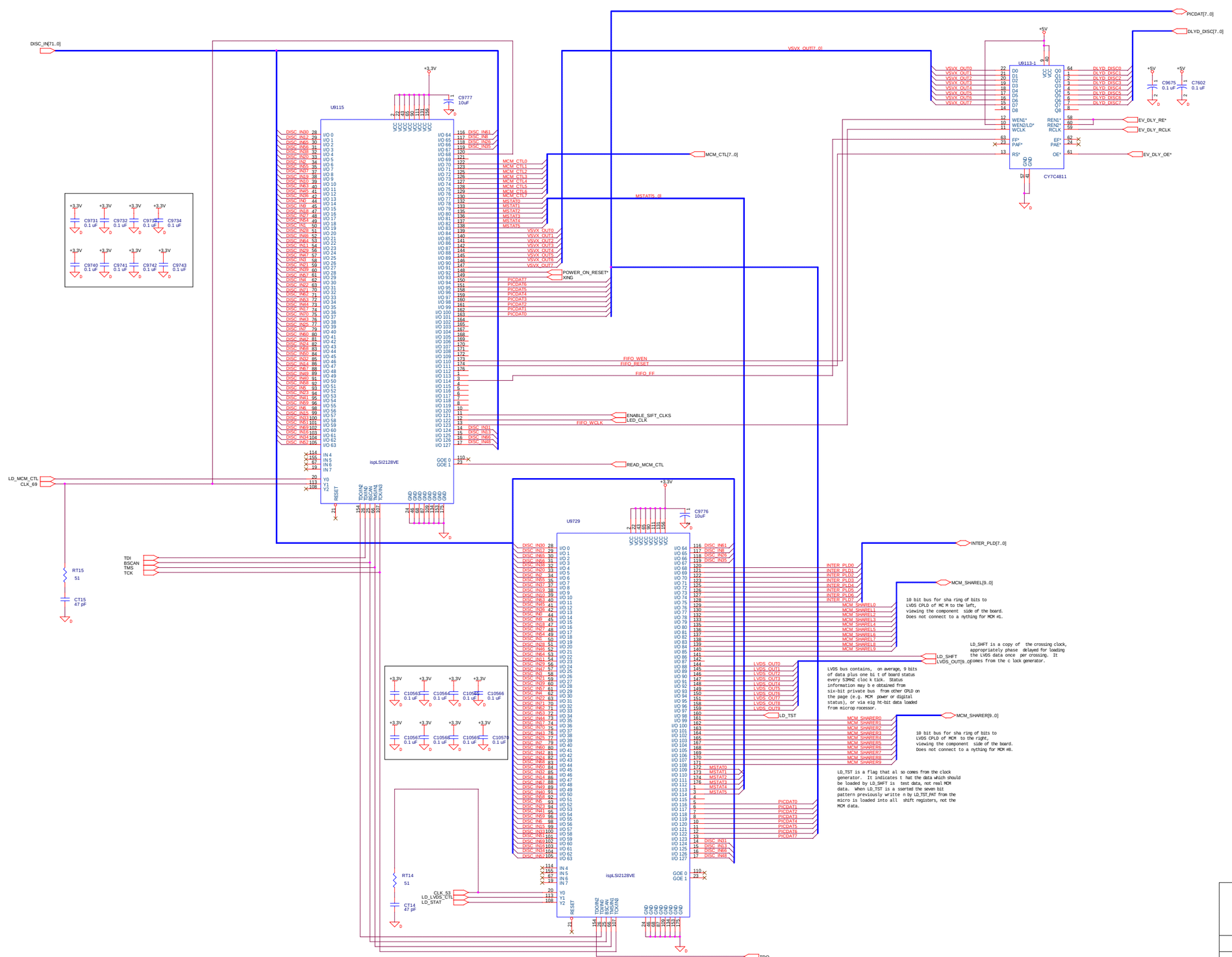
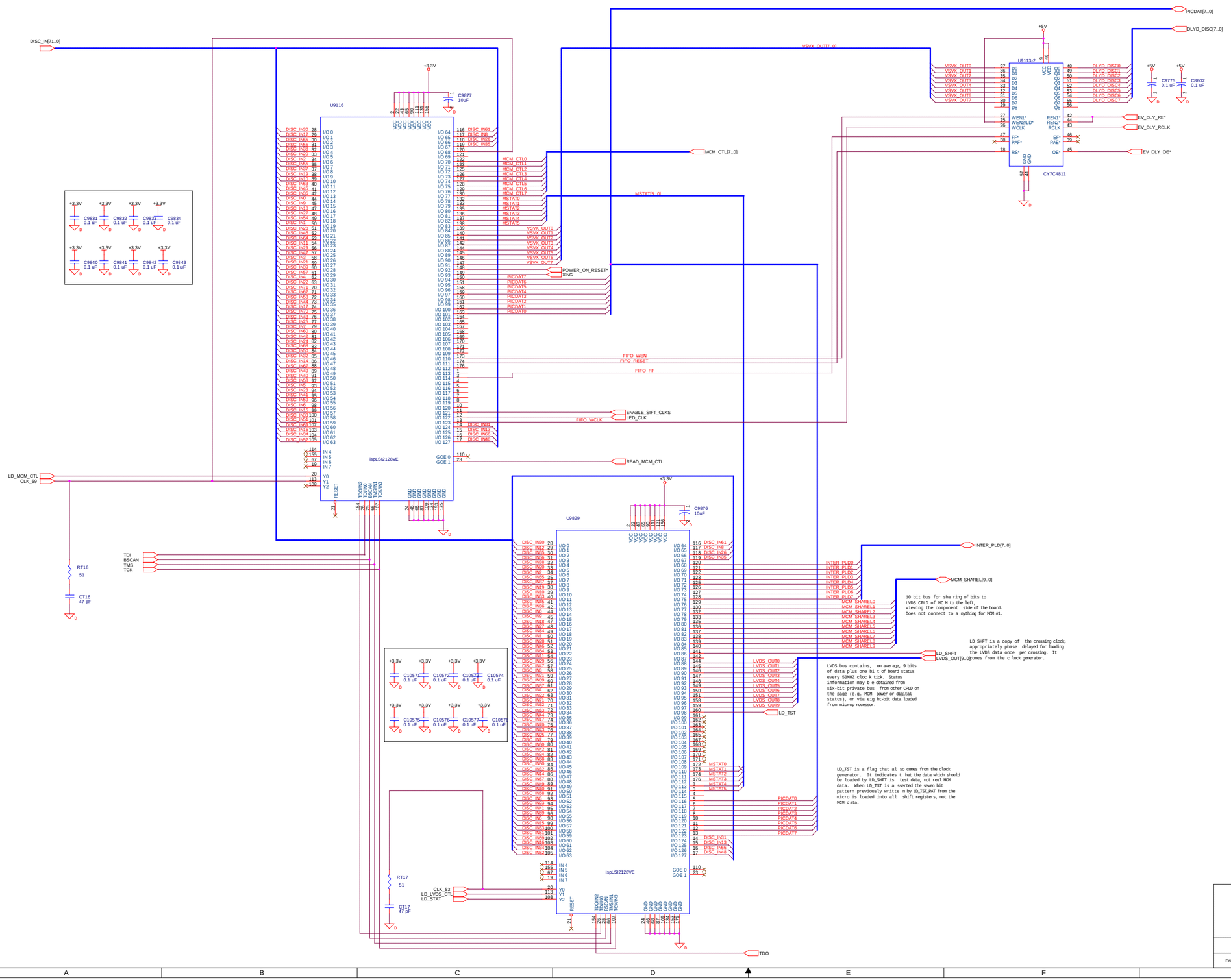


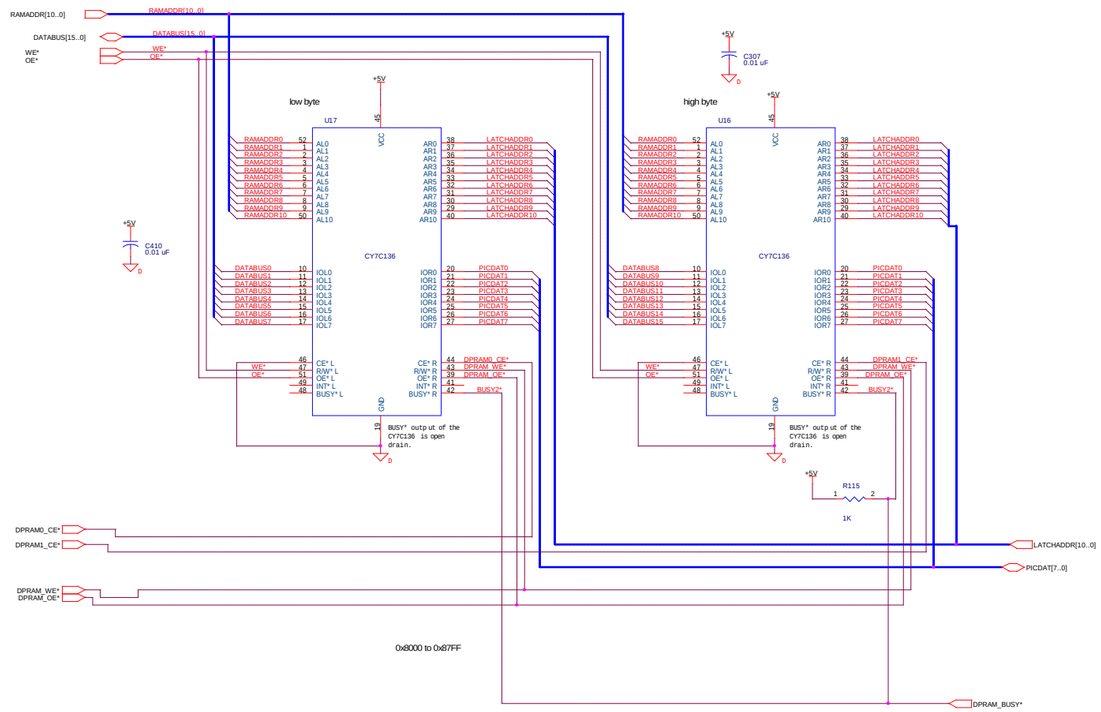
All parts on t his page, if installed, are in stalled in both left-handed and right-handed boar ds.

	D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End Fermi National Accelerator Laboratory P.O. Box 500 M/S 352 Batavia, IL 60510 <OrgAddr3>			
	VSVX and LVDS data serializers, MCM #7			
	Size D	CAGE Code <Cage Code>	DWG NO 3823-113-ED-330238	Rev C
Friday, February 16, 2001	Scale		Sheet 17 of 42	



All parts on t his page, if installed, are in stalled in both left-handed and right-handed boar ds.

	D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End Fermi National Accelerator Laboratory P.O. Box 500 M/S 352 Batavia, IL 60510 <OrgAddr4>			
	VSVX and LVDS data serializers, MCM #8			
	Size D	CAGE Code <Cage Code>	DWG NO 3823-113-ED-330238	Rev C
Friday, February 16, 2001	Scale		Sheet 18 of 42	



All parts on t his page, if installed, are in stalled in both left-handed and right-handed boar ds.

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
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P.O. Box 500 M/S 352
Batavia, IL 60510

Dual-Port RAM

Size	CAGE Code	DWG NO	Rev
D		3823-113-ED-330238	C

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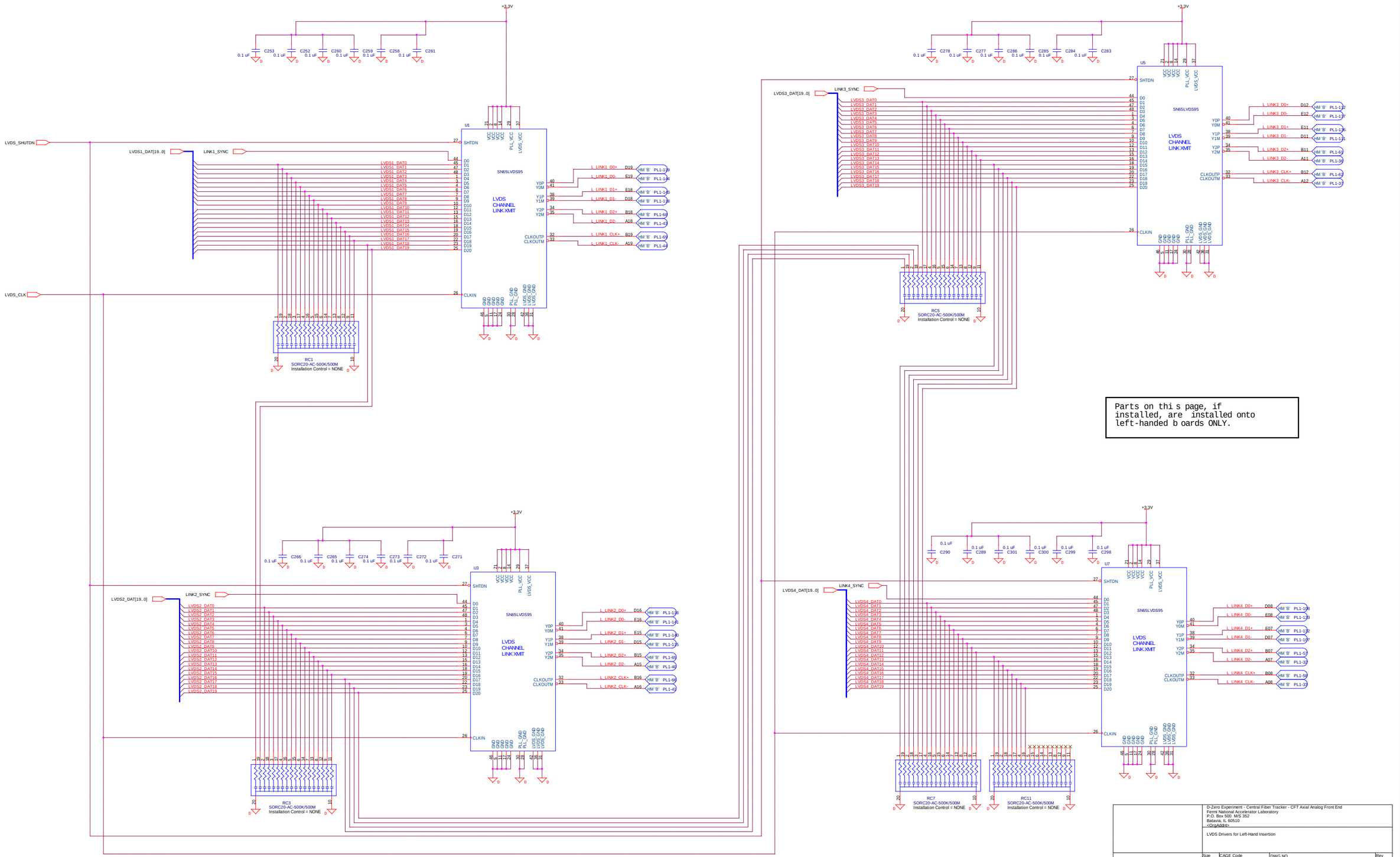

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
<OrgAddr4>

LVDS Drivers for Left-Hand Insertion

Size	CAGE Code	DWG NO	Rev
D	<Cage Code>	3823-113-ED-330238	C

Thursday, February 15, 2001

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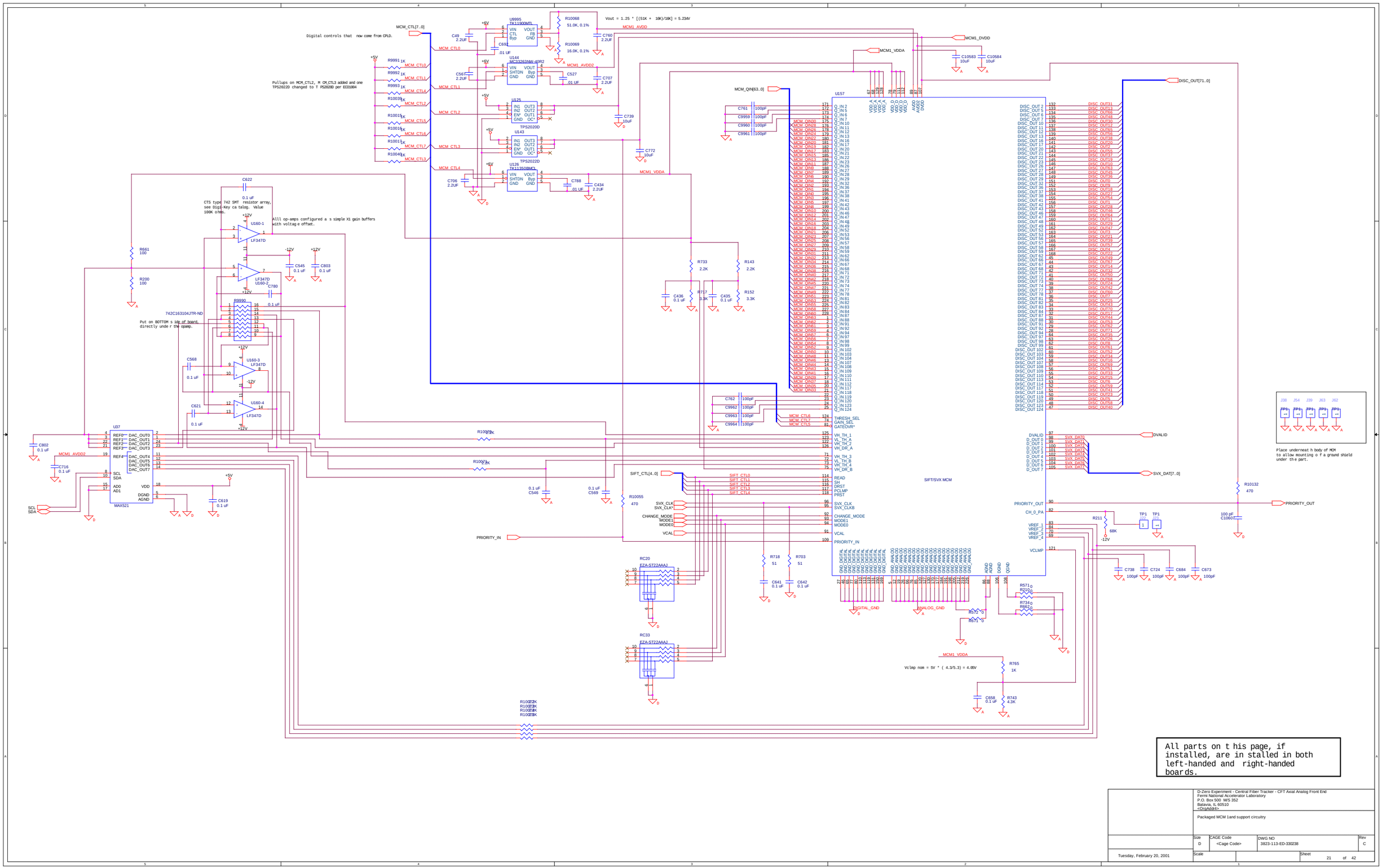

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
<OrgAddr4>

Packaged MCM 1and support circuitry

Size	CAGE Code	DWG NO	Rev
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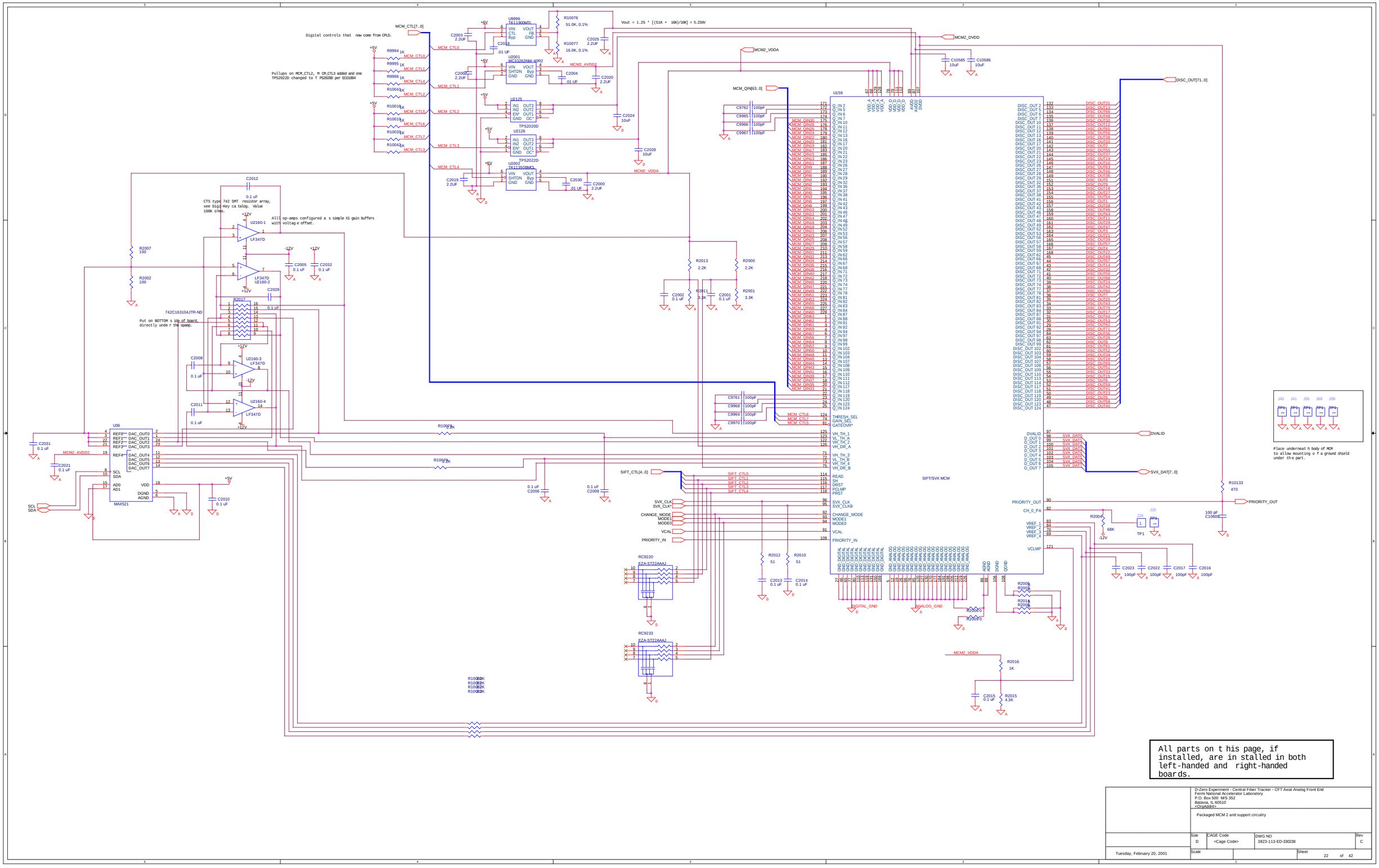
Digital controls that now come from CPLD.
Pullups on MCM_CTL2, M CM_CTL3 added and one TPS2022D changed to T PS2020D per ECO1004
Vout = 1.25 * [(51K + 16K)/16K] = 5.234V
CTS type 742 SMT resistor array, see Digi-Key ca talog. Value 100K ohms.
All op-amps configured a s simple X1 gain buffers with voltag e offset.
Put on BOTTOM s ide of board, directly unde r the opamp.
742C163104JTR-ND
Place underneat h body of MCM to allow mounting o f a ground shield under th e part.
All parts on t his page, if installed, are in stalled in both left-handed and right-handed boards.
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
Packaged MCM 2 and support circuitry
Size D
CAGE Code <Cage Code>
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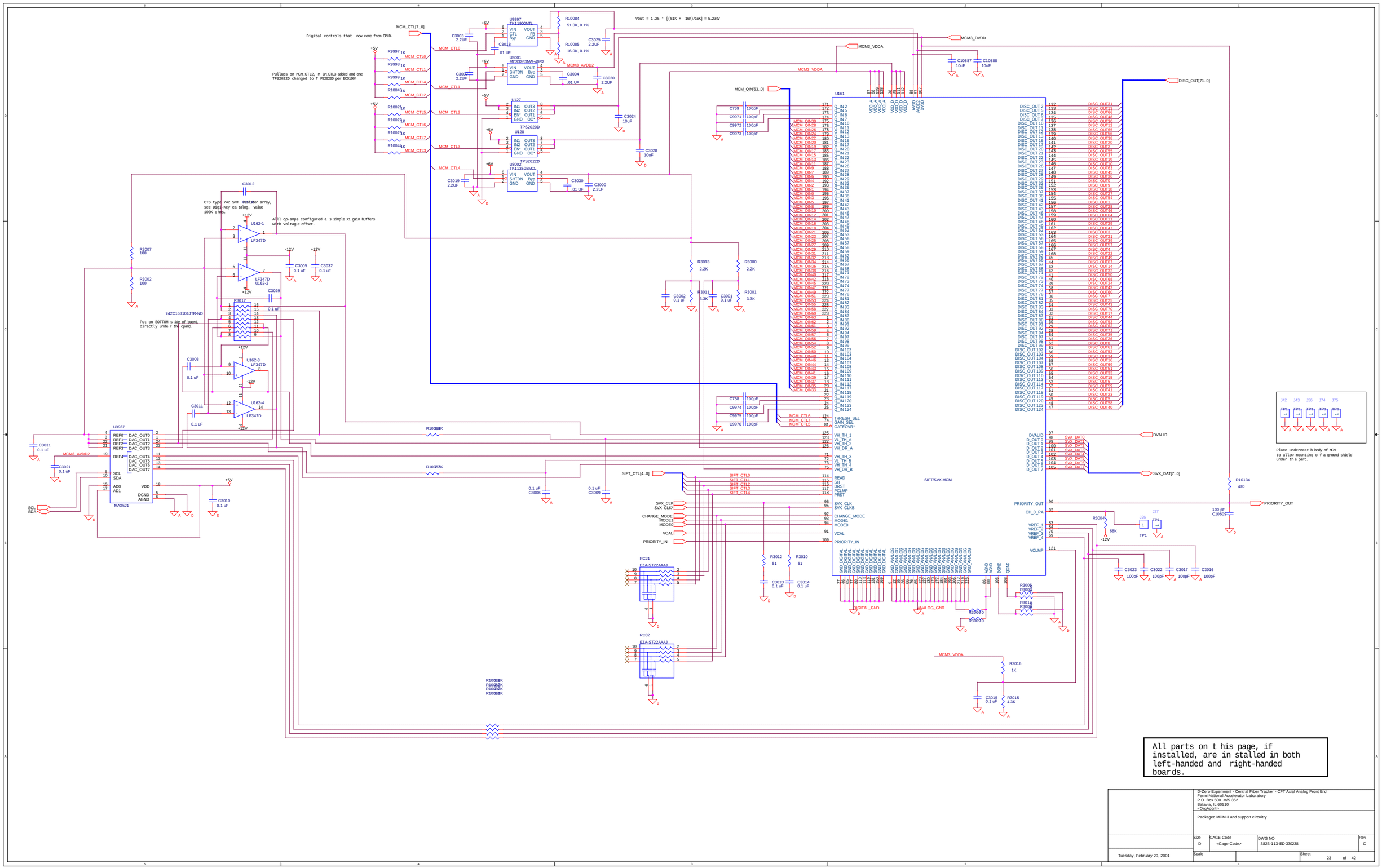
Digital controls that now come from CPLD.
Pullups on MCM_CTL2, M CM_CTL3 added and one TPS2022D changed to T PS2020D per ECO1004
Vout = 1.25 * [(51K + 16K)/16K] = 5.234V
CTS type 742 SMT resistor array, see Digi-Key ca talog. Value 100K ohms.
All op-amps configured a s simple X1 gain buffers with voltag e offset.
742C163104JTR-ND
Put on BOTTOM s ide of board, directly unde r the opamp.
Place underneat h body of MCM to allow mounting o f a ground shield under th e part.
All parts on t his page, if installed, are in stalled in both left-handed and right-handed boar ds.
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
Packaged MCM 3 and support circuitry
Size D
CAGE Code <Cage Code>
DWG NO 3823-113-ED-330238
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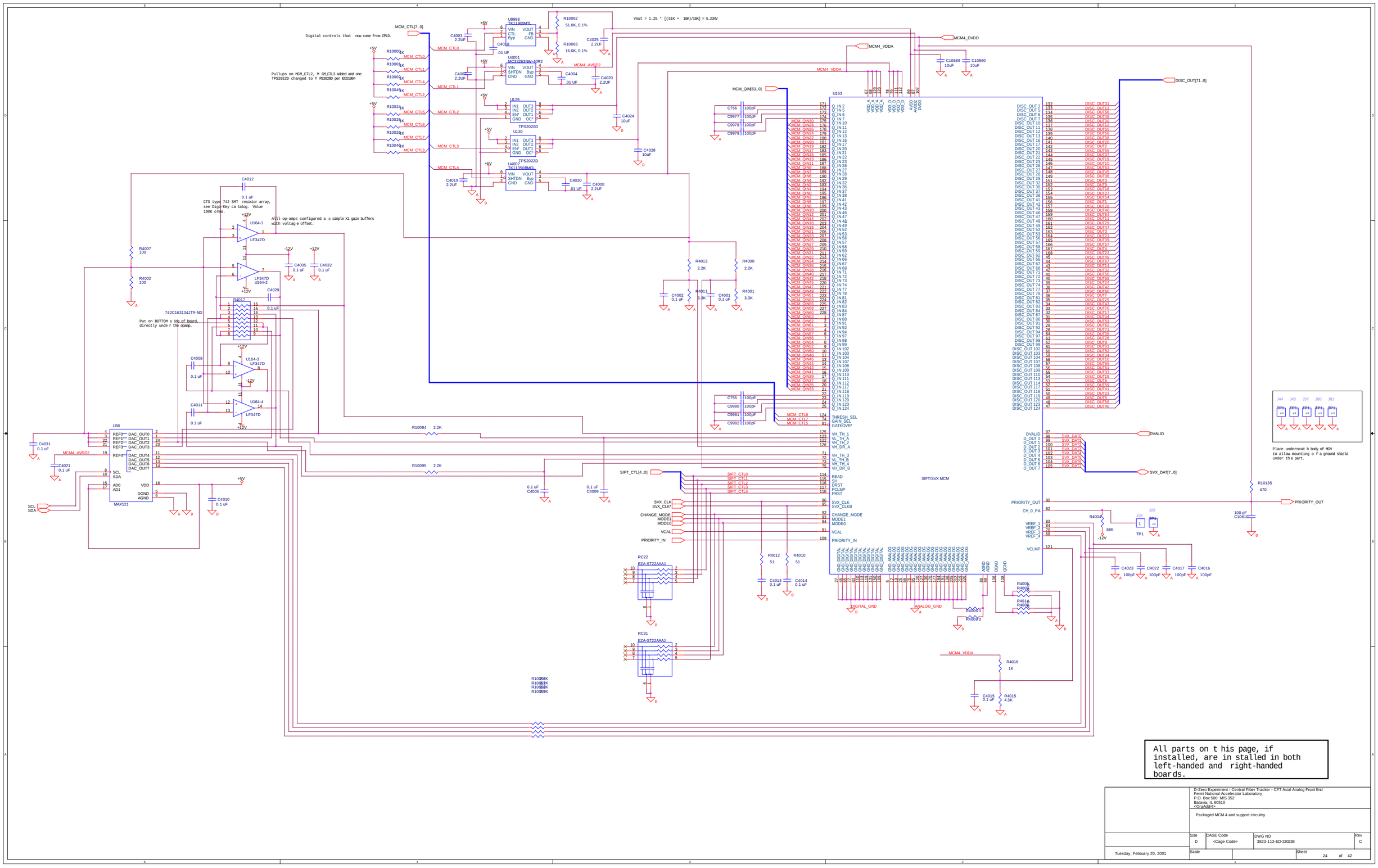
Digital controls that now come from CPLD.
Pullups on MCM_CTL2, M CM_CTL3 added and one TPS2022D changed to T PS2020D per ECO1004
Vout = 1.25 * [(51K + 16K)/16K] = 5.234V
CTS type 742 SMT resistor array, see Digi-Key ca talog. Value 100K ohms.
All op-amps configured a s simple X1 gain buffers with voltag e offset.
Put on BOTTOM s ide of board, directly unde r the opamp.
742C163104JTR-ND
Place underneat h body of MCM to allow mounting o f a ground shield under th e part.
All parts on t his page, if installed, are in stalled in both left-handed and right-handed boards.
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
Packaged MCM 4 and support circuitry
Size D
CAGE Code <Cage Code>
DWG NO 3823-113-ED-330238
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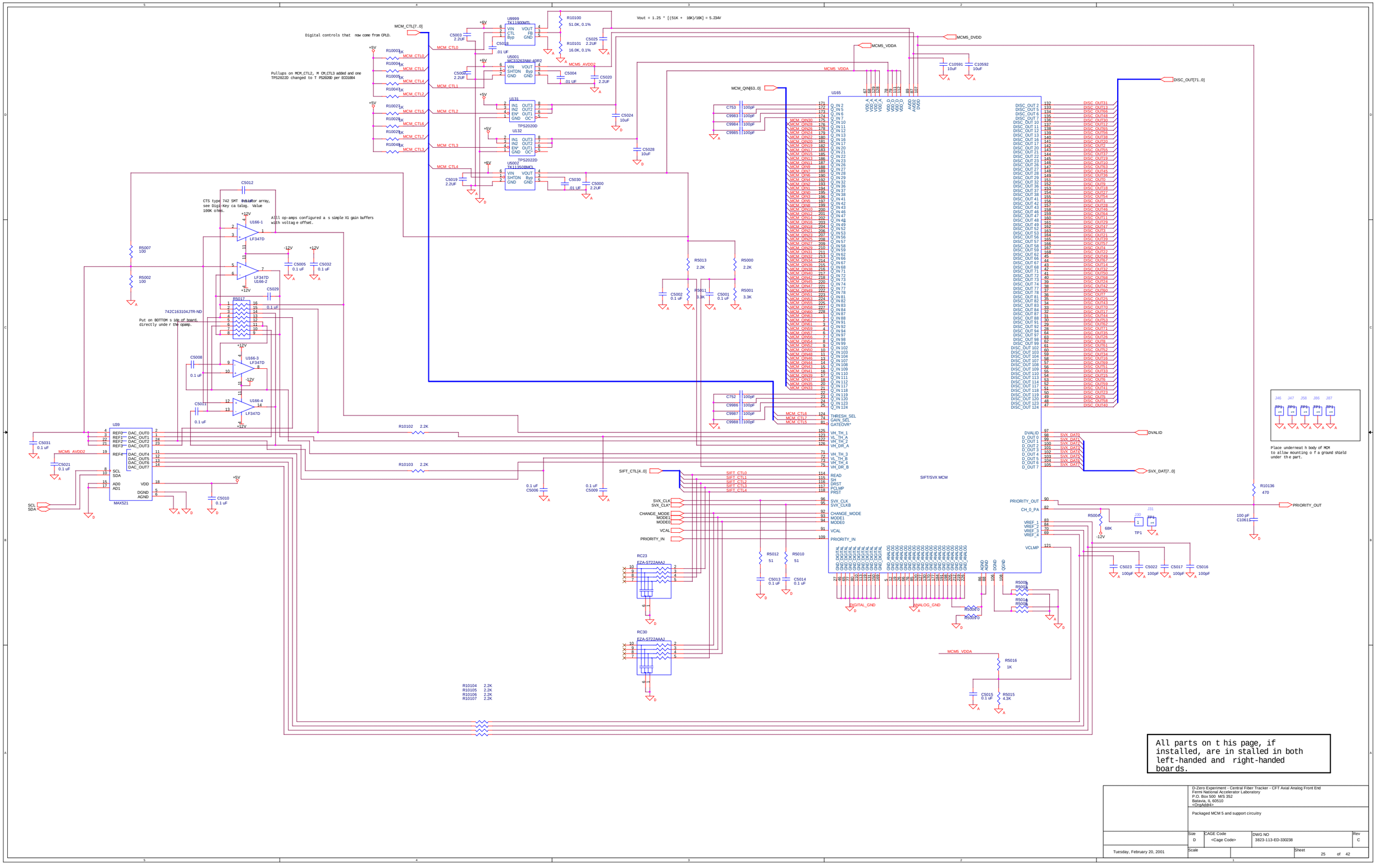

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
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Batavia, IL 60510
<OrgAddr4>

Packaged MCM 5 and support circuitry

Size	CAGE Code	DWG NO	Rev
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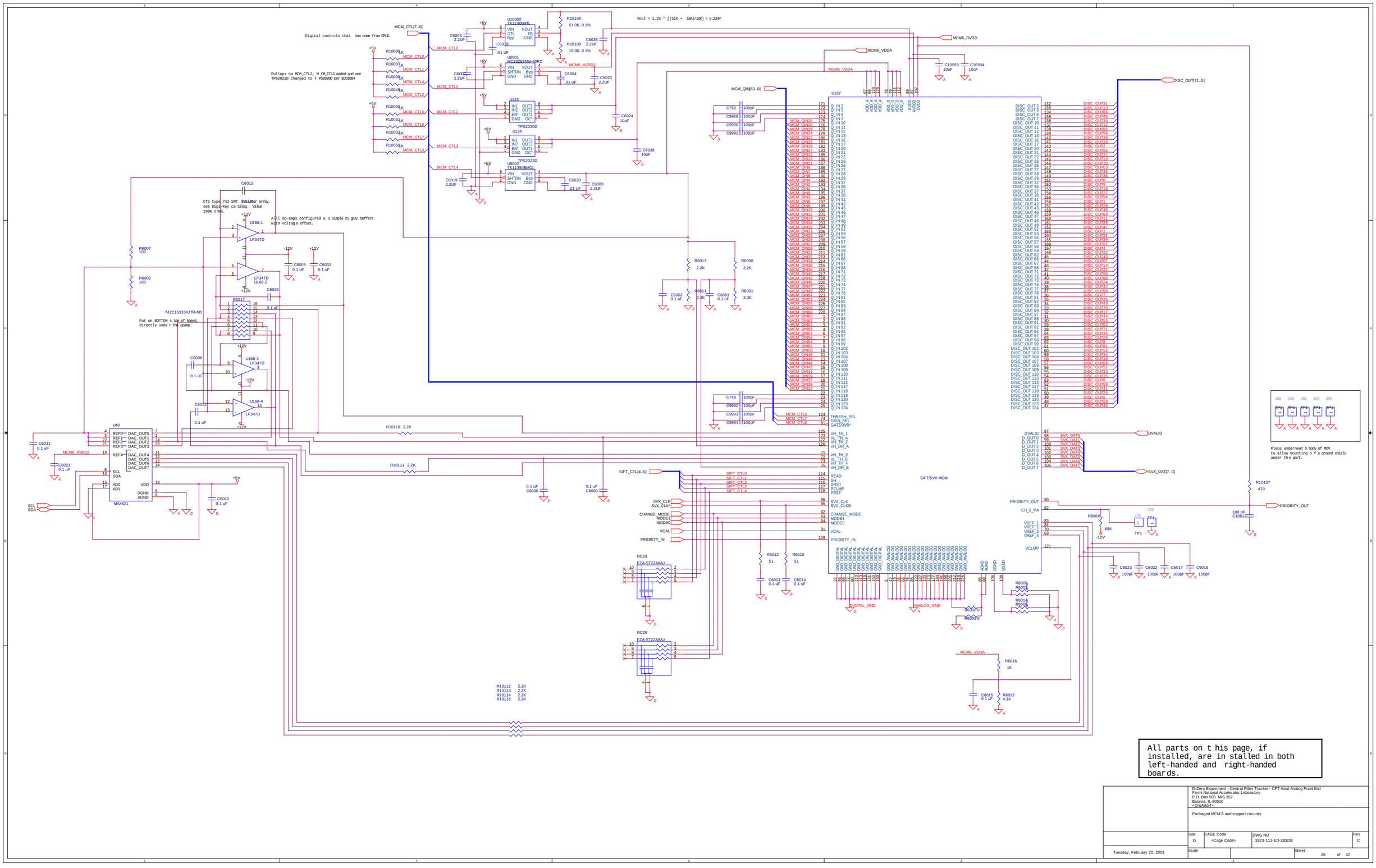
Vout = 1.25 * [(51K + 10K)/10K] = 5.234V
Digital controls that now come from CPLD.
Pullups on MCM_CTL2, M CM_CTL3 added and one TPS2022D changed to T PS2020D per ECO1004
CTS type 742 SMT resistor array, see Digi-Key ca talog. Value 100K ohms.
All op-amps configured a s simple X1 gain buffers with voltag e offset.
742C163104JTR-ND
Put on BOTTOM s ide of board, directly unde r the opamp.
MAXS21
SIFT/SVX MCM
U167
Place underneat h body of MCM to allow mounting o f a ground shield under th e part.
All parts on t his page, if installed, are in stalled in both left-handed and right-handed boards.
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
<OrgAddr4>
Packaged MCM 6 and support circuitry
Size D
CAGE Code <Cage Code>
DWG NO 3823-113-ED-330238
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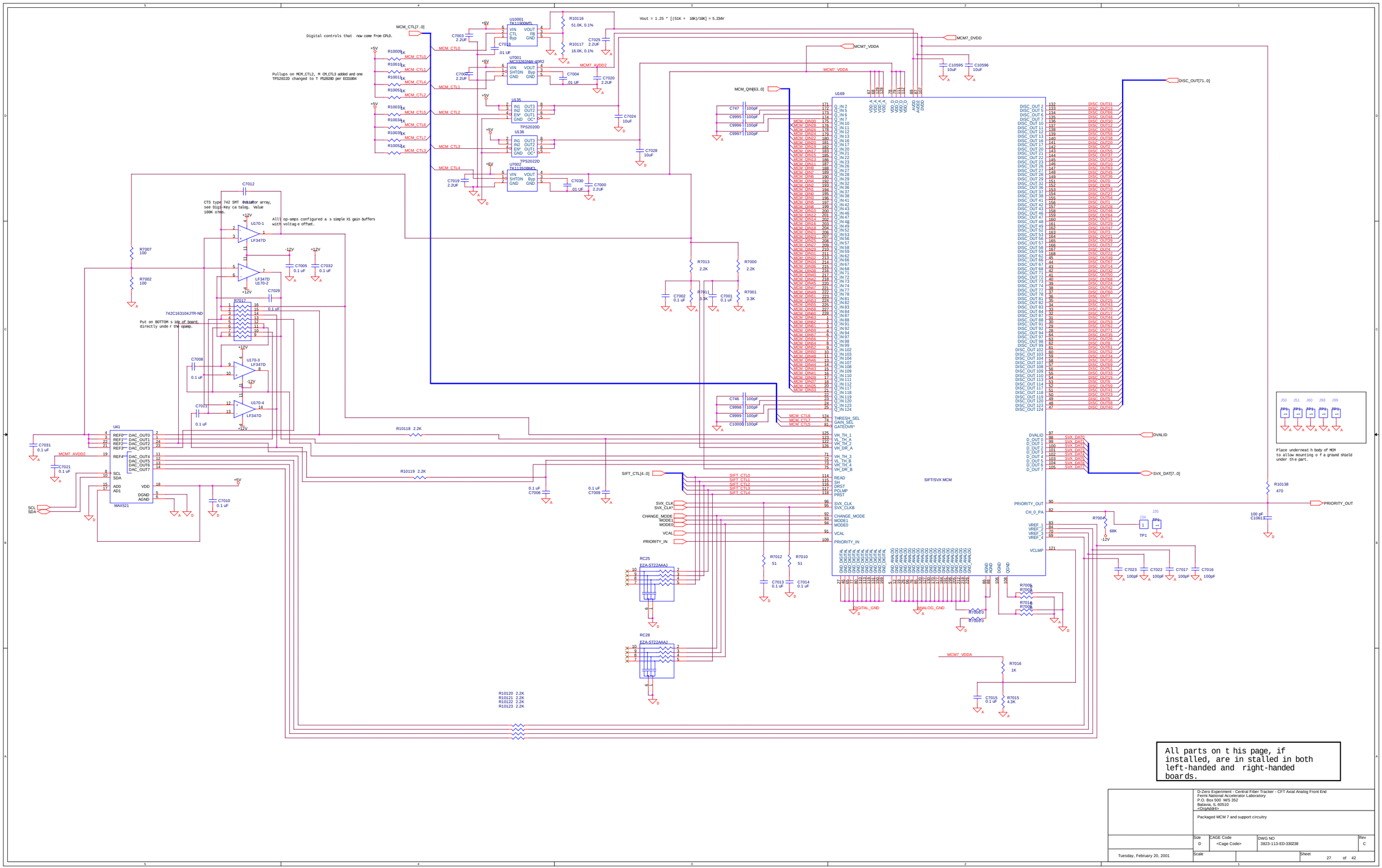
Digital controls that now come from CPLD.
Pullups on MCM_CTL2, M CM_CTL3 added and one TPS2022D changed to T PS2020D per ECO1004
Vout = 1.25 * [(51K + 10K)/10K] = 5.234V
CTS type 742 SMT resistor array, see Digi-Key ca talog. Value 100K ohms.
All op-amps configured a s simple X1 gain buffers with voltag e offset.
Put on BOTTOM s ide of board, directly unde r the opamp.
742C163104JTR-ND
Place underneat h body of MCM to allow mounting o f a ground shield under th e part.
SIFT/SVX MCM
All parts on t his page, if installed, are in stalled in both left-handed and right-handed boar ds.
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
Packaged MCM 7 and support circuitry
Size D
CAGE Code <Cage Code>
DWG NO 3823-113-ED-330238
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Tuesday, February 20, 2001
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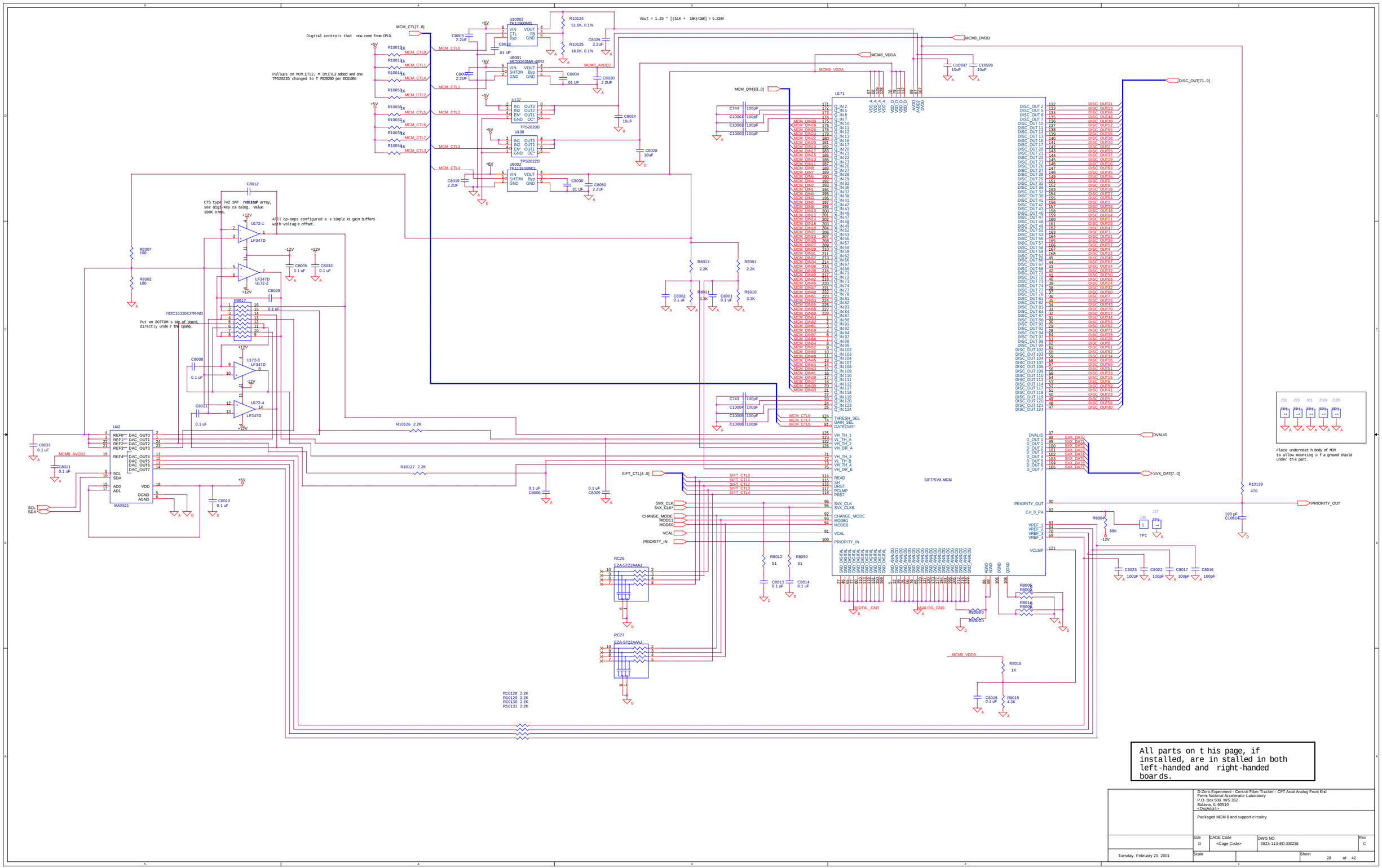
Vout = 1.25 * [(51K + 10K)/10K] = 5.234V
Digital controls that now come from CPLD.
Pullups on MCM_CTL2, M CM_CTL3 added and one TPS2022D changed to T PS2020D per ECO1004
CTS type 742 SMT resistor array, see Digi-Key ca talog. Value 100K ohms.
All op-amps configured a s simple X1 gain buffers with voltag e offset.
742C163104JTR-ND
Put on BOTTOM s ide of board, directly unde r the opamp.
Place underneat h body of MCM to allow mounting o f a ground shield under th e part.
All parts on t his page, if installed, are in stalled in both left-handed and right-handed boards.
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
Packaged MCM 8 and support circuitry
Size D
CAGE Code <Cage Code>
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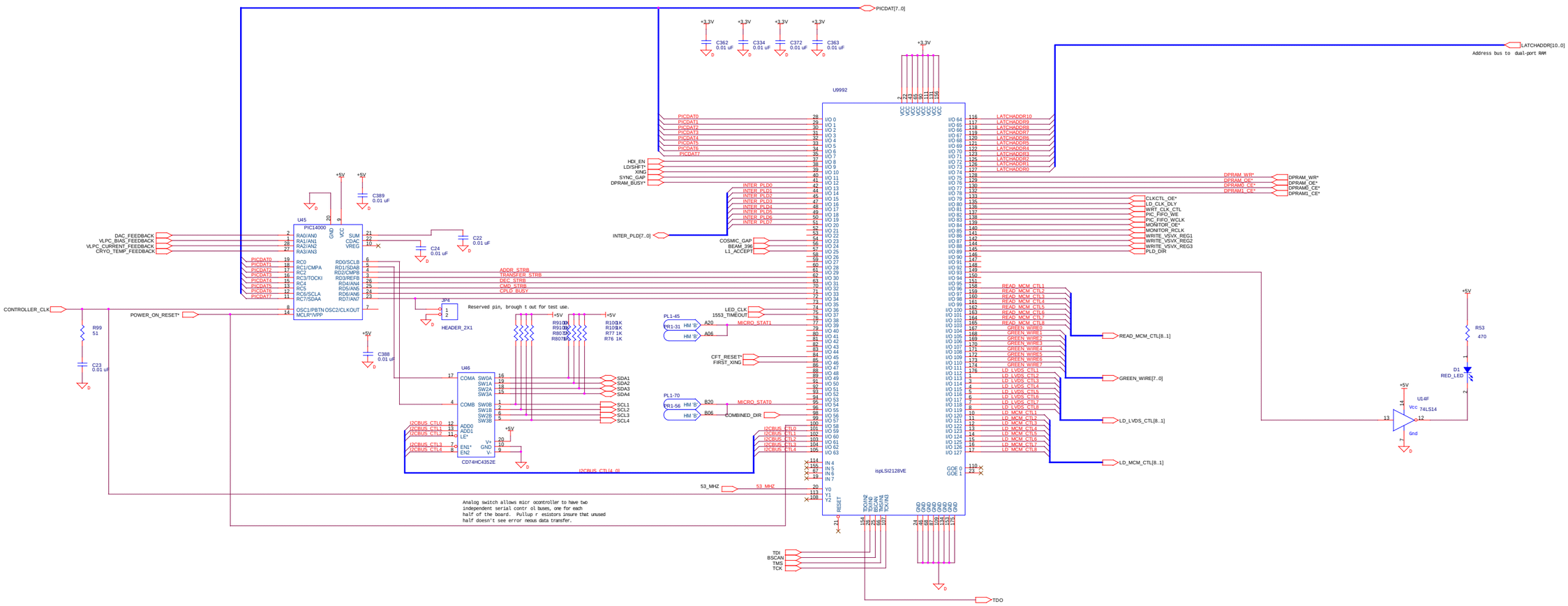

All parts on t his page, if installed, are in stalled in both left-handed and right-handed boards.

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
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Batavia, IL 60510

Microcontroller and Flash RAM

Size	CAGE Code	DWG NO	Rev
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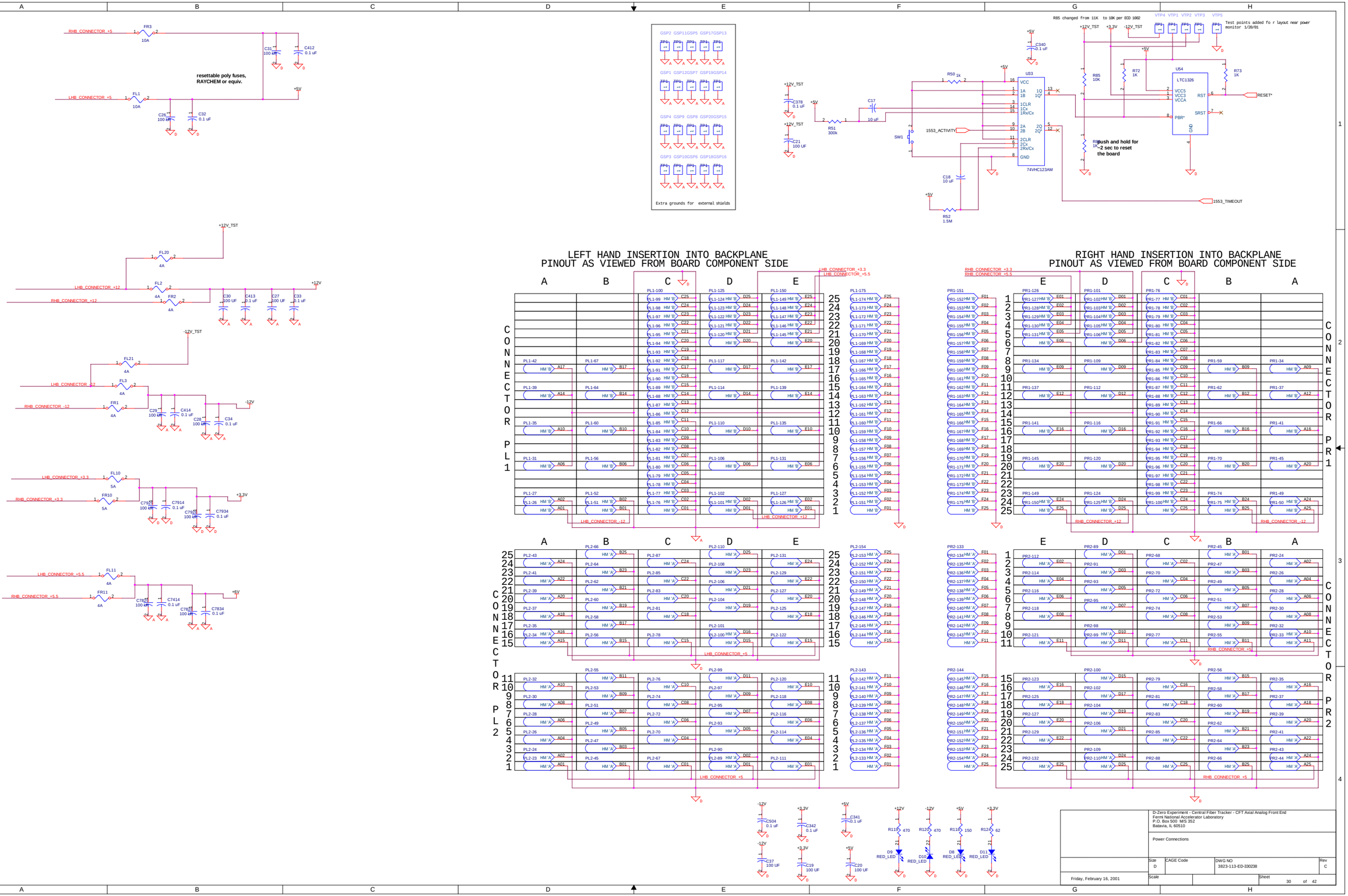

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510

Power Connections

Size	CAGE Code	DWG NO	Rev
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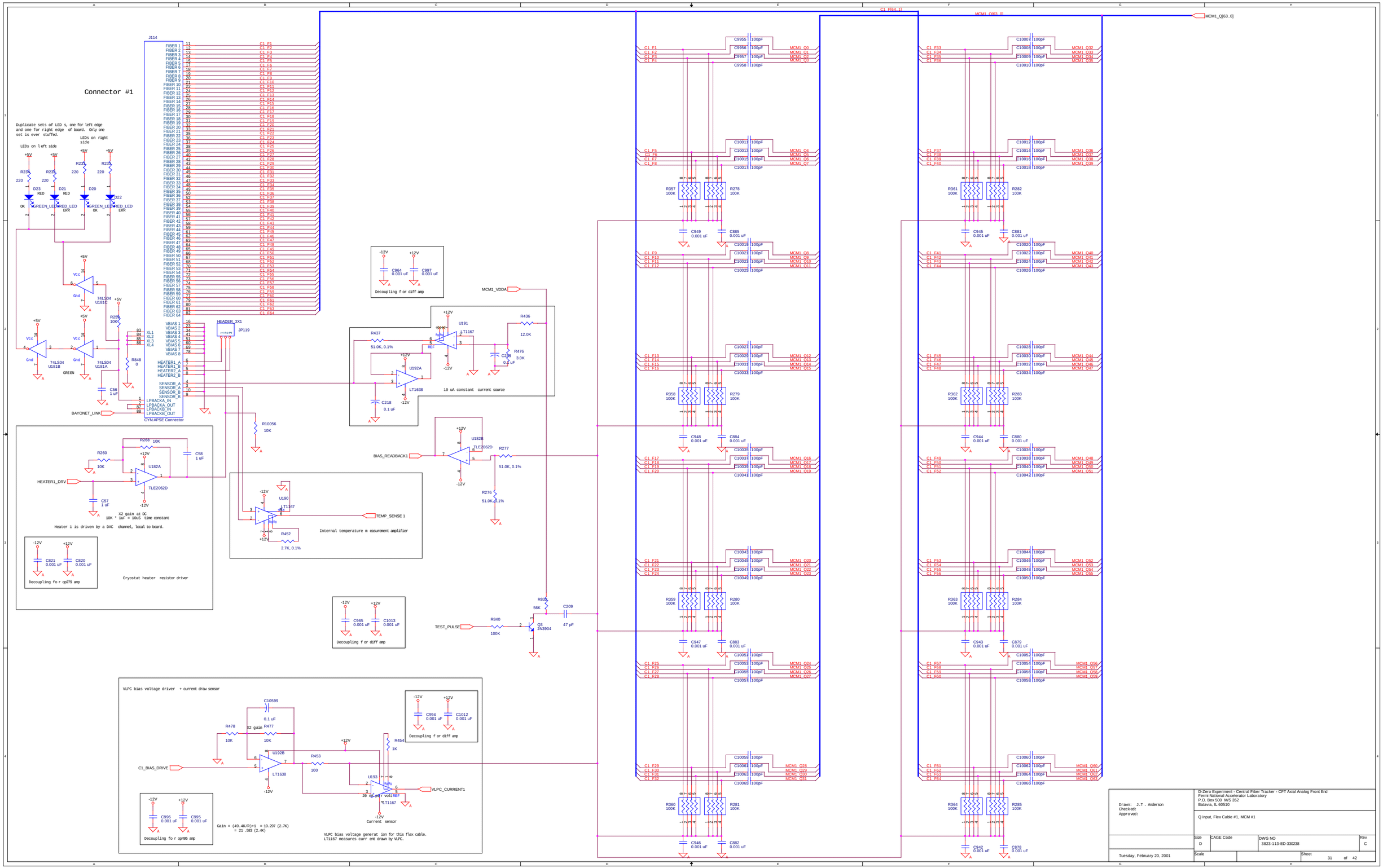
Connector #1
J114
CYNAPSE Connector
Duplicate sets of LED s, one for left edge and one for right edge of board. Only one set is ever stuffed.
LEDs on left side
LEDs on right side
Decoupling f or diff amp
HEADER_3X1
JP119
BAYONET_LINK
HEATER1_DRV
TEMP_SENSE 1
Internal temperature m easurement amplifier
10 uA constant current source
BIAS_READBACK1
MCM1_VDDA
TEST_PULSE
Cryostat heater resistor driver
VLPC bias voltage driver + current draw sensor
C1_BIAS_DRIVE
VLPC_CURRENT1
Current sensor
VLPC bias voltage generat ion for this flex cable.
LT1167 measures curr ent drawn by VLPC.
C1_F64_1
MCM1_Q63_0
MCM1_Q[63..0]
Drawn: J.T. Anderson
Checked:
Approved:
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
Q input, Flex Cable #1, MCM #1
Size D
CAGE Code
DWG NO 3823-113-ED-330238
Rev C
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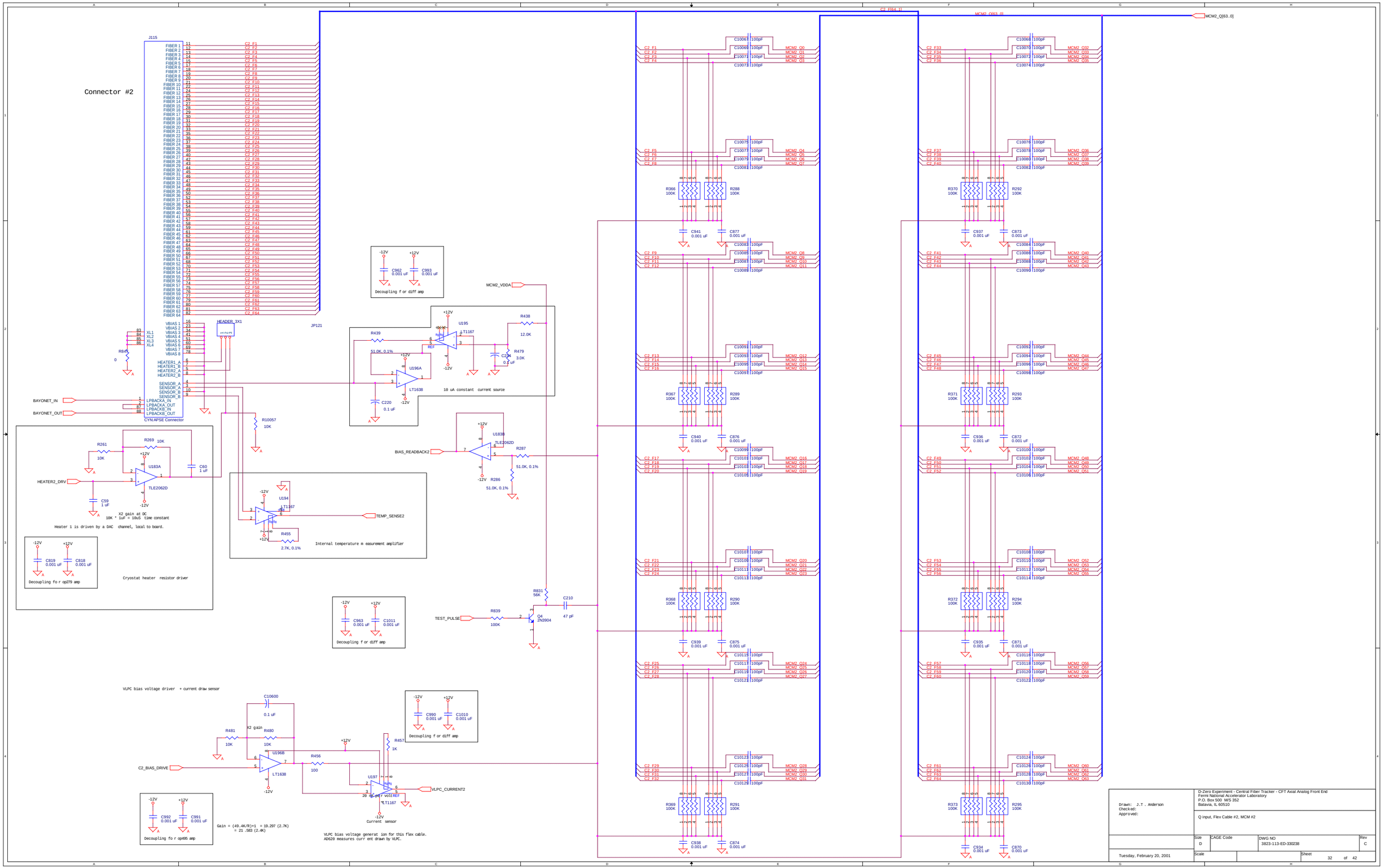
Connector #2
J115
CYNAPSE Connector
JP121
HEADER_3X1
BAYONET_IN
BAYONET_OUT
HEATER2_DRV
Heater 1 is driven by a DAC channel, local to board.
X2 gain at DC
10K * 1uF = 10uS time constant
Cryostat heater resistor driver
Decoupling for op279 amp
Decoupling for diff amp
10 uA constant current source
Internal temperature measurement amplifier
TEMP_SENSE2
BIAS_READBACK2
TEST_PULSE
MCM2_VDDA
C2_F64_1
MCM2_Q63..0
MCM2_Q[63..0]
VLPC bias voltage driver + current draw sensor
C2_BIAS_DRIVE
VLPC_CURRENT2
Current sensor
Gain = (49.4K/R)+1 = 19.297 (2.7K)
= 21.583 (2.4K)
VLPC bias voltage generation for this flex cable.
AD620 measures current drawn by VLPC.
Drawn: J.T. Anderson
Checked:
Approved:
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
Q input, Flex Cable #2, MCM #2
Size D
CAGE Code
DWG NO 3823-113-ED-330238
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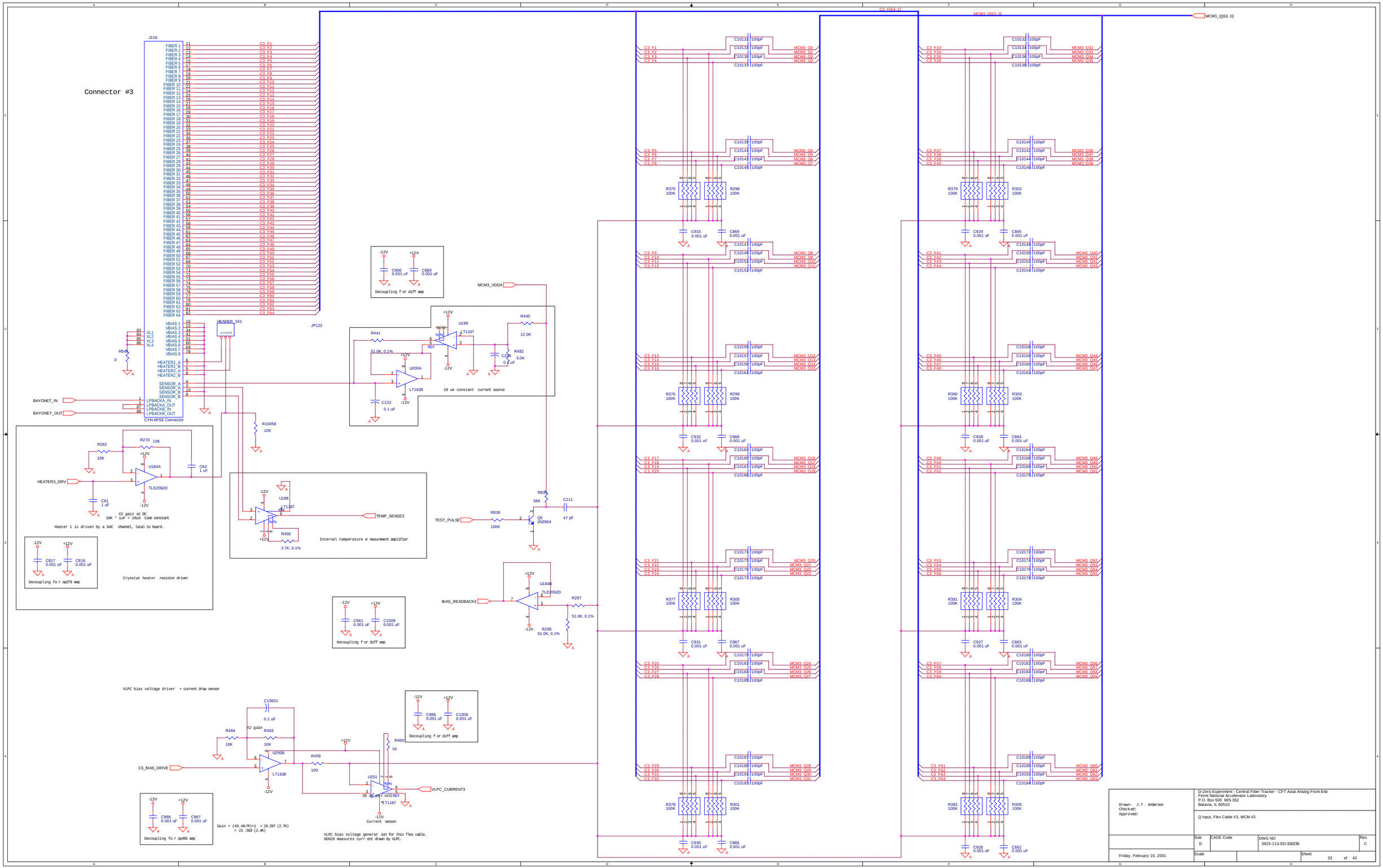
Connector #3
J116
JP123
CYNAPSE Connector
HEADER_3X1
BAYONET_IN
BAYONET_OUT
HEATER3_DRV
TEMP_SENSE3
Internal temperature m easurement amplifier
10 uA constant current source
Decoupling f or diff amp
Cryostat heater resistor driver
Heater 1 is driven by a DAC channel, local to board.
X2 gain at DC
10K * 1uF = 10uS time constant
TEST_PULSE
BIAS_READBACK3
MCM3_VDDA
MCM3_Q[63..0]
VLPC bias voltage driver + current draw sensor
C3_BIAS_DRIVE
VLPC_CURRENT3
Current sensor
VLPC bias voltage generat ion for this flex cable.
AD620 measures curr ent drawn by VLPC.
Gain = (49.4K/R)+1 = 19.297 (2.7K)
= 21 .583 (2.4K)
Drawn: J.T. Anderson
Checked:
Approved:
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 MS 352
Batavia, IL 60510
Q input, Flex Cable #3, MCM #3
Size D
CAGE Code
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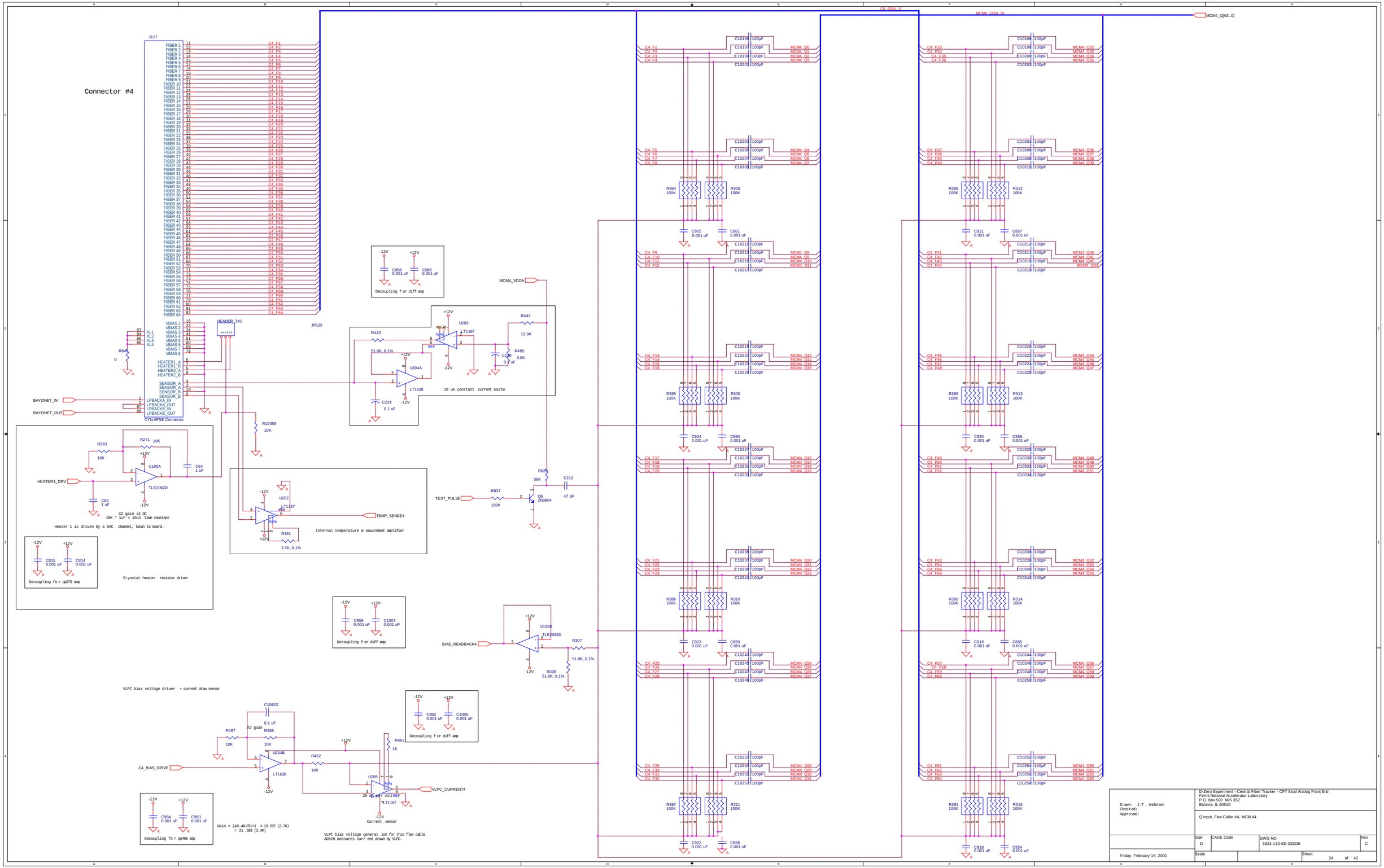

Connector #4
J117
CYNAPSE Connector
JP125
HEADER_3X1
BAYONET_IN
BAYONET_OUT
HEATER4_DRV
TEST_PULSE
BIAS_READBACK4
C4_BIAS_DRIVE
VLPC_CURRENT4
TEMP_SENSE4
MCM4_VDDA
MCM4_Q[63..0]
Decoupling for diff amp
10 uA constant current source
Internal temperature measurement amplifier
Cryostat heater resistor driver
Heater 1 is driven by a DAC channel, local to board.
X2 gain at DC
10K * 1uF = 10uS time constant
Decoupling for op279 amp
VLPC bias voltage driver + current draw sensor
Decoupling for op495 amp
Gain = (49.4K/R)+1 = 19.297 (2.7K)
= 21.583 (2.4K)
VLPC bias voltage generation for this flex cable.
AD620 measures current drawn by VLPC.
Current sensor
Drawn: J.T. Anderson
Checked:
Approved:
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
Q input, Flex Cable #4, MCM #4
Size D
CAGE Code
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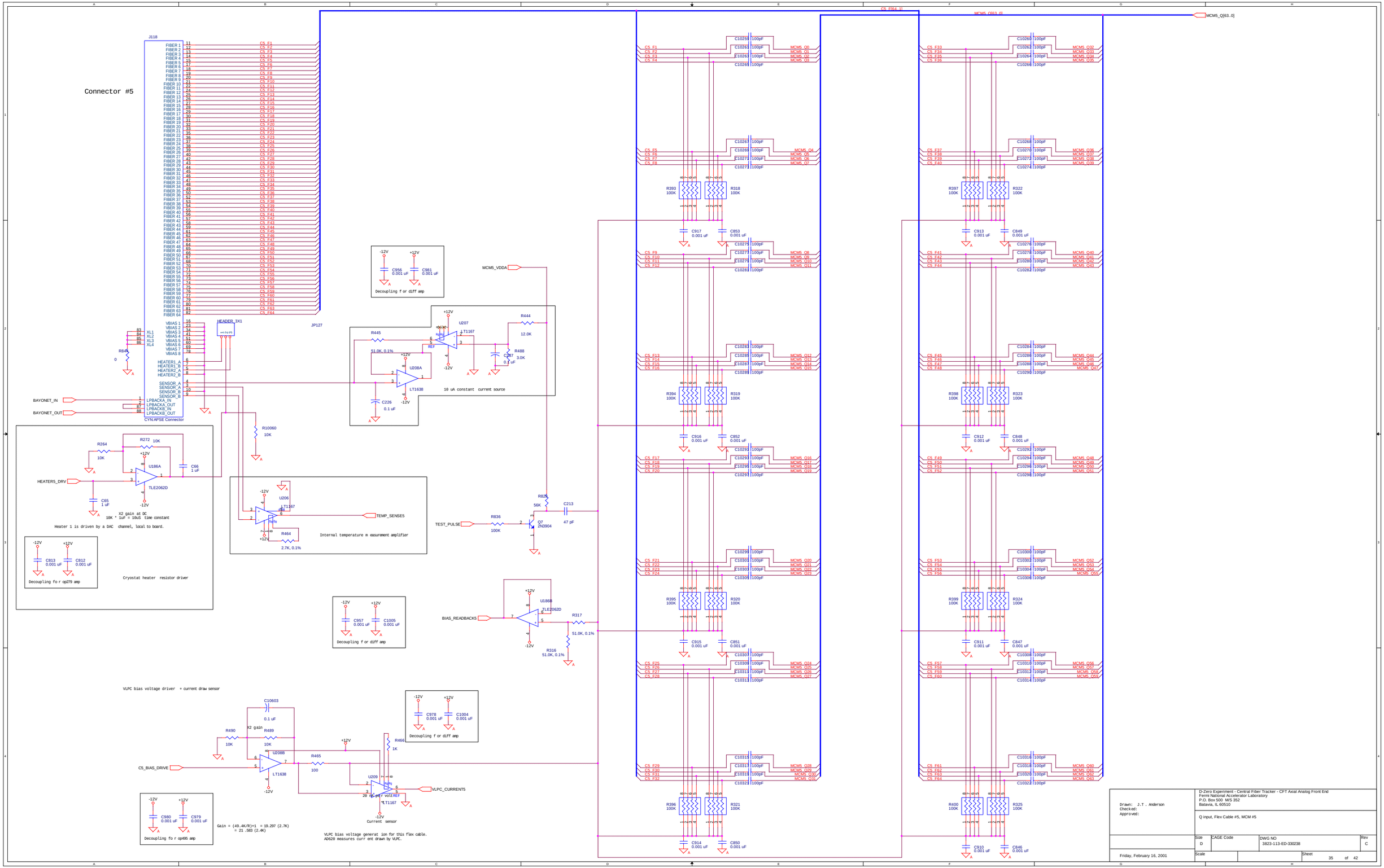
Connector #5
J118
CYNAPSE Connector
JP127
HEADER_3X1
BAYONET_IN
BAYONET_OUT
HEATER5_DRV
TEMP_SENSE5
TEST_PULSE
BIAS_READBACK5
C5_BIAS_DRIVE
VLPC_CURRENT5
MCM5_VDDA
MCM5_Q[63..0]
Decoupling for diff amp
10 uA constant current source
Internal temperature measurement amplifier
Cryostat heater resistor driver
Heater 1 is driven by a DAC channel, local to board.
X2 gain at DC
10K * 1uF = 10uS time constant
Decoupling for op279 amp
Decoupling for diff amp
VLPC bias voltage driver + current draw sensor
Decoupling for op495 amp
Gain = (49.4K/R)+1 = 19.297 (2.7K)
= 21 .583 (2.4K)
VLPC bias voltage generation for this flex cable.
AD620 measures current drawn by VLPC.
Current sensor
Drawn: J.T. Anderson
Checked:
Approved:
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
Q input, Flex Cable #5, MCM #5
Size D
CAGE Code
DWG NO 3823-113-ED-330238
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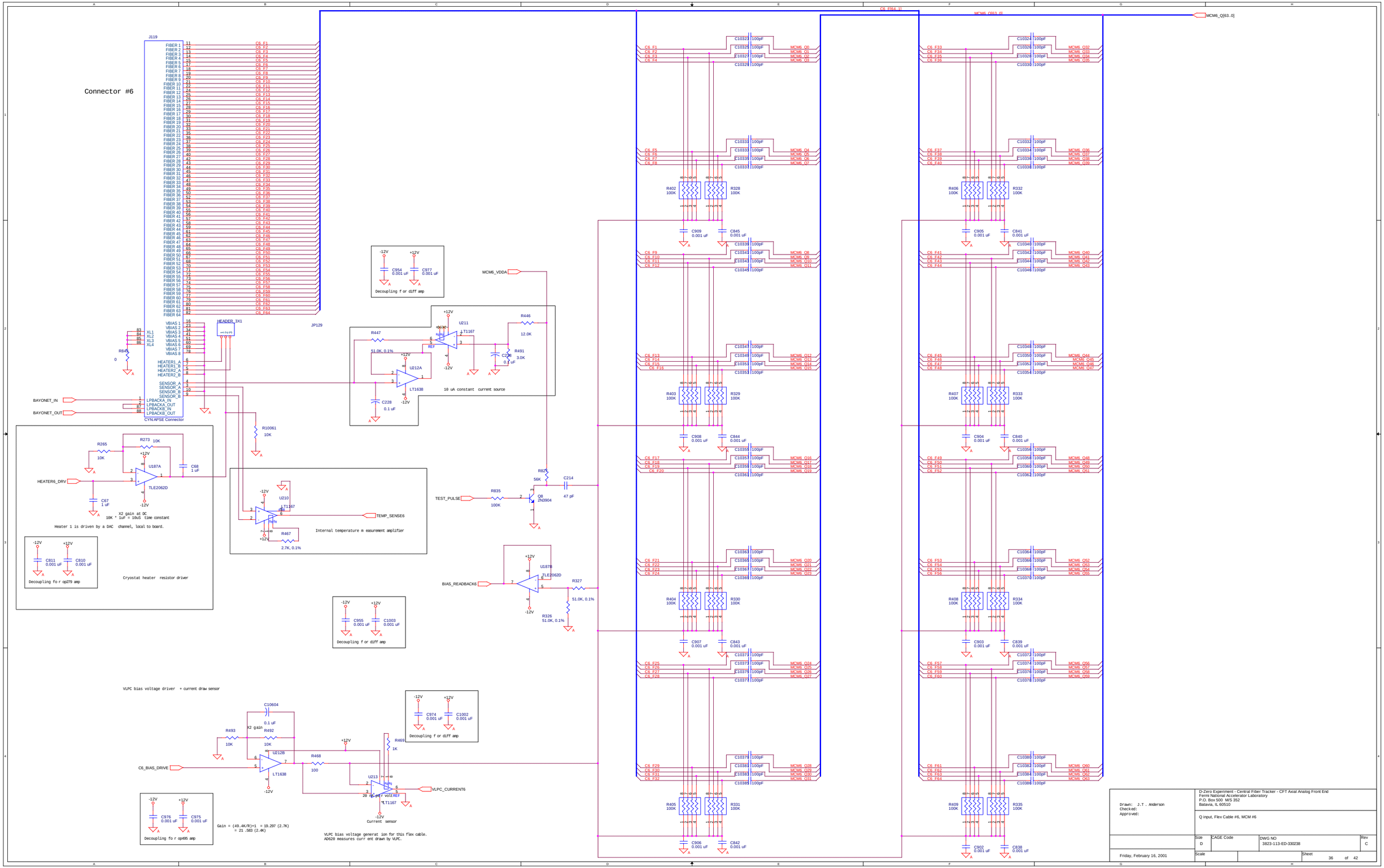
Connector #6
J119
CYNAPSE Connector
JP129
HEADER_3X1
BAYONET_IN
BAYONET_OUT
Decoupling for diff amp
MCM6_VDDA
10 uA constant current source
HEATER6_DRV
X2 gain at DC
10K * 1uF = 10uS time constant
Heater 1 is driven by a DAC channel, local to board.
Decoupling for op279 amp
Cryostat heater resistor driver
TEMP_SENSE6
Internal temperature measurement amplifier
TEST_PULSE
BIAS_READBACK6
Decoupling for diff amp
VLPC bias voltage driver + current draw sensor
C6_BIAS_DRIVE
Decoupling for op495 amp
Gain = (49.4K/R)+1 = 19.297 (2.7K)
= 21.583 (2.4K)
VLPC_CURRENT6
Current sensor
VLPC bias voltage generation for this flex cable.
AD620 measures current drawn by VLPC.
MCM6_Q[63..0]
Drawn: J.T. Anderson
Checked:
Approved:
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
Q input, Flex Cable #6, MCM #6
Size D
CAGE Code
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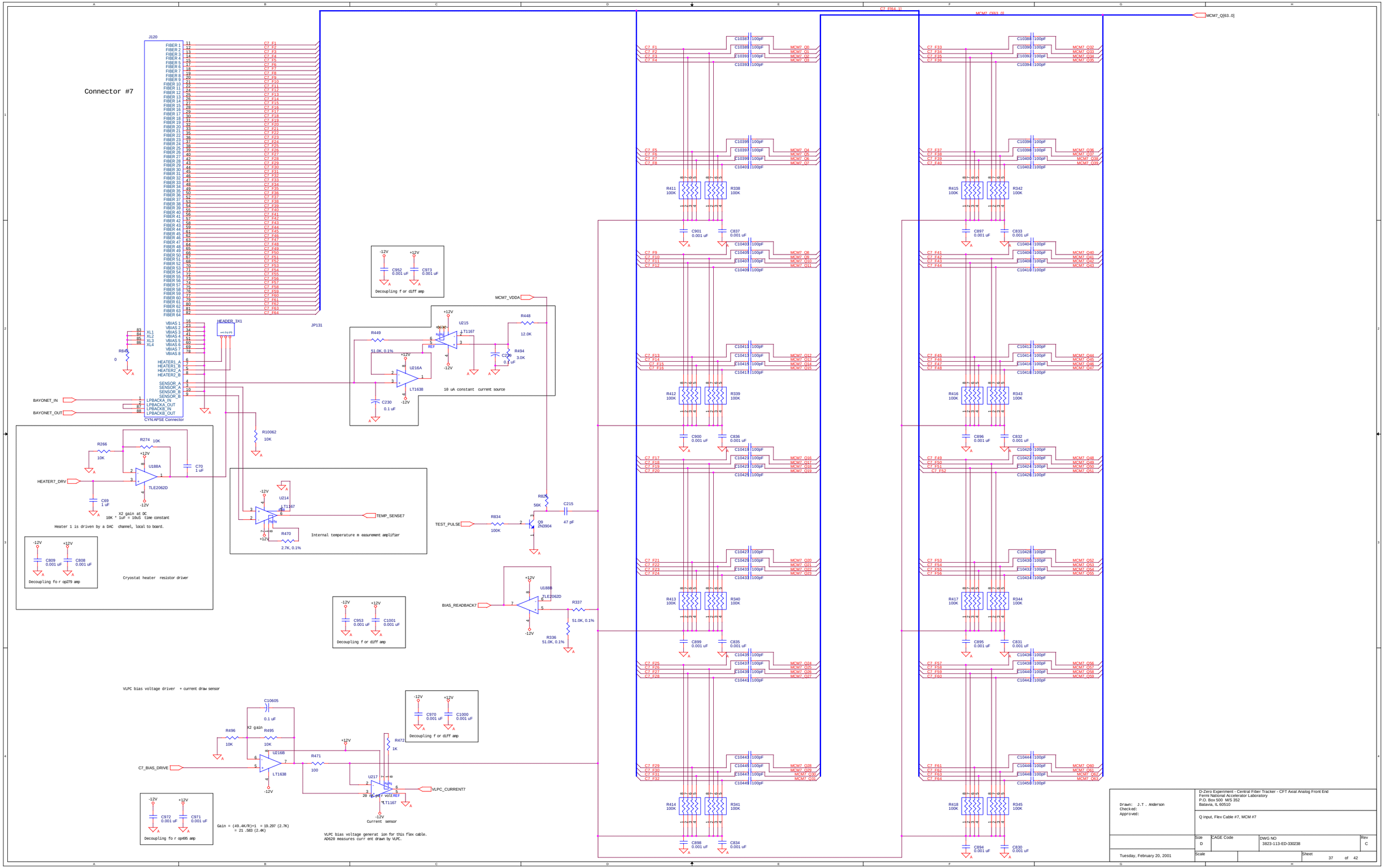
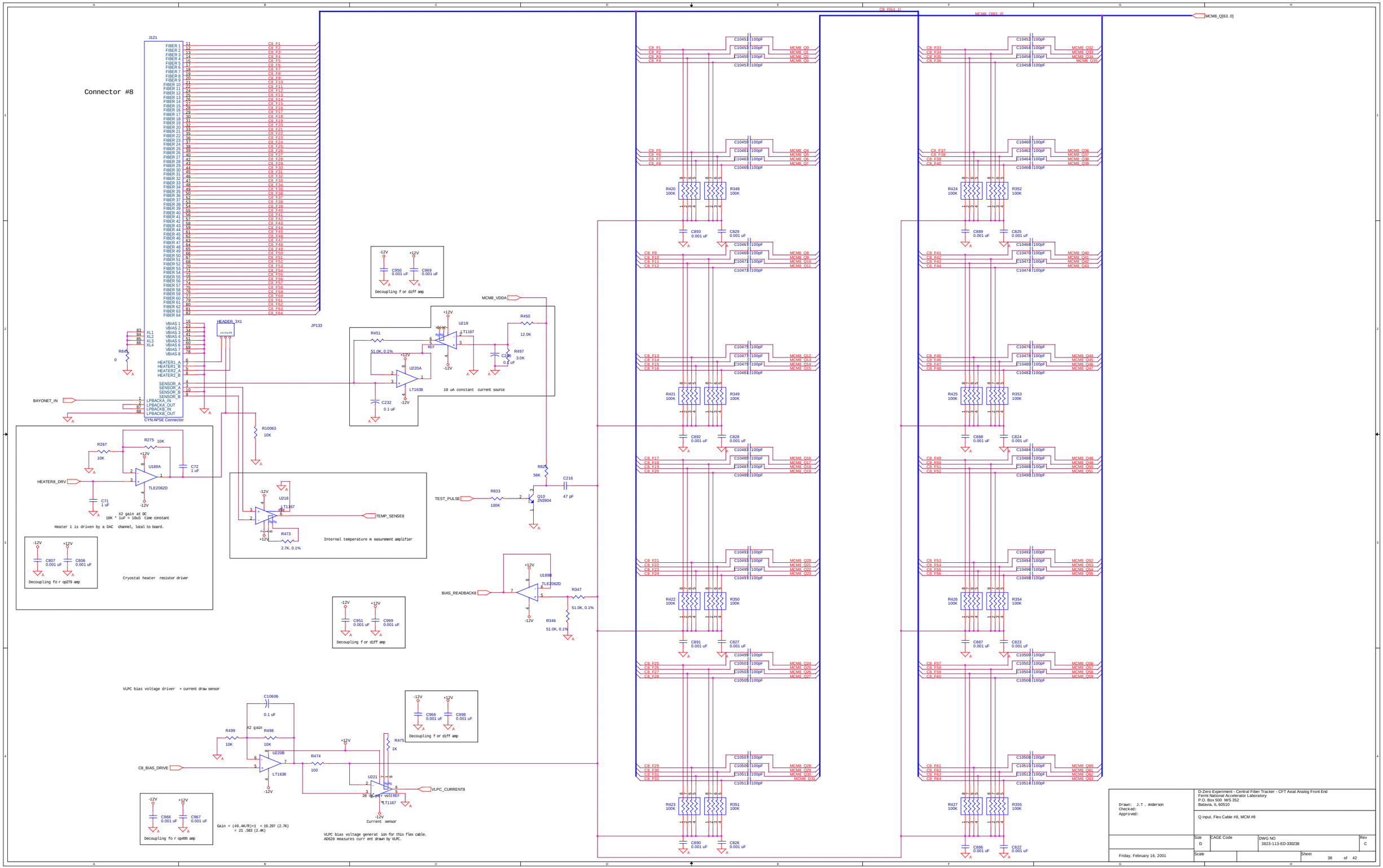
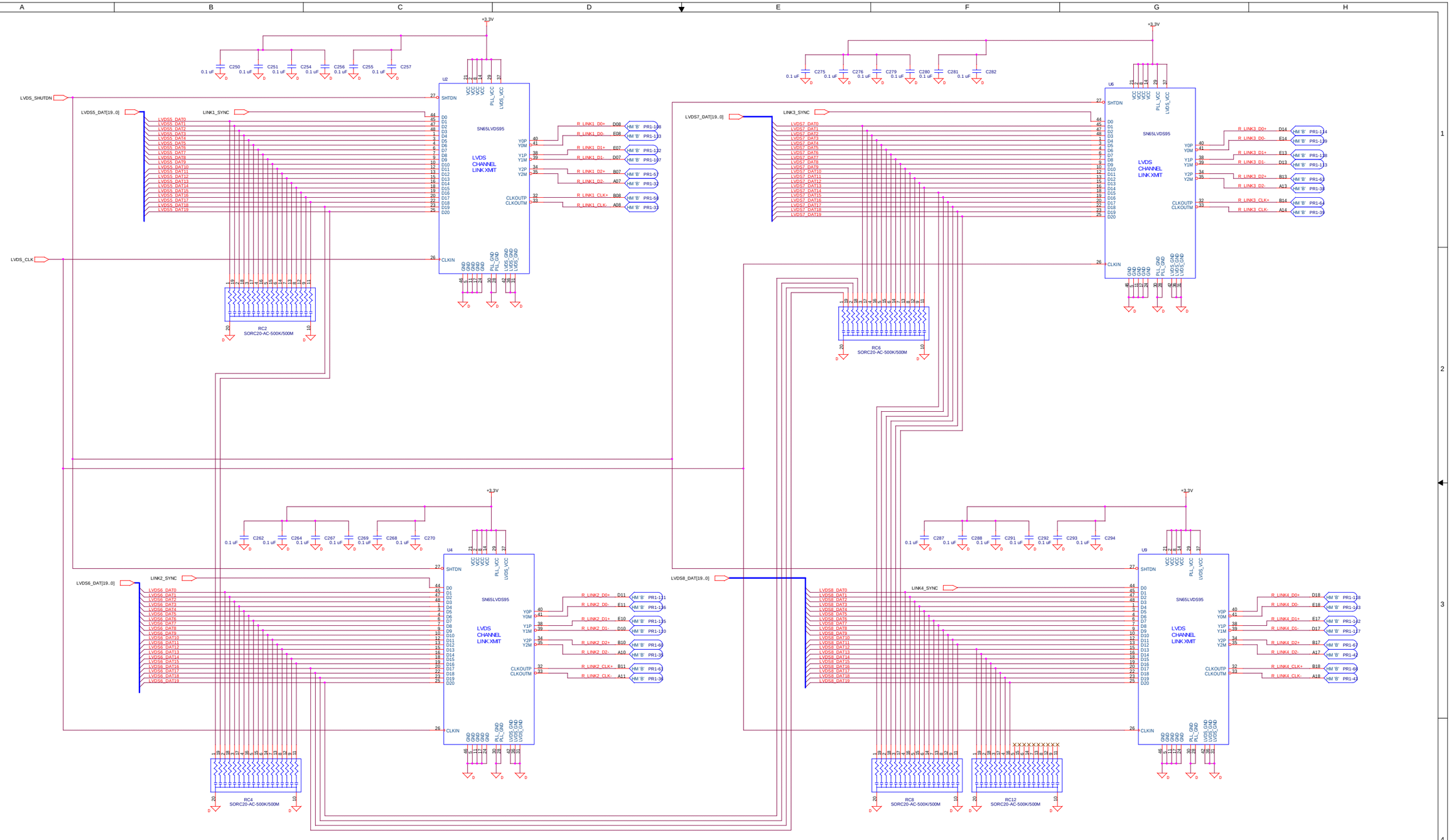

Connector #7
J120
CYNAPSE Connector
JP131
HEADER_3X1
BAYONET_IN
BAYONET_OUT
HEATER7_DRV
R266 10K
R274 10K
U188A
TLE2062D
C70 1 uF
C69 1 uF
X2 gain at DC
10K * 1uF = 10uS time constant
Heater 1 is driven by a DAC channel, local to board.
Decoupling for op279 amp
C809 0.001 uF
C808 0.001 uF
Cryostat heater resistor driver
R10062 10K
Decoupling for diff amp
C952 0.001 uF
C973 0.001 uF
MCM7_VDDA
R449 51.0K, 0.1%
U215 LT1167
R448 12.0K
R494 3.0K
C229 0.1 uF
U216A LT1638
C230 0.1 uF
10 uA constant current source
U214 LT1167
TEMP_SENSE7
R470 2.7K, 0.1%
Internal temperature measurement amplifier
TEST_PULSE
R834 100K
R82 56K
C215 47 pF
Q9 2N3904
BIAS_READBACK7
U188B TLE2062D
R337 51.0K, 0.1%
R336 51.0K, 0.1%
C953 0.001 uF
C1001 0.001 uF
VLPC bias voltage driver + current draw sensor
C10605 0.1 uF
R496 10K
R495 10K
X2 gain
U216B LT1638
C7_BIAS_DRIVE
R471 100
R472 1K
U217 LT1167
VLPC_CURRENT7
Current sensor
C970 0.001 uF
C1000 0.001 uF
C972 0.001 uF
C971 0.001 uF
Gain = (49.4K/R)+1 = 19.297 (2.7K)
= 21 .583 (2.4K)
VLPC bias voltage generator for this flex cable.
AD620 measures current drawn by VLPC.
C7_F64_1
MCM7_Q63_0
MCM7_Q[63..0]
R411 100K
R338 100K
R412 100K
R339 100K
R413 100K
R340 100K
R414 100K
R341 100K
R415 100K
R342 100K
R416 100K
R343 100K
R417 100K
R344 100K
R418 100K
R345 100K
Drawn: J.T. Anderson
Checked:
Approved:
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
Q input, Flex Cable #7, MCM #7
Size D
CAGE Code
DWG NO 3823-113-ED-330238
Rev C
Tuesday, February 20, 2001
Scale
Sheet 37 of 42


Connector #8
J121
CYNAPSE Connector
JP133
HEADER_3X1
BAYONET_IN
HEATER8_DRV
TEST_PULSE
BIAS_READBACK8
C8_BIAS_DRIVE
TEMP_SENSE8
VLPC_CURRENT8
MCM8_VDDA
MCM8_Q[63..0]
C8_F64..1
MCM8_Q63..0
Decoupling f or diff amp
10 uA constant current source
Internal temperature m easurement amplifier
Heater 1 is driven by a DAC channel, local to board.
X2 gain at DC
10K * 1uF = 10uS time constant
Cryostat heater resistor driver
VLPC bias voltage driver + current draw sensor
Gain = (49.4K/R)+1 = 19.297 (2.7K)
= 21 .583 (2.4K)
VLPC bias voltage generat ion for this flex cable.
AD620 measures curr ent drawn by VLPC.
Current sensor
Drawn: J.T. Anderson
Checked:
Approved:
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 MS 352
Batavia, IL 60510
Q input, Flex Cable #8, MCM #8
Size D
CAGE Code
DWG NO 3823-113-ED-330238
Rev C
Friday, February 16, 2001
Scale
Sheet 38 of 42



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Fermi National Accelerator Laboratory
P.O. Box 500 MS 352
Batavia, IL 60510
<OrgAddr>

LVDS Driver, Right-Handed Insertion

Size	CAGE Code	DWG NO	Rev
D	<Cage Code>	3823-113-ED-330238	C

Friday, February 16, 2001

Scale

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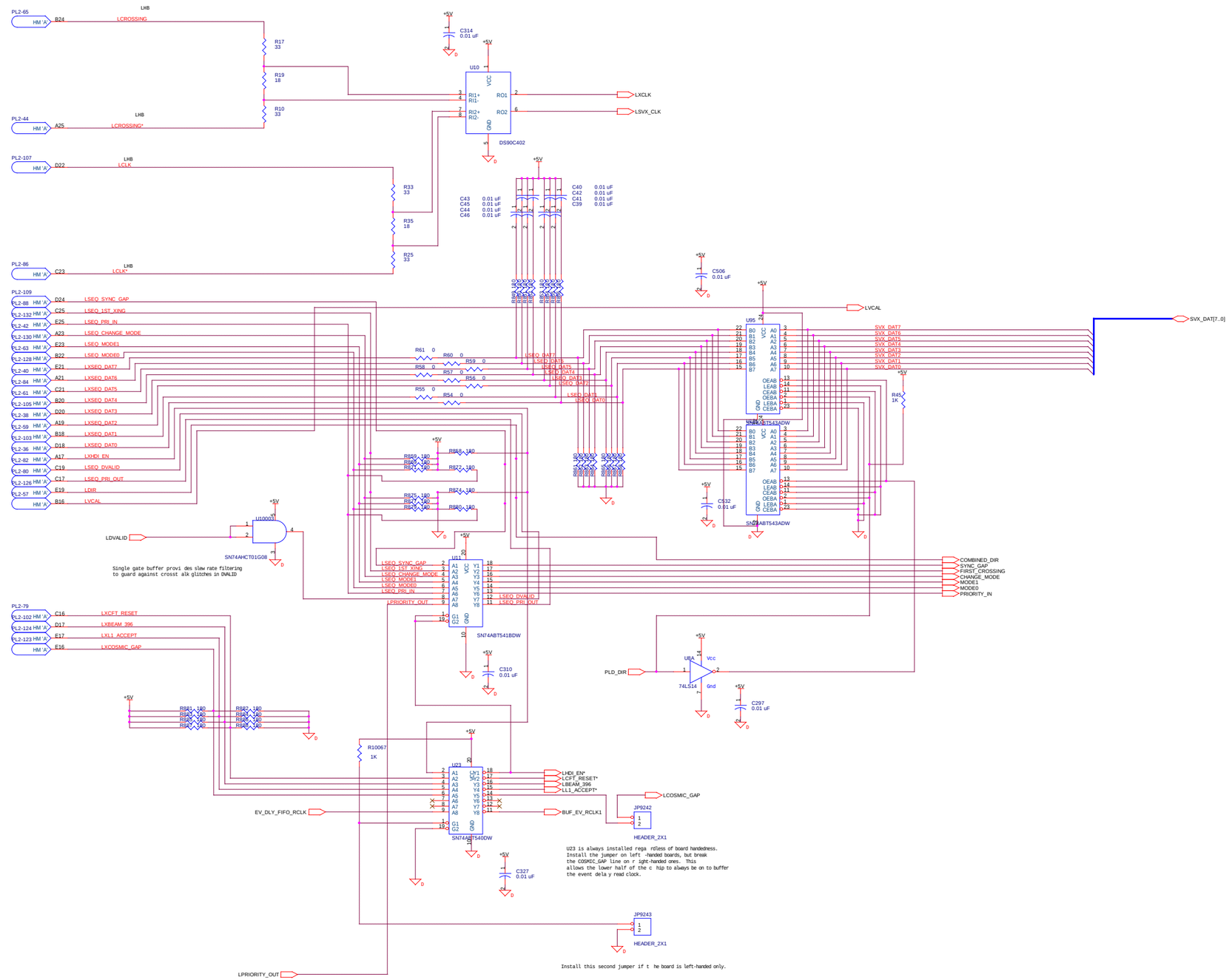

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P.O. Box 500 MS 352
Batavia, IL 60510

SVX Sequencer Connector - Left Handed Insertion

Size	CAGE Code	DWG NO	Rev
D		3823-113-ED-330238	C

Tuesday, February 20, 2001

Scale

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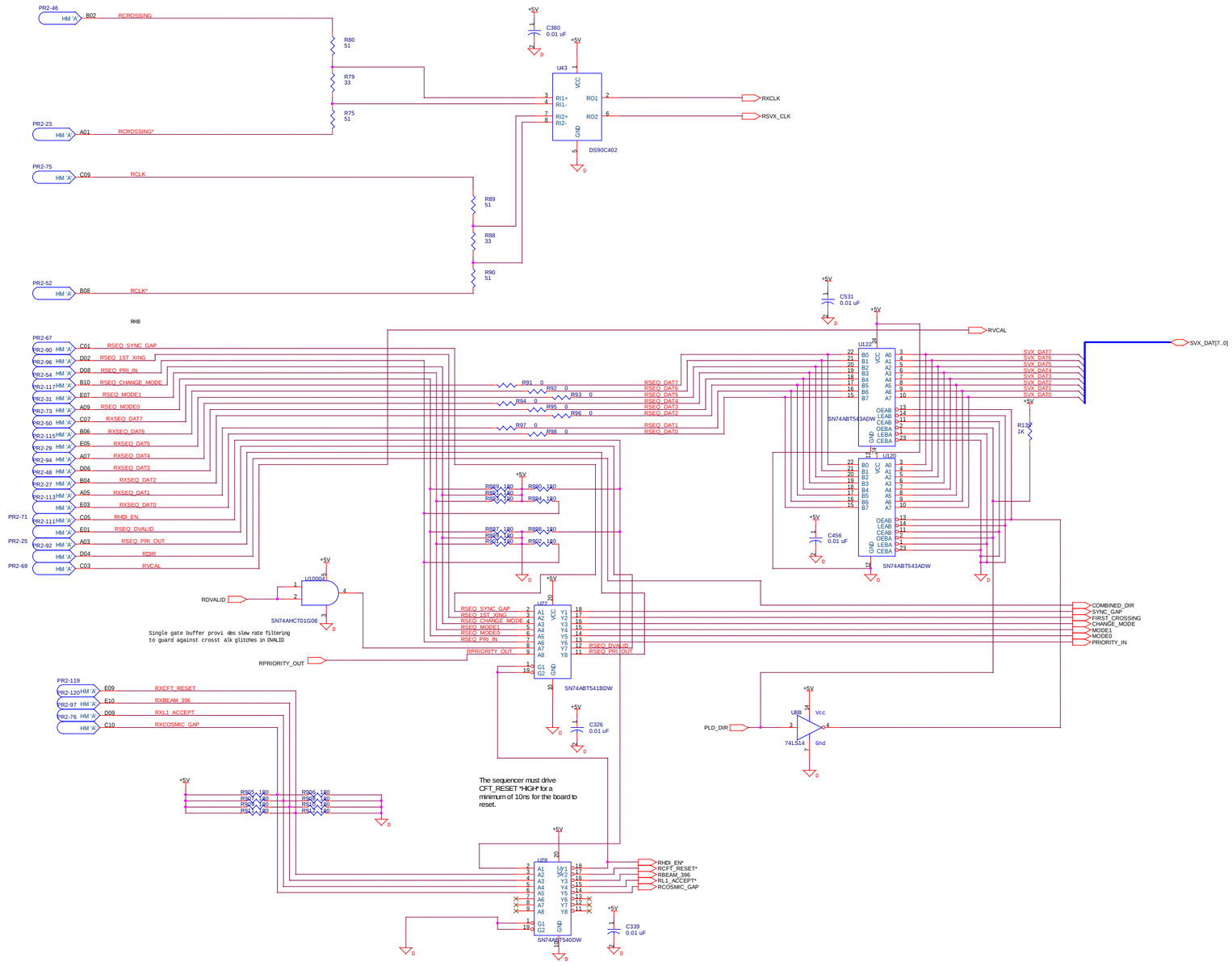

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510

SVX Sequencer Connector - Right-Handed Insertion

Size	CAGE Code	DWG NO	Rev
D		3823-113-ED-330238	C

Wednesday, February 21, 2001

Scale

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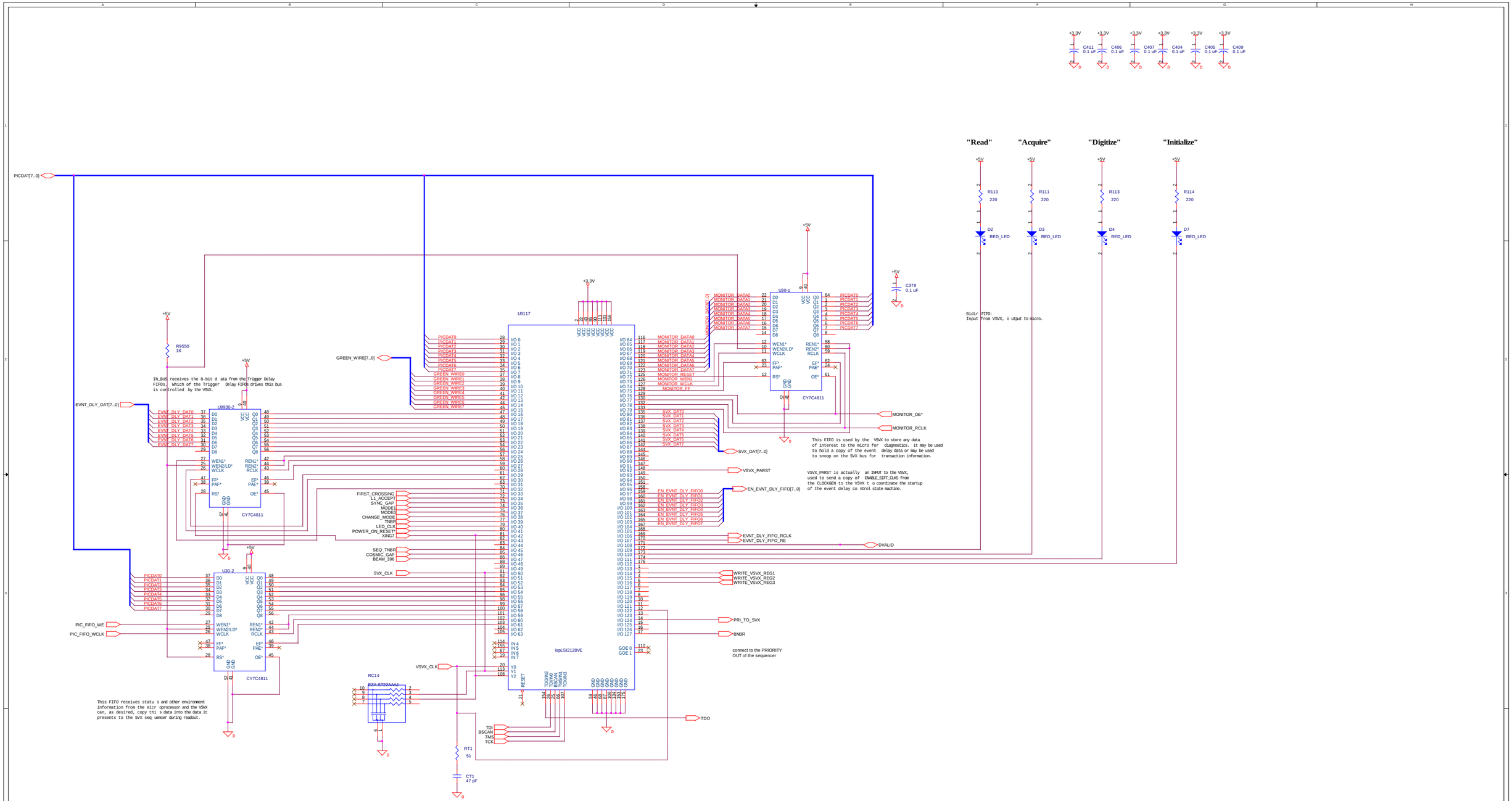

Drawn: Jamie son T. Olsen Checked: Approved:	D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End Fermi National Accelerator Laboratory P.O. Box 500 MS 352 Batavia, IL 60510		
	Virtual SVX		
	Size D	CAGE Code	DWG NO 3823-113-ED-330238	Rev C
Thursday, February 15, 2001	Scale		Sheet 42 of 42