Hybrid testing

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- Summary of discussion at KSU
  - Hybrids need to be tested as thoroughly as possible before burn-in
    - Chips will be wafer tested but
      - Dicing yield
      - Collective effects
    - Simple things (spreadsheet level)
      - Full parameter space scan
      - Pipeline cell scan
  - Voltage scans
    - VDD scan with Purple Card
    - KU and Fermilab will do R&D to define specs
  - Timing scans
    - KSU and Fermilab will do R&D to define specs
    - DV phase with Purple Card, 2 ns steps
    - Phase of CLK and /CLK
    - <u>Duty cycle of clock</u>
  - Full chain test – partly addresses timing issues above
    - Different length cables : 80-conductor, twisted pair, jumper
    - Main reason why duty cycle is different for different channels
    - Different firmware