



Fermi National Accelerator Laboratory

D0 Silicon Strip Detector Upgrade Project

SVX SEQUENCER BOARD

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1 INTRODUCTION

The SVX Sequencer boards are 9U by 280mm circuit boards that reside in slots 2 through 21 of each of eight Eurocard crates in the D0 Detector Platform. The basic purpose is to control the SVX chips for data acquisition and when a trigger occurs, to gather the SVX data and relay the data to the VRB boards in the Movable Counting House. Functions and features are as follows:

- Initialization of eight SVX chip strings using the MIL-STD-1553 data bus.
- Real time manipulation of the SVX control lines to effect data acquisition, digitization, and readout based on the NRZ/Clock signals from the Controller.
- Conversion of 8-bit electrical SVX readout data to an optical signal operating at 1.062 Gbit/sec, sent to the VRB. Eight HDIs will be serviced per board.
- Built-in logic analyzer which can record the most important control and data lines during a data acquisition cycle and put this recorded information onto the 1553 bus.
- Identification header and end of data trailer tacked onto data stream.
- 1553 register which can read the current values of the control and data lines.
- 1553 register which can test the optical link.
- 1553 registers for crossing pulse width, calibration pulse voltage, and calibration pipeline select.
- 1553 register for reading the optical drivers' status link.
- 1553 register for power control of SVX chips and ignoring bad SVX strings.
- Front panel displays and LEDs show the board status at a glance.
- In-system programmable EPLDs are programmed via 1553 or Altera's "Bitblaster"
- Automatic readout abort after 45us
- Supplies BUSY signal back to Trigger Framework
- Supports a heartbeat system to prevent excessive SVX current draw
- Supports a SVX power trip feature if heartbeat failure occurs

2 I/O CONFIGURATION

2.1 General Crate Configuration

The boards will reside in eight centrally-located crates in the detector platform. These are 9U by 320mm Eurocard crates with a board separation of 0.8". There are 21 slots. Maximum Sequencer cards per crate is projected to be eighteen. Slot one in each crate will house a "Sequencer Controller" card that receives the Serial Command Link. This card interprets the link and distributes control signals across the Sequencer J1 backplane to each of the Sequencer Boards.

The J2/J3 backplanes provide the connection to 3M cables that go to the SVX chips. The cables carry control and bus signals and connect to a "Transition board," where the SVX power also connects. From there a flex-circuit cable will carry the control, bus and power to the HDIs on which three to nine chips are mounted.

Two 1553 cables will connect to the J1 backplane, as will the crate power. Four fibers are routed out the front panel of each Sequencer.

Each of slots 2 through 21 will have five bits of geographic addressing labeled 1 through 20 respectively.

2.2 Control Signals from the Sequencer Controller

The Sequencer Controller is a circuit board residing in slot 1 of the Sequencer crate. It transforms Serial Command Link (SCL) signals into pairs of Sequencer control signals (NRZ & Clock). Each sequencer receives, across the backplane, its own pair of signals with adjusted timing. The signals tell the Sequencer the proper times to reset the SVX preamps, trigger, digitize, and read out SVX data.

NRZ stands for Non-Return to Zero and is a basic data transmission protocol whereby a high represents a logic 1 and a low represents a logic 0. The Clock line simply acts as a strobe for NRZ. In our control link, NRZ consists of a continuous stream of seven-bit packets, each bit being the same duration as one Tevatron RF cycle. The packets are synchronized with the accelerator. The bits in each packet consist of one framing bit which is always high, a bit which is high if a beam crossing is imminent, four bits representing the command desired, and one parity bit (odd parity). If the controller detects that a framing bit is zero, a NoSynch indication will occur, readable via 1553 or front panel LED. Synch is automatically re-established by sending only the framing bit for three cycles. This also happens to be the Idle command. The four command bits are defined in Table 1.

Idle	0 0 0 0
Acquire	0 0 0 1
Trigger	0 0 1 1
Ramp	1 0 1 0
Digitize	0 0 1 0
Readout	0 1 1 0
Reset_Preamp	0 1 0 1
Cal_Inject	0 1 1 1
Extract Pipeline Charge	1 0 1 1
Reserved_9	1 0 0 1
Readout Abort	0 1 0 0
Turn off SVX Power	1 1 0 0
PRD2	1 0 0 0
G_Link Lock Sequence	1 1 1 1
SVX2 Preamp Reset	1 1 0 1
Reserved_E	1 1 1 0

Table 1. Command codes encoded in NRZ

2.3 Interface to the SVX Chips

The J2/J3 backplane accepts the Futurebus-style connectors from the Sequencer. Four such 4 by 18 connectors exist on each Sequencer; each connector carries the signals for two HDIs. The backplane routes these signals to connectors on the rear of the backplane that accept the 3M cables that go to the Transition boards. Four such cables are associated with each Sequencer board. The bidirectional bus signals use TI 74ABT162500 transceiver chips to drive the 82Ω cable. Other control signals use TTL drivers. A direction line is routed to the Transition board to control the transceivers on that board. Another signal called HDI-EN is sent to the Transition board to tell it to turn power on to the SVX chips.

2.4 Data Readout to the VRB

During readout of the SVX chips, the eight data bits from each of two HDIs is strobed into FIFO memories, and almost immediately read out into a Hewlett-Packard G-Link transmitter chip. These sixteen bits, each changing at 53Mb/s, are serialized by the G-Link and the resultant 1.062Gb/s serial signal is fed into a Finisar Laser optical driver. A 160 ft. fiber carries this signal out the front panel and to the VRBs in the MCH. Four such links emerge from each sequencer; each VRB accepts four fiber links. The data stream recovered by the VRB consists of eight bit words in succession. The data for each HDI is as follows:

```

Sequencer ID
HDI # & Status
Chip ID
Byte of zeroes
Channel ID
Data
Channel ID
Data
...and so on
hex "C0C0" (for end marker)

```

To distinguish between Chip ID and Channel ID the MSB is set to "1" in the Chip ID and it is set to "0" in the Channel ID. This is a feature of the SVX chip.

2.4.1 Header in Data Readout to the VRB

The Sequencer ID is a number from 0 to 255; there will be about 150 total sequencers in the detector. The next byte is defined, starting with the MSB, as follows:

Downloaded status bit 2
Downloaded status bit 1
Downloaded status bit 0
Control Link No_Synch
Control Link Parity Error
HDI # bit 2
HDI # bit 1
HDI # bit 0

The Downloaded status bits are provided for general use and are set via 1553. As of Summer 2002, these three bits are being used in some crates to provide a check for the SCL L1 BX Number that the VRB Controller provides in the event data. It does this by resetting a three bit counter every Sync gap, and the counter value is sent to these three bits. Its success depends on the fact that there is a constant delay from L1 Accept to the beginning of Readout mode, when the bits are presented to the header.

The No_Synch and Par_Err bits are reset to zero shortly after the data header is sent to the VRB. If a constant or momentary fault condition occurs after this time, the appropriate bit will be set to one and latched for readout during the next event readout.

The three HDI # bits are numbered 0 - 7 and are associated with the cables connecting to the HDI Interface Modules as follows:

0	A half of top cable (wrt Sequencer backplane)
1	B half of top cable
2	A half of second cable
3	B half of second cable
4	A half of third cable
5	B half of third cable
6	A half of bottom cable
7	B half of bottom cable

2.4.2 Trailer in Data Readout to the VRB

The Trailer for each HDI data stream will be hex C0C0 and will be appended to the data immediately following the last data byte of the last chip on its HDI. This trailer will appear in what would be the next Chip ID field (if the HDI had one extra chip), so there should be no SVX chips assigned a chip ID of C0. The forced readout of channel 127 of the last chip on each HDI (a feature of the SVX2E chip) will not be used; the option to use this feature, however, still exists.

2.5 1553

The J1 backplane has two pairs of triaxial bulkheads, each connected to a separate 1553 Controller output. One pair of bulkheads connects to slots 2 through 11; the other connects to slots 12 through 21. Each Sequencer has two identical circuits operated as its own Remote Terminal (RT). Thus there are 20 RTs connected to each 1553 Controller. The various registers in the Sequencer are accessed by reading/writing to a different subaddress. Subaddressing of each RT is defined in the table in Section 5.

3 GENERAL CONTROL CIRCUITRY

3.1 Main Control

The NRZ Control Link is the main input to the Control EPLD (Altera 7192S). The EPLD manipulates the SVX bus lines, Mode lines, and TNBR in the appropriate fashion based on the commands received over the Control link.

The SVX chips can be initialized when the Sequencer Controller is sending the Idle command. Data taking commences when the Acquire code is sent. Occasional Preamp Reset codes, most likely once every Tevatron revolution, will keep the preamps from saturating. When a trigger occurs, the Trigger code is sent which causes the Sequencer to effect digitization in the SVX chips. After a predetermined delay, the Sequencer Controller sends the Readout code, and the chips are instructed to read out the data.

3.2 Control/Status Registers

Two identical EPLDs perform some general utility functions, one for each half of the Sequencer. This utility EPLD operates the Sequencer's Status Register 1 (subaddress 9). The bits are defined in Table 2 and Table 3.

<u>Bit</u>	<u>Function</u>	
0	Bit appears in Status Word at beginning of readout LSB	R/W
1	Bit appears in Status Word at beginning of readout	R/W
2	Bit appears in Status Word at beginning of readout MSB	R/W
3	High if a Parity Error has occurred in the Control Link	RO
4	High if the Control Link had lost synch.	RO
5	Reserved	
6	Reset the Logic Analyzer FIFO	
7	Software reset	WO
8	HDI select for diagnostics LSB	R/W
9	HDI select for diagnostics MSB	R/W
10	Select Seq. half to hex displays	R/W
11	Logic Analyzer FIFO Trigger LSB	R/W
12	Logic Analyzer FIFO Trigger	R/W
13	Logic Analyzer FIFO Trigger MSB	R/W
14	Bit set high when loading FIFO "Almost Full" offsets	R/W
15	Reserved	

Table 2.1 Control/Status Register # 1 bits (Subaddress 9)

<u>Bit</u>	<u>Function</u>	
0	Pulse Shadow Register for HDI 0	WO
1	Pulse Shadow Register for HDI 1	WO
2	Pulse Shadow Register for HDI 2	WO
3	Pulse Shadow Register for HDI 3	WO
4	SVX Power Trip command received/ Reset	R/W
5	Send data pattern into G-Link	WO
6	Re-synchronize G-Link	WO
7-15	Unused	

Table 2.2 Control/Status Register # 2 bits (Subaddress 10)

<u>Bit</u>	<u>Function</u>	
0	Enable Power for HDI 0	R/W
1	Enable Power for HDI 1	R/W
2	Enable Power for HDI 2	R/W
3	Enable Power for HDI 3	R/W
4	Ignore HDI 0	R/W
5	Ignore HDI 1	R/W
6	Ignore HDI 2	R/W
7	Ignore HDI 3	R/W

Table 2.3 Control/Status Register # 3 bits (Subaddress 11)

<u>Bit 13</u>	<u>Bit 12</u>	<u>Bit 11</u>	<u>Logic Analyzer Trigger</u>
0	0	0	Cal or Trig Codes
0	0	1	Cal
0	1	0	Trig
0	1	1	Readout
1	0	0	Nosynch
1	0	1	Parity Error
1	1	0	Acquire
1	1	1	Reserved

Table 3. Logic Analyzer Trigger encoding in the Status Word.

4 DIAGNOSTICS

4.1 Snapshot Register

Since the Sequencer boards will be in the platform and therefore in an interlocked enclosure, remote diagnostics are necessary to isolate the cause and location of a malfunction. If the board freezes and no control is possible, reading subaddress 12 will give the current status of the bus lines, Mode 0 and Mode 1, TNBR, Nosynch, and the four BNBR lines. This is called the “Snapshot” register. Bits 8 and 9 of Status Register 1 choose which of the four HDIs will appear for the Bus lines. Table 4 shows the bit arrangement.

<u>Bit</u>	<u>Signal</u>
0-7	Bus 0-7
8	TNBR
9	Mode 1
10	Mode 0
11	NoSynch
12	BNBR1
13	BNBR2
14	BNBR3
15	BNBR4

Table 4. Bit assignment for diagnostic registers.

4.2 “Logic Analyzer” Register

Another feature is a built-in logic analyzer which records the same bits (except Parity Error replaces TNBR) as the Snapshot register, except that a 4096-deep record of a previous event is stored, strobed at the main clock frequency of 53MHz. Triggering of this logic analyzer is selectable by writing to Status register 1. See Tables 2.1 and 3. The trigger selects which event starts the recording of the signals in the logic analyzer FIFO. Selecting ACQ would show most of the data acquisition cycle. The FIFO can prepare to retrigger upon receiving CSR1 bit 6 (or a general board reset, bit 7). Selecting NoSynch or ParErr as a trigger, in contrast, causes continual writing to the FIFO until a loss of NRZ synch or parity error occur. The FIFO will record the last 4096 clocks before the error has occurred, and will not retrigger until either the FIFO has been read or a software reset is given. The logic analyzer is read out by reading Subaddress 13 4096 times.

4.3 G-Link Test Data Pattern

When bit D14 of subaddress 9 is low, then 64 a test pattern of words may be written into the data FIFOs via subaddresses 14 and 15. To send this data pattern through the G-Link to the VRB, simply write a 1 into bit D5 of subaddress 10. This bit need not then be written low.

4.4 Fiber Driver Status Link

The Finisar optical fiber drivers have a serial status link to view parameters such as temperature and optical power output. All four drivers are connected into this one status link viewable by communicating with subaddress 18. The bit definitions are in table 5.

<u>Bit</u>	<u>Signal</u>
0	Serial bit into optical driver
1	Serial bit from optical driver
2	SCLK enable bit
3	READY bit from optical driver
4	CS to top optical driver
5	CS to second optical driver
6	CS to third optical driver
7	CS to bottom optical driver

Table 5. Bit assignment for optical driver diagnostic register.

The host procedure is to read the register for READY low. Then the host writes one CS high; none will be enabled if more than one is chosen. The host then reads the register for READY high. If READY is low, drive CS low and retry. Host sends 8 writes, sending a probe-code as described in Finisar application note AN-2010; each write must have the CS line high and the SCLK line high. The host then writes 0 to disable CS, then writes the CS high again, along with SCLK enable. Read the register nine times to get the data encoded on bit 1. The last eight reads has the hex value returned from the Finisar. Write all zeroes when finished. Note that codes in AN-2010 are in decimal and values returned from the Finisar are in hex, MSB first.

4.5 Board Serial Number

Reading Subaddress 11 from either board RT gives the serial number hard-wired onto the Sequencer. It is an eight bit number and each board shall have a unique number.

4.6 Front Panel

Front panel displays include hex displays of the eight bus lines; again, the HDI desired is selectable in Status register 1 bits 8 and 9, and bit 10 selects the Sequencer half to be displayed. LEDs for each half of the Sequencer indicate Idle, Acquire, Cal_Inj cycle, and normal Trigger. Board-wide indicators are Parity error, No Synch, and 1553 strobe. Sixteen lines from each half of the Sequencer are available for probing with an oscilloscope or logic analyzer.

5 1553 REGISTERS

The following table defines the 1553 registers used by the SVX Sequencer.

<u>Subaddress</u>	<u>Function</u>
0	N/A 1553 spec defines as Mode Code
1	Init HDI A
2	Init HDI B
3	Init HDI C
4	Init HDI D
5	Crossing pulse width (Odd or Even RT controls both board halves)
6	Calibration voltage (Odd or Even RT controls both board halves)
7	Calibration pipeline (Odd or Even RT controls both board halves)
8	Sequencer ID (appears in readout data stream)
9	Control/Status Register # 1
10	Control/Status Register # 2
11	CSR #3 HDI Power command (bits 0-3), HDI Ignore (bits 4-7)
12	Read current state of bus and control lines
13	Read logic analyzer FIFO (4096 words deep)
14	Fiber Test path AB, FIFO AF flag value
15	Fiber Test path CD, FIFO AF flag value
16	EPLD Programming Register
17	EPLD Programming Key
18	Read Laser-Driver Status Link
19	Board Serial Number

Table 6. Definitions of the 1553 registers.

<u>Slot</u>	<u>Top R.T.</u>	<u>Bottom R.T.</u>	
2	0	1	1553 Cable 1
3	2	3	
4	4	5	
5	6	7	
6	8	9	
7	A	B	
8	C	D	
9	E	F	
10	10	11	
11	12	13	
12	0	1	
13	2	3	
14	4	5	
15	6	7	
16	8	9	
17	A	B	
18	C	D	
19	E	F	
20	10	11	
21	12	13	

Table 7. Geographic addresses of the crate's slots.

6 Operation

6.1 Initialization

The following is a procedure describing the general initial setup of the SVX Sequencer. A good way to set up new software is to mimic the commands on the Excel spreadsheet in the folder Doserver1\Projects\Electronics\Svxseq3. Set the crossing pulse width to h30, Cal voltage to h80, Cal pipeline to match what is downloaded into the SVX chips. Load the Sequencer ID with a value corresponding to some meaningful relationship with the detector configuration. After turning on power to the chips, set bits 0 through 3 of subaddress 11 to enable the bus and control lines to the HDIs. Bits 4 through 7 could be set to ignore a known-bad HDI. Write bit 4 high to Subaddress 10 to get the chips into the initialize mode.

To set the FIFO flag offsets, first write h4000, then h4080 to Subaddress 9, then write 2525 four times each to Subaddresses E and F. This is the correct value for nine-chip HDIs (see section 6.2).

Next, set the desired Status Word, HDI Select, and Logic Analyzer Trigger bits in Subaddress 9, making sure that bit 14 is low.

To initialize the chips use Subaddresses 1 through 4, where each bit of the serial 1553 signal is used for the serial download to the chips. Therefore, bits go to the chips in multiples of sixteen. Since each chip has 190 bits in its initialization shift register, twelve words are sent for each chip in a string. Twelve times sixteen is 192, resulting in two “filler bits” per SVX that must be sent in the beginning of the first word.

A three-chip HDI will require 36 1553 data words. The first data word will have six filler bits. An eight chip HDI will require exactly 95 data words with no filler bits. A nine chip HDI will require 107 data words with two filler bits in the first word.

After an HDI is downloaded, a “1” must be written to the appropriate Shadow Register bit in Control/Status register # 2 in order to latch the critical bits into the SVX chips. After this fleeting bit is sent, the SVX input shift register may be read to verify a correct download.

6.2 Setting the Almost-Full Flags

When an SVX chip passes priority to the next chip, an input clock cycle is skipped, so there are gaps in the data strobes from the SVX chip. Therefore the FIFOs in the Sequencer can be read out faster than they are filled. The Sequencer logic uses the “Almost Full” flag from the FIFO to know when to begin emptying the FIFO’s data into the G-Link. The Almost Full flag goes active a predetermined number of words before the FIFO is full. This number is adjustable, and we use this feature to hold deadtime to a minimum.

In order for the Sequencer’s FIFOs to operate properly it is important to have bit D14 of Subaddress 9 high when doing a reset to the board (Bit 7 of subaddress 9). This tells the FIFOs that we want to use the Almost-Full flags. Once the reset has been done Bit 14 should be set low prior to data taking.

To set the flag depth if the reset *has* already been done, set bit D14 of Subaddress 9 high. You must then write four values to subaddresses 14 and 15. With this FIFO, the third value

written determines the location of the Almost-Full flag; the current best value is hex 2828. (The FIFO is 64 bytes deep, and 28 hex is 40 decimal, so 64-40 is 24 bytes are filled in the FIFO before being read out, which leaves enough time for the gaps in the SVX data). Bits D00-D07 write to FIFOs A and C, and Bits D08-D15 write to FIFOs B and D. See the data sheet for the IDT72421 FIFO for more details, but note that I invert bit D14 of subaddress 9, which goes to the /LD pin of the FIFOs.. When done, write bit D14 low.

Important: since the reset line on the Sequencer is common to both halves of the board, the correct sequence for loading the flags if the reset has *not* been previously done is to write to subaddress 9 for both halves of the board (both RTs), then write the values to subaddresses 14 and 15 for both halves of the board, then write bit D14 low for both halves. If the sequence is done for each half separately, the second reset will clear the flag settings for the first half, and data errors may result.

6.3 G-Link Error Recovery

If the G-link becomes out of synch, a 1 written to bit D6 of subaddress 10 might re-synch it. A software reset is another thing to try.

If the SVX chips become frozen, a 1 written to bit D4 of subaddress 10 may restore operation. This operation is also recommended after initial power-up of the SVX chips. These bits need not then be written low.

Sections 6.4 through 6.7 explain several features of the Sequencer added as retrofit logic to fix unforeseen problems.

6.4 Readout Abort Feature

The Readout Abort feature was added to recover HDIs which would cause Front End Busy because one of the chips would not send Priority_Out, thus failing to indicate end-of-readout. Implementation is mostly on the Sequencer Controller. Basically there is a modulo 340 counter which is started at the beginning of SVX readout which is set to send a pulse to the state machine when 44.9us has elapsed. This is just about the time it takes to read out a 9-chip HDI in read-all mode. If this time elapses, a code is sent to the Sequencers that gets its state machine from the “waiting for end-of-readout” state back to the acquisition state.

On the Sequencer, however, in the Appender EPLD, there is a circuit that looks at the three least-significant bits of the data coming from the SVXs and if the data is the same for two consecutive clock cycles on both edges of the clock, then it is assumed that the Chips are not outputting Chip IDs and a pulse will be sent to the Control EPLD which will also cause a readout abort and send the main state machine back to the acquire state.

6.5 Front Panel BUSY Wiring

In order to present the Trigger Framework with a better indication of the Busy state of the Sequencers, we added a daisy chain of wires across the front panels back to the Controller in 2004. Each Sequencer sends BUSY back to the previous board when either its Mode1 line is high (it is either in digitize mode or readout mode), or the Sequencer to the right is indicating BUSY. Therefore if any board is busy the Controller will then indicate BUSY to the Trigger Framework via the return link which runs antiparallel to the SLC.

6.6 The Heartbeat System

In order to counteract a known feature of the SVX chip in which lack of triggers can cause high current draw on the DVDD supply, possibly fusing wire bonds, the Heartbeat system was devised in 2004. Only a few clocks in digitize mode once every ten seconds or so are needed to keep the DVDD current low, so a trigger generator was installed in the moveable counting house that causes the Trigger Framework to send special “heartbeat” triggers to the Trig_In lermo on the front panel of each SMT Sequencer Controller. The SeqC then interprets this pulse just like a Level 1 Pulse from the SCL and a non-physics trigger occurs, keeping the SVX current low.

See D0 Note 5918 for a description of the complete system.

6.7 The Defibrillator

In August 2006 the Heartbeat portion of the Trigger Framework tripped and high current alarms occurred in many of the HDIs. After this incident, there were about 41 additional HDIs that didn't download or read out data. It was determined that large SVX current draw apparently opened wire bonds to several SVX chips. Many of these chips have since been recovered by a revised Adapter Card design but in order to try to prevent such occurrences in the future, the Defibrillator was developed. This modification implements a watchdog timer IC on the Controller whose timer is reset by every trigger or heartbeat. If neither occurs for 90 seconds, the timer will time out and the Controller will send a Trip code across NRZ to all the Sequencers. The Sequencers will turn off SVX power by dropping the HDI_Enable signal going to the Interface Boards.

Please see Engineering Note U090202 for a more detailed description of this modification.

For a detailed description of the incident causing the failures and the subsequent engineering effort, please refer to DZero Note 5697.

7 JTAG

The JTAG interface of the in-system-programmable EPLDs is used for burning the program into the EPLDs. There are four lines: TDI, TDO, TCK, and TMS. TDI and TDO are the data lines and are daisy chained from one EPLD to the next. TMS is a control line and TCK is the clock. The procedure will be to convert the Altera output file into the bitstream necessary to program the EPLDs, then ship the bitstream via 1553 to subaddresses 16. Table 8 & 9 show the bit assignments. Subaddress 17 is a “key” into which a code must be written prior to programming the EPLDs. This code is h0D. Unlike downloading the SVX chips where every 1553 data word loads sixteen bits, each 1553 data word sends only one bit to the JTAG port (One bit every 20 μ s, plus the overhead of Control and Status words in the 1553 protocol.). This is slower but will be exercised only when reprogramming of the EPLDs is necessary; nevertheless, the complete programming of all four EPLDs is projected to take less than one minute per card.

1553 Bit	Write	Read
4	Key[4]	0
3	Key[3]	TDO
2	Key[2]	0
1	Key[1]	0
0	Key[0]	Unlocked = 1

Table 8. 1553 bits for programming the ISPLDs via the JTAG port, Key Register, Subaddress 17

1553 Bit	Write	Read
4	N.A.	0
3	N.A.	0
2	TDI	TDI
1	TMS	TMS
0	TCK	TCK

Table 9. 1553 bits for programming the ISPLDs via the JTAG port, JTAG Register, Subaddress 16

APPENDIX A

The Schematic Diagram for this board is number 3823-110-EC-330169 can be found in the D0 flat files at the northeast corner of the third floor of DAB. The OrCad file is in the folder D0server1\Projects\Electronics\SVXSeqd. The backplanes are described in Engineering Notes 3823-110-EN-478 and 3823-110-EN-479. This information can also be found at <http://d0server1.fnal.gov/users/utes/default.htm>.

APPENDIX B

The most up-to-date versions of the EPLD files are kept by the SMT group and the CFT group.

APPENDIX C

Jumper Placement

JMP1	TOP for EPROM loading of EPF8452
JMP2	BOTTOM for EPROM loading of EPF8452
JMP3	BOTTOM for EPROM loading of EPF8452
JMP4	TOP for EPROM loading of EPF8452
JMP5	LEFT for 15 second timeout on 1553 12MHz crystal power
J1, J17, J5, J18	ON for normal operation of Clock Buffers
J3, J8	UP for 53MHz readout, DOWN for crystal controlled readout
J4	LEFT
J7	BOTTOM

G-Link Speed Jumpers:

MHz.....	42-75	21-51	11-25	7.5-13
DIV1 (top).....	OFF	OFF	ON	ON
DIV0 (bottom).....	OFF	ON	OFF	ON

APPENDIX D
Crossing Width and Vcal Settings

<u>Hex value</u>	<u>C. Wid (ns)</u>	<u>V. Cal Volts</u>
0	13	0
8	13.3	.126
10	15.5	.287
18	18	.446
20	20.4	.61
30	25	.93
40	29.4	1.24
50	33.8	1.56
60	38	1.9
70	42	2.22
80	46.9	2.53
90	50.6	2.85
A0	54.7	3.16
B0	58.9	3.48
C0	62	3.8
D0	66	4.12
E0	69.6	4.44
F0	72.7	4.76
FF	77.1	4.99