Fermi National Accelerator Laboratory

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Engineering Note

Date: 1/28/00

Project: SVX Sequencer Backplane
Doc. No: U010128A

Subject: Temperature Rise Measurements

Introduction

The SVX Sequencer J1 backplane (D0 Engineering Note Number 3823.110-EN-478) was measured for temperature rise at expected operating current. The backplanes provide the Sequencers with +5 volt and -5.2 volt power. The backplane was specified by Fermilab and designed and built by Interlogic Industries of Melville, NY. It is a six layer board with two layers for signals, two identical 2 oz. Copper layers for ground, and two identical 2 oz. Copper layers sharing the two power planes. Three (+5, -5.2, GND) tin-plated, oxygen free copper busbars are attached to the backplane via soldered-on power bugs, spaced every 0.8". Maximim current density in the busbar is 160A/(.0625" x 1.5") = 1706A/sq. in.

When calculations were made to determine current density in the backplane, some fairly large numbers resulted (see tables 1& 2) most frequently for the -5.2 volt plane.

Location	Current Density (A/sq. in.)
Vertical channel above power bug	17,708
Above slot 17, below screw hole	24,000
Above slot 16	14,545
Above slot 15	13,636
Above slot 4	3636

Table 1. Current density calculations for portions of the J1 -5.2 volt plane. The first two were the largest values expected due to conductor geometry.

Location	Current Density (A/sq. in.)
Copper Channel into slot 5	5555
Copper Channel into slot 9	4348
Copper Channel into slots 18-21	3077
Copper Channel into slots 20-21	7143
Copper Channels into slot 1	27,800

Table 2. Current density calculations for portions of the J1 +5 volt plane. The last entry was the largest value expected due to conductor geometry.

As a result of these calculations, temperature measurements were made of the backplane under worst case conditions to determine actual heating.

Preliminary resistive load test--No forced air cooling

The test consisted of installing power resistors in each slot downstream (slots 2 - 15) of the suspected worst case conducting channel, connected between the -5.2V pins and ground and powering-up the crate, then measuring the temperature at various points until thermal equilibrium was reached. The resistors were sized to draw slightly more current per slot (3.3A) than the Sequencers (3.0A). Note that this test was carried out without forced air cooling. Results are shown in Table 3.

Time	Temp at Resistors	Temp above slot 17	Temp above slot 11
0 min.	71	71	71
5	357	95	102
10	422	103	118
15	465	113	144
20	480	120	155
25	484	124	162
40	489	126	166

Table 3. Measured temperature of the -5.2 volt portion of the backplane at intervals after being powered. The higher temperatures at slot 11 are due to the fact that the resistors were heating the backplane due to their proximity. There is actually less current through this portion of the backplane. The resistor in slot 15 was probably close enough to affect the temperature above slot 17.

The most suspect portion of the +5 volt plane, the narrow conductor channels carrying current to the two power pins of slot 1, was also tested with a 3.3 A current draw. The temperature rise in this area was two degrees Celsius after thirty minutes.

Fully-loaded crate with production cards

This test was carried out using a fully loaded crate: twenty Sequencers and one Sequencer Controller. Cooling was done using a six fan pack blowing ambient air. The current draw for the +5V supply is 96 amps and that for the -5.2 V supply is 58 amps. Temperatures were measured as follows:

Time	Temp at Bus Bar	Temp above slot 17	Temp above slot 11
0 min.	72	72	72
10	80	89	84
20	80	89	84
30	80	89	84

Conclusion

The high current density above slot 11 of the -5.2 Volt portion of the backplane results in at most a 55 degree F (30 degree C) temperature rise in that area of the backplane, without forced air cooling. Under actual operation with moderate forced air cooling the temperature rise is 17 degrees F (9 degrees C).

The J2 and J3 backplanes carry signals only from logic gates, the most drive being 128mA.