



Fermi National Accelerator Laboratory

D0 Silicon Strip Detector Upgrade Project

SVX SEQUENCER CONTROLLER BOARD

D0 Engineering Note Number 3823.110-EN-557

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1 INTRODUCTION

The Sequencer Controller boards are 9U by 340mm circuit boards that will reside in slot 1 of each of eight Sequencer crates in the D0 detector platform. The primary purpose is to control the Sequencers during data acquisition based on trigger information from the D0 Trigger Framework.

Functions and features are as follows:

- Receives the Serial Command Link (SCL) from the D0 Trigger System and controls the operation of the Sequencers by forming a custom serial control link (NRZ/Clock) which is distributed individually to each Sequencer via the J1 Backplane.
- Controllable delays adjust NRZ control link phasing to compensate for the various cable-length delays between the Sequencers and SVX chips. Delay control is common for slots 2-11, and for slots 12-21 of the crate.
- Each NRZ control link is phase controlled so that commands reach each Sequencer in a given half-crate simultaneously, i.e., the link is compensated for backplane propagation delays.
- External communication via MIL-STD-1553.
- Stand-alone operation via 1553 trigger commands in absence of an SCL link.
- 1553-writeable register for triggering a laser, etc. followed by an acquisition cycle.
- TTL front panel input to trigger an acquisition cycle, e.g. from a scintillator.
- Synch Trig, Veto, Busy and Preamp Reset TTL outputs on front panel LEMOs.
- On-board 53.104 MHz oscillator for stand-alone operation.
- 1553 or SCL-triggerable Cal-inject cycle.
- Front-panel inputs to accept NRZ/Clock link from the VRB Controller.
- Front panel displays and LEDs show the board status at a glance.
- In-system programmable EPLDs are programmed via Altera's "Byteblaster".

Figure 1 shows the block diagram of the Sequencer Controller.

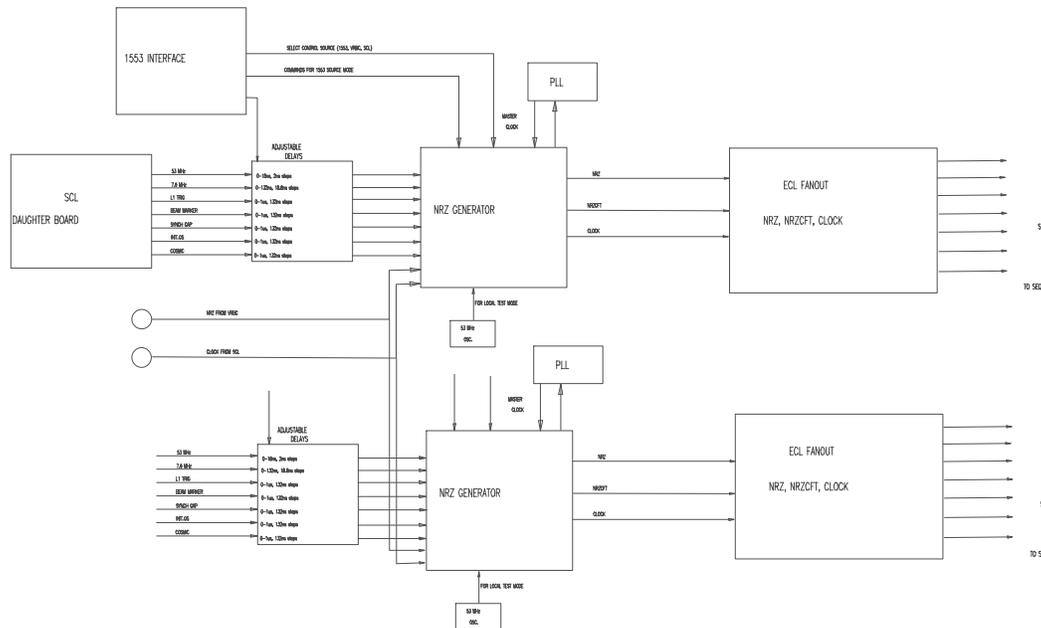


Figure 1. Block Diagram of the Sequencer Controller

2 I/O CONFIGURATION

2.1 General Configuration

The boards will reside in slot 1 of the SVX Sequencer crate. Slots 2 through 21 are available for Sequencers. Half of the Controller will distribute NRZ and Clock to slots 2 through 11, and the other half will service slots 12 through 21. The Serial Command Link will plug into the front panel, as will the 1553 connection.

2.2 Interface to the Serial Command Link

The SCL plugs through the front panel into the SCL Receiver daughter board. This board creates parallel bits defined in the D0 SCL Specification. The bits used by the Controller are:

- 53 MHz
- 7.6 MHz
- L1 Accept
- First Period In Turn
- Real Beam Marker
- Sync Gap
- Cosmic Gap
- SCL ReadyL1 Accept Qualifiers

2.3 Interface to the SVX Sequencers

The dual signal serial links consisting of NRZ and Clock originate in the Sequencer Controller based on timing and triggering information received from the SCL. Two serial links travel on the J1 backplane to each Sequencer, one for the Silicon system and one for the Fiber Tracker system. There are four lines to each Sequencer. Two lines make up a differential clock, a third line is for Silicon NRZ, and the fourth line is for Fiber NRZ. NRZ stands for Non-Return to Zero and is a basic data transmission protocol whereby a high represents a logic 1 and a low represents a logic 0. The Clock line simply acts as a strobe for NRZ. In our control link, NRZ consists of a continuous stream of seven-bit packets, each bit being the same duration as one Tevatron RF cycle. The packets are synchronized with the accelerator. The bits in each packet consist of one framing bit which is always high, a bit which is high if a beam crossing is imminent, four bits representing the command desired, and one parity bit (odd parity). The definitions of the NRZ codes for Silicon NRZ is shown in Table 2.1.

Idle	0 0 0 0
Acquire	0 0 0 1
Trigger	0 0 1 1
Pipe	1 0 1 1
Ramp	1 0 1 0
Digitize	0 0 1 0
Readout	0 1 1 0
Reset_Preamplifier	0 1 0 1
Cal_Inject	0 1 1 1
Readout Abort	0 1 0 0
Reserved_9	1 0 0 1
Reserved_C	1 1 0 0
Reserved_8	1 0 0 0
Reserved_F	1 1 1 1
Reserved_D	1 1 0 1
Reserved_E	1 1 1 0

Table 2.1. Command codes encoded in Silicon NRZ

The NRZ link for the Fiber system is not encoded. Instead, each bit has a definition as follows:

Bit 1	Framing Bit
Bit 2	Spare
Bit 3	CFT Reset
Bit 4	Synch Gap
Bit 5	1st Crossing
Bit 6	L1 Accept
Bit 7	Parity Bit

Table 2.2. Command codes encoded in CFT NRZ

A table of the backplane signals exists in Appendix A.

2.4 Front Panel Connections

2.4.1 1553 Connection

The 1553 connection for the Controller is on the Front panel. Connect the 1553 cable into one of these connectors. Two triaxial connectors exist so that if there are more 1553 Remote Terminals at some other location, a second cable can be connected to put that RT in the chain. If there are no other terminals downstream, a 75 ohm termination must be connected to the second connector.

2.4.2 Optional NRZ Inputs from the VRB Controller

In some test setups there will not be an SCL available. In this case, the triggering information will come from the VRB Controller in the form of differential ECL NRZ and Clock. These inputs are on the front panel.

2.4.3 Optional Triggering Inputs and Outputs

In some cases it may be desirable to have triggering logic interface directly to the Sequencer Controller. Here are the descriptions of these signals:

TRIG-IN Front Panel Input operation

A high pulse applied to the TRIG-IN input will cause a data acquisition cycle to occur in the SVX chip. Typically, this pulse is applied to the Sequencer at the same time charge is injected into the SVX. The charge pulse should be synchronized to the SVX crossing clock using the VETO-OUT signal.

VETO-OUT Front Panel Output operation

VETO-OUT is provided to be externally ANDed with a random (e.g. scintillator) trigger so that a charge pulse is applied to the SVX at the proper time. The idea is to allow the charge pulse to arrive at the SVX within a window of time that begins at the falling edge of the SVX crossing clock and lasts for approximately 56ns. This narrow window assures that none of the pulse's charge gets injected into the subsequent pipeline cell of the SVX chip. A pulse concurrent with the charge pulse should be applied to the TRIG-IN input to trigger the SVX digitization cycle.

VETO-OUT is synchronous with the clock and pulses high for 56ns in 132ns crossing mode, beginning 58ns after the falling edge of the SVX acquire clock. It pulses high for 130ns in 396ns crossing mode, beginning 22ns after the falling edge of the SVX acquire clock.

A user-provided delay on the charge pulse must be provided to ensure the earliest moment charge can be injected is just after the falling edge of the acquire clock as measured at the SVX. VETO-OUT is low during preamp resets and while BUSY is low (while the SVX is in digitize and readout mode).

SYNCTRIG output operation

This output signal is designed to be used to synchronously trigger an external pulse into the SVX chip (e.g. a laser). When bit D01 is written high to the Trigger Register, a pulse will appear on this output, and a digitization/readout cycle will commence. In 132ns mode, this pulse occurs in pipeline 5, 130ns before the leading edge of the next crossing pulse at the SVX. In 396ns mode, this pulse occurs in pipeline 2, 220ns before the leading edge of the next crossing pulse at the SVX. These measurements assume a 28' grey cable to the SVX. Note that two or three consecutive D01 bits might need to be written to ensure that the occasional Preamp Reset is not interfering with the asynchronous software-generated trigger.

3 GENERAL CONTROL CIRCUITRY

3.1 Remote Terminal address

The 1553 RT address is configured by dipswitch S1 positions 1 through 5. Position 1 is the LSB. This should be set to a number unique from any other RT on the 1553 bus.

3.2 1553 Register List

Each RT in the module has a subaddress structure as shown in Table 3.1:

<u>Subaddress</u>	<u>Function</u>
1	Control/Status Register, Left half of Crate
2	Diagnostic Triggering Register
3	NRZ delay in 2ns steps
4	NRZ delay in 18.8ns steps
5	NRZ delay in 132ns steps
6	SCL Status Bits
7	
16	Control/Status Register, Right half of Crate
17	Diagnostic Triggering Register
18	NRZ delay in 2ns steps
19	NRZ delay in 18.8ns steps
20	NRZ delay in 132ns steps

Table 3.1 Subaddress definitions

3.3 Control/Status Register

There are four bits in the Control/Status Register defined as follows:

<u>Bit</u>	<u>Function</u>
0	Trigger Source bit 0
1	Trigger Source bit 1
2	Pedestal adjustment bit
3	Undefined
4	High = Framing bit only for NRZ_CFT
5	High = SCL L1Accepts cause Cal Injects
6	High = Abort Readout after 3.5 us
7	High = general Reset to board

Table 3.2 Control/Status Register bits

There are three possible operational modes for running the Controller, each depending on the source of the trigger. Table 3.3 shows how to set bits 0 and 1 for each of the modes.

<u>Bit1</u>	<u>Bit 0</u>	<u>Function</u>
0	0	Trigger Source from SCL
0	1	Trigger Source from 1553
1	0	Trigger Source from VRBC
1	1	Undefined

Table 3.3 Trigger source table

The pedestal adjustment bit adjusts the delay between the start of the ramp and the start of the counter of the Wilkenson ADC in the SVX chip. When set to 1, an extra delay of 132ns is incurred, putting about 14 extra counts onto the pedestal.

When bit 4 is set to 1 the NRZ_CFT signal will only have the framing bit, allowing the Sequencer to set up synchronization on that link.

When bit 5 is set high, the Controller is put into SCL Cal Inject mode whereby a L1Accept arriving from the SCL causes a Cal Inject cycle in the Sequencers instead of the normal beam collision digitization.

When bit 6 is set high, the Controller will, via NRZ, cause the Sequencer to abort Readout mode after 3.5 us, preventing very long readout times when an event has an overabundance of channels over threshold.

When bit 7 is set to 1 a reset is given to the control logic in the NRZ generator. This bit need not then be set to zero.

3.4 Diagnostic Triggering Register

The Diagnostic Triggering Register is active when bits 1 and 0 of the CSR are set to 1553 mode as shown in Table 3.3. In this mode, triggers come solely from 1553 commands. For operation of the Diagnostic Triggering Register, please refer to section 4.

3.5 Delay Control Registers

For proper detector operation, it is important to have all SVX chips synchronized to the Tevatron beam crossings during the acquire mode. Since space in the detector platform is at a premium, all signal carrying cables could not be made the same length, so the Sequencer Controller has some signal delay features to compensate for these differing lengths. After adjustment is made, all SVXs should have crossing clocks occurring simultaneously while in the Acquire mode.

3.5.1 Subaddress 3, 18

This register adjusts the delay of the Clock to the Sequencers in 2.5ns steps. It does this by means of selecting the appropriate tap on an analog delay line. There are ten taps, so allowable values for this register are 0 through A hex. 0000 has the least delay of zero ns.

3.5.2 Subaddress 4, 19

This register adjusts the delay of the NRZ to the Sequencers in 18.8ns steps by means of delaying the 7.6 MHz strobe to the shift registers described in 3.4.3 through an adjustable length shift register. Bits 0 through 2 are the only active bits, so there are eight possible delay settings for a maximum of 132ns. Again, a setting of 000 has the least delay of zero ns.

3.5.3 Subaddress 5, 20

This register adjusts the delay of the NRZ to the Sequencers in 132ns steps by means of sending each line of the Serial Command link through an adjustable length shift register. Bits 0 through 2 are the only active bits, so there are eight possible delay settings for a total of 923ns. A setting of 000 has the least delay of zero ns.

4 DIAGNOSTICS

4.1 Diagnostic Triggering Register

The Diagnostic Triggering Register is active when bits 1 and 0 of the CSR are set to 1553 mode as shown in table 3.3. In this mode, triggers come solely from 1553 commands. The following are the most frequently used sequences of commands.

4.1.1 Trigger Register operation

The Trigger Register (2, 17) puts the SVX in initialize mode for downloading, initiates Cal-Inject cycles or software-generated triggers, and sets the crossing interval for non Cal-Inject cycles. Cal-Inject mode operates in 132ns mode only.

Cal_Inject Sequence long after a Preamp Reset:

<u>Command</u>	<u>Function</u>
80	Go to IDLE to prepare for Cal_inject or Downloading the SVX chip
88	Sets Acquire mode for Cal_Inject preparation
A8	(Optional) Reset the preamp before initiating a Cal_Inject
84	Initiate a Cal-Inject cycle
80	Back to IDLE

Cal_Inject Sequence eighteen acquire clocks after a Preamp Reset:

<u>Command</u>	<u>Function</u>
80	Go to IDLE to prepare for Cal_inject or Downloading the SVX chip
84	Sets Acquire mode and then initiates a Cal_Inject cycle
80	Prepare for another cycle

Cal_Inject Sequence with a random Preamp Reset prior to it:

<u>Command</u>	<u>Function</u>
00	Sets Acquire mode
88	Initiates a Cal-Inject cycle
80	Prepare for another cycle

To prepare for Software-generated Triggers:

<u>Command</u>	<u>Function</u>
00	Set crossing interval to 132ns, or
01	Set crossing interval to 396ns
02	Send trigger in 132ns mode, or
03	Send trigger in 396ns mode

To prepare for External Triggers:

<u>Command</u>	<u>Function</u>
00	Set crossing interval to 132ns
01	Set crossing interval to 396ns

System waits for trigger, when it occurs, BUSY goes active and an interrupt is sent to the processor. When the FIFO has been emptied of data BUSY will go low and another trigger is allowed.

4.2 Front Panel Indicators

Front panel displays include two hexdisplays, each one showing the NRZ code being sent on its half of the Sequencer backplane. Lemo coaxial connectors exist for monitoring preamp reset interval and the 53MHz clock received from the SCL. LEDs exist for power, 1553 strobe, L1 Trigger, L2 Accept, Beam crossing, SCL Init, and SCL Error. A monitoring connector provides 1553 signal, NRZ, CFT NRZ, and board voltages.

4.2.1 Display Showing the NRZ code

The front panel display that shows the current NRZ code can be interpreted by the following:

<u>Display</u>	<u>Code</u>
0	Idle for Initialize
1	Acquire
3	Trigger
A	Ramp
2	Digitize
6	Readout
5	Preamp Reset
7	Cal_Inject
Others	Unused

4.3 SCL Status Register

This register displays four status bits which the SCL Receiver card offers as outputs:

<u>Bit</u>	<u>Definition</u>
0	SCL_READY
1	SCL_SYNCERROR
2	SCL_DATAERROR
3	INIT_SECTION
4-7	Unused

Only bit 0 should be high during normal operation. If any other bit is high a Sequencer Controller reset may clear the condition; otherwise a reset at the hub end of the SCL may be necessary. A description of the bits defined above may be found at:
http://www-ese.fnal.gov/d0trig/SCLR_Spec.pdf

5 Operation

5.1 Setting the RT Address

The 1553 RT address is configured by dipswitch S1 positions 1 through 5. Position 1 is the LSB. This should be set to a number unique from any other RT on the 1553 bus.

5.2 Initialization

Refer to Figures 3.2 and 3.3 and load the Control/Status Register in subaddress 1 for 1553 triggering. Set subaddress 2 for acquire mode. This allows crossing clocks to appear at the SVX chips. With SVX Emulator boards in place, monitor the clock line to adjust subaddresses 3, 4, and 5 to make the crossing clocks simultaneous. Then set the CSR back to the desired operating mode.

6 JTAG

The EPLDs (Erasable-Programmable Logic Devices) are programmed via Altera's "bitblaster" which plugs into the front panel of the board. The other end of the bitblaster is connected to the PC. The board's EPLDs are programmed by entering the Maxplus program, selecting the "Programmer" option, selecting the right set of files to send over the bitblaster, and clicking on the "Program" field.

APPENDIX A

SVX Sequencer Crate J1 Backplane Pin Assignments, Slot 1

<u>Row</u>	<u>Column A</u>	<u>Column B</u>	<u>Column C</u>
1	GND	+NRZ1	-NRZ1
2	+CLK2	+CLK1	-CLK1
3	GND	+NRZ2	--NRZ2
4	-CLK2	+NRZ3	-NRZ3
5	GND	+CLK3	-CLK3
6	+CLK4	+NRZ4	-NRZ4
7	GND	+NRZ5	-NRZ5
8	-CLK4	+CLK5	-CLK5
9	GND	+NRZ6	-NRZ6
10	+CLK7	+CLK6	-CLK6
11	GND	+NRZ7	-NRZ7
12	-CLK7	+NRZ8	-NRZ8
13	+5V	+CLK8	-CLK8
14	+CLK9	+NRZ9	-NRZ9
15	+5V	+NRZ10	--NRZ10
16	-CLK9	+CLK10	-CLK10
17	-5.2V	+NRZ11	-NRZ11
18	+CLK12	+CLK11	-CLK11
19	-5.2V	+NRZ12	--NRZ12
20	-CLK12	+NRZ13	-NRZ13
21	GND	+CLK13	-CLK13
22	+CLK14	+NRZ14	-NRZ14
23	GND	+NRZ15	-NRZ15
24	-CLK14	+CLK15	-CLK15
25	GND	+NRZ16	-NRZ16
26	+CLK17	+CLK16	-CLK16
27	GND	+NRZ17	-NRZ17
28	-CLK17	+NRZ18	-NRZ18
29	GND	+CLK18	-CLK18
30	+CLK19	+NRZ19	-NRZ19
31	GND	+NRZ20	--NRZ20
32	-CLK19	+CLK20	-CLK20

J1 Backplane Pin Assignments, Slots 2-21

<u>Row</u>	<u>Column A</u>	<u>Column B</u>	<u>Column C</u>
1	GND	GND	GND
2	GA0	GND	+NRZ
3	GA1	GND	-NRZ
4	GA2	+5V	GND
5	GA3	+5V	+CLK
6	GA4	+5V	-CLK
7	GND	+5V	GND
8	+5V	GND	+5V
9	+5V	GND	+5V
10	+5V	GND	GND
11	+5V	GND	+5V
12	GND	GND	+5V
13	-5.2V	-5.2V	GND
14	-5.2V	-5.2V	+1553
15	-5.2V	-5.2V	-1553
16	GND	GND	GND

APPENDIX B

The Schematic Diagram for this board is number 3823-112-EB-330306 can be found in the D0 flat files at the northeast corner of the third floor of DAB.

APPENDIX C

The EPLD files may be included on the following pages, but the most up-to-date versions can be found in D0server4\projects\electronics\Seq_Cont_v2. Use Max+plus II to view them.