Silicon Detector Studies using the Laser Test Station at the SiDet Facility

Maria Teresa P. Roco*
Fermi National Accelerator Laboratory
Batavia, IL. 60510-0500

ABSTRACT

This note presents the results of measurements performed on a single-sided test ladder and a production small-angle double-sided detector using the laser test stand setup at the Fermilab Silicon Detector (SiDet) facility.

1 Introduction

Measurements have been performed on a single-sided ladder and a double-sided detector using a 1064 nm laser. These include timing studies to optimize the charge collection efficiency, measurement of the depletion voltage and leakage current, measurement of the charge collection efficiency, risetime, and random noise as a function of the preamplifier bandwidth. The data acquisition and readout electronics are the same as what was used in a recent test beam as described in [1]. The readout system at the SiDet facility has been set up to operate at the 132 ns crossing mode. The detectors were operated at room temperature during these measurements.

The laser setup in the Silicon Detector Facility is described in [2]. A semiconductor laser is used to emit light at 1064 nm wavelength. It is capable of producing light pulses with rise times less than 1 ns. Light is transmitted via an optical fiber 6.2 μm in diameter. The focusing system consists of a collimating lens and an adjustable post holder which allows the vertical positioning of the lens relative to the detector. A spot size narrower than the nominal detector strip pitch of 50 μm has been achieved in [2].

2 SVX-II Download Parameters

For details on the SVX-IIe operation, the beginner’s guide in [3] gives a good overview. The operation of the chip can be set up and controlled by downloading parameters, consisting of 190 bits for each chip, to its internal registers during the Initialize mode. The first 128 bits set up a test input mask and the remaining bits are used for internal control. Table 1 lists the some of the parameters which can be changed by users during download. They are briefly defined below:

*e-mail address: roco@fnal.gov
Table 1: A short list of download parameters for the double-sided detector. Parameters in hexadecimal are preceded by 0x. The parameters for the single-sided ladder are the same as those used for the p-side of the double-sided detector.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>p-side</th>
<th>n-side</th>
</tr>
</thead>
<tbody>
<tr>
<td>PABW</td>
<td>0xC</td>
<td>0xC</td>
</tr>
<tr>
<td>Ramp Trim</td>
<td>0x700</td>
<td>0x700</td>
</tr>
<tr>
<td>Pipeline</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Chip ID</td>
<td>0x90</td>
<td>0xF0</td>
</tr>
<tr>
<td>ADC Pedestal</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Polarity</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

- **PABW**: For different bunch crossing intervals, the response or bandwidth of the SVX-II preamplifier can be adjusted by means of internal switches and capacitors to provide the optimum preamplifier output risetime and minimum noise. A high PABW setting corresponds to a longer risetime which results in a given signal being present in the subsequent interaction interval. A lower PABW setting corresponds to a shorter risetime but the signal may be noisier than necessary. Operating at the $132 \, ns$ crossing interval, the proper bandwidth is chosen such that the risetime at the output of the integrator reaches 99% of its final value in approximately 100 $ns$.

- **Ramp Trim**: adjusts the ramp capacitor value by adding binary weighted capacitors to $C_r$. $1/C_r$ is the slope of the A/D ramp. For the same input signal, a small value of $C_r$ gives a steeper ramp slope (lower # of ADC counts), while a large $C_r$ value which gives a shallower slope (higher # of ADC counts).

- **Pipeline**: sets the offset between the write and read shift register pointers which addresses the 32 pipeline cells (0-31) of the SVX-II. For example, if set to 0, when the acquisition is stopped and a pipeline readout is initiated, the sample which is read out is the last one taken.

- **Chip ID**: to identify each chip in the daisy chain, each one is downloaded with a different chip ID number.

- **ADC Pedestal**: for fine adjustments of the ADC pedestal value. It sets the ramp offset and controls the amount of noise hits observed at any given threshold level.

- **Polarity**: sets the four polarity bits used to choose either a positive or negative input for the SVX-II chip.

Except for the preamplifier bandwidth (PABW) setting, the download parameters listed above are generally kept at their nominal values. For these measurements, data sparsification was not implemented during data taking.
3 Timing Studies

The laser is pulsed externally using a pulse generator. The light pulse emitted by the laser is monitored using a Hewlett-Packard digitizing oscilloscope. The pipeline clock of the SVX-II is also monitored. The time delay between the laser pulse and the readout clock can be varied by changing the delay on the gate generator.

The charge collection efficiency is measured as a function of the time delay and the preamplifier bandwidth (PABW) setting. Fig. 1 shows the collected charge on the single-sided ladder plotted as a function of the time delay in ns for various PABW settings. Maximum charge is collected at about 150 ns for the different PABW values. The slope of the rise is observed to be steeper at smaller PABWs. One also notices a decrease in the collected charge for PABW set to 24 and 63. This is shown more clearly in Fig. 2, where the fraction of collected charge is shown as a function of the PABW setting. For the 132 ns crossing mode, a significant fraction of the charge is lost at large PABW values. For optimum charge collection efficiency, the SVX-II should be operated at PABW ≤ 12. This is not the case for the 396 ns interaction mode, where 100 % charge is collected for the full PABW range.

It is also interesting to plot the collected charge as a function of the time delay for various values of the bias voltage. The timing measurements are repeated at a PABW setting of 12 with the bias voltage set at 20, 40 and 50 V as shown in Fig. 3. There is a almost no difference between the curves for bias voltages 40 and 50 V when the detector is fully depleted. At 20 V when the detector is not fully depleted, less than half of the charge is collected at the optimum delay time.

4 Laser Calibration

From the timing studies, the delay is now set to ~150 ns for optimum charge collection efficiency. The next thing that should be done is to calibrate the laser such that the average charge collected is equal to the number of ADC counts in 1 mip. From recent beam tests, 1 mip corresponded to a most probable value of ~ 26 ADC counts.

This is a straightforward procedure. First, the minimum beam spot size is obtained by positioning the detector about 1 cm away from the focusing lens. Next, the detector response is measured as a function of the laser attenuation. The intensity of the light emitted from the laser was found to be too strong that at the highest attenuation setting, the charge collected in the detector far exceeds the expected value for a mip. The laser output is then split into two optical fibers. With a split beam, a laser attenuation setting of 7.8 dB gave the closest value for the average charge corresponding to 1 mip. Fig. 4 shows the collected charge distribution after laser calibration.
5 Results

The characterization of each silicon detector that will be used for testing or production purposes is an important task. Several standard measurements are performed to determine the detector’s electrical characteristics including the leakage current, depletion voltage and breakdown voltage. The detector will be used in production only if it passes the required specifications given in [4]. The laser test stand has been used to perform a number of these characterization measurements for detector studies.

5.1 Single-Sided Ladder Measurements

Data were taken at different values of the bias voltage $V_B$ from 0 up to 60 V. The leakage current is plotted as a function of $V_B$ as shown in Fig. 5. At 60 V the detector and the readout chips are drawing less than 6 $\mu$A of current. The collected charge is also shown in Fig. 5 as a function of the bias voltage. The charge plateaus at values of $V_B$ larger than 40 V which indicates that full depletion has been reached.

An interesting measurement is to determine the dependence of the random noise in the ladder as a function of the preamplifier bandwidth. As mentioned earlier, the SVX-II chip should be operated at PABW settings $\leq 12$ in order to achieve maximum charge collection efficiency. However, smaller PABW values give rise to noisier signals. This is illustrated in Fig. 6 which shows a fast increase in random noise with decreasing PABW. A similar plot for an irradiated ladder can be found in [1]. It should be noted that these measurements were performed at room temperature. Detector leakage currents are quite sensitive to temperature and can be reduced significantly by operating the detectors between 0-5°C. A recent study showing the temperature dependence of noise is presented in [5].

5.2 Double-Sided Detector Measurements

This section summarizes the results of the measurements performed on the 2nd double-sided detector 1591-15-2. This is the second double-sided (DS) detector to be studied. The first one was concluded to be defective, having a small polysilicon resistance and failing the required electrical specifications. DS 1591-15-2 is considered to be a high quality detector according to earlier probe station measurements at UCR [6]. However, initial laser test stand measurements showed a significant difference in the amount of collected charge between the $p$ and $n$ sides as seen in Fig. 7. In an attempt to understand this difference, one of the studies performed was to measure and compare the risetimes of the two sides at the the output of the SVX-II preamplifier.

A digital oscilloscope, Tektronix TDS620, was used to measure the risetime, defined as the elapsed time in collecting between 1% and 99% of the total charge, for the $p$ and $n$ sides at various preamplifier bandwidth settings shown in Fig. 8 [a,b,c] for the $p$-side and
Fig. 9 [a,b,c] for the n-side. In these plots two number are given on the right hand side. The top one is the risetime obtained by moving the two reference lines on the scope to where one perceives the beginning and end of the charge collection occur, respectively. To some degree this measurement is arbitrary and biased. The second number is obtained by running one of the oscilloscope’s pre-programmed modules which executes a well defined algorithm to calculate risetimes/falltimes and gives reproducible results. Fig. 10 is a summary of the latter results. These plots show that the both p and n sides have similar risetimes for the full bandwidth range. This is expected for good quality detectors and does not explain the difference in the amount of collected charge between the two sides. The dependence of the risetime on the bias voltage is also shown in Fig. 10. The risetime decreases steeply with increasing bias voltage and plateaus when the detector reaches full depletion. For these measurements the DS detector was operated at a bias -50 V.

Another study involved generating known input charges on a number of channels specified by the test input mask. Test input charges are generated by applying an external (CAL) voltage on a small capacitor into the integrator input. Data taken for the p-side showed the expected linear behavior between the collected charge and the applied CAL voltage, which is proportional to the injected charge. However, data for the n-side showed a non-linear behavior as shown in Fig. 11. This was a considered a breakthrough since it gives one an idea where the problem might be. At this point the correctness of the parameters being downloaded to the chips in both the p and n sides has been verified.

The discrepancy in the amount of collected charge between the p and n sides is now understood and is attributed to some components, including the ramp capacitor, which had bad solder connections on the HDI. After repairing the HDI, the data in Fig. 12 show the expected linear relationship for both p and n sides. The measurements taken earlier are then repeated with the bias voltage set to -50 V and the delay set to 162 ns.

The pulse heights for the channels directly under the laser beam shown in Fig. 13 for the p and n sides are now very similar. The leakage current and the collected charge in the p and n sides, are plotted as a function of the bias voltage in Fig. 14 for PABW=12. The collected charge for the p and n sides agree to within a few percent for the bias voltage range up to 75 V. The Gaussian width of the clusters are also compared for the two sides in Fig. 15. It has been observed that the n-side cluster width increases with decreasing bias voltage and plateaus near full depletion, while the p-side cluster size remains constant for voltages even below depletion.

Finally, the random noise is measured for the full bandwidth range and the results are shown in Fig. 16 for both p and n sides. One can convert the number of ADC counts into number of electrons using the conversion 1 ADC count equal to 960 $e^-$. This is obtained using the test beam data where 1 mip was determined to be 26 ADC counts. At the bandwidth setting optimum for the 132 ns crossing mode, the average random noise is 1.2 ADC counts corresponding to an equivalent noise charge of about 1150 $e^-$. 5
6 Summary

The laser station at the SiDet facility has proven useful in performing studies to characterize the silicon detectors and test the operation and performance of the SVX-II and the readout electronics. Future improvements to the system, particularly the laser table motion control and data acquisition software, will be capable of scanning across the detector in small ($\sim 10 \mu m$) steps. This will be useful in determining the variation in the response from channel to channel and characterize the difference in performance between good and bad channels.

Initial laser tests of the double-sided detector identified an unknown (i.e. undocumented) effect on the $p$-side. It was observed that the forward bias of the isolation implants in the $p$-side generated very large leakage currents. This resulted in the modification of the design for the power distribution for the double-sided detectors. The $p$-side should then be operated at negative bias and the $n$-side operated at ground.

References


Figure 1: The collected charge plotted as a function of the delay time between the laser pulse and the readout clock for various preamplifier bandwidth settings.
Figure 2: The fraction of collected charge is plotted as a function of the preamplifier bandwidth setting for the 132 ns crossing mode. To achieve optimum charge collection efficiency, the SVX-II must be operated with $PABW \leq 12$. 
Figure 3: The collected charge plotted as a function of the delay time between the laser pulse and the readout clock for three bias voltage values 20, 40 and 50 V.
Figure 4: Collected charge for the single-sided ladder after calibrating the laser.
Figure 5: (top) Leakage current as a function of the bias voltage. (bottom) Depletion voltage measurement. The collected charge is plotted as a function of the bias voltage.
Figure 6: The random noise in the single-sided ladder, operated at $V_B = +40\,V$, is plotted as a function of the preamplifier bandwidth setting.
Figure 7: (top) The collected charge is plotted as a function of the bias voltage for the p and n-sides of the double-sided detector. (bottom) Timing studies show similar behavior for both p and n-sides. The discrepancy in the amplitudes is explained in the text.
Figure 8: [a] (top) Measurement of the risetime for the p-side of the double-sided detector with $V_B = -50$ V and PABW=0, (bottom) PABW=4.
Fig. 7 [b] Measurement of p-side risetime for (top) PABW=12, (bottom) PABW=24.
Fig. 7 [c] Measurement of p-side risetime for (top) $P_{ABW}=36$, (bottom) $P_{ABW}=63$. 
Figure 9: [a] (top) Measurement of the risetime for the n-side of the double-sided detector for PABW=0, (bottom) PABW=4.
Fig. 8 [b] Measurement of n-side risetime for (top) PABW=12, (bottom) PABW=24.
Fig. 8 [c] Measurement of n-side risetime for (top) PABW=36, (bottom) PABW=63.
Figure 10: (top) Risetime as a function of the preamplifier bandwidth setting (summarizing Figs. 8-9) for the p-side and the n-side of the double-sided detector. (bottom) Dependence of the risetime on the bias voltage (PABW=0).
Figure 11: Non-linear relationship between the collected charge in the n side of the double-sided detector and the applied CAL voltage is attributed to bad solder connections on some components on the HDI.
Figure 12: The expected linear relationship, for both (top) p and (bottom) n sides, between the collected charge and the applied CAL voltage after the bad solder connections on the HDI are repaired.
Figure 13: *Pulse heights on the p and n sides of the double-sided detector after repairing the bad solder connections on the HDI.*
Figure 14: (top) Leakage current as a function of the bias voltage. (bottom) Depletion voltage measurement. The collected charge is plotted as a function of bias voltage.
Figure 15: The number of strips in the cluster plotted as a function of the bias voltage for the p and n sides of the double-sided detector DS 1591-15-2 with PA BW=12.
Figure 16: The random noise in the p and n sides of the double-sided detector DS 1591-15-2, operated at $V_B = -50$ V, is plotted as a function of the preamplifier bandwidth setting.