

SVX Power and Input Offset Voltage Studies at NWA
September 25,1997

L. Bagby, M. Johnson, R. Lipton

During the test beam run of the Silicon and VLPC upgrade detectors for D0, the SVX occasionally exhibited a run-away current mode after applying power to the chips. This study was conducted to determine how often this condition occurs. It was also found that the proposed method of compensating the SVX input offset voltage within the SIFT chip did not work. The offset voltages of several SVX chips were measured to determine the magnitude of variance across the chip.

Manual Current Measurements

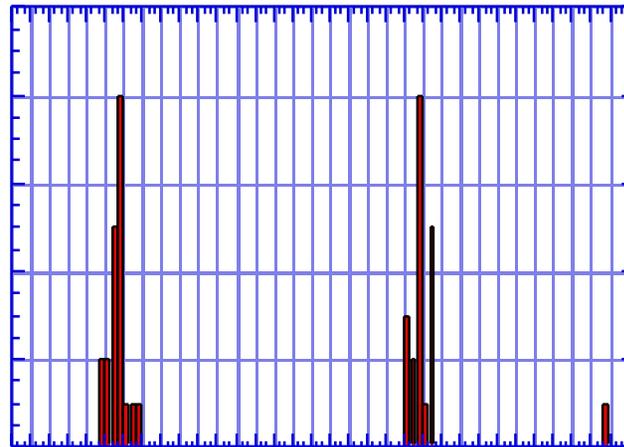
The SVX chip requires three power supplies for operation. They are named AVDD1 (5.2V), AVDD2 (3V), and DVDD (5.2V). At NWA these supplies were provided by a Tektronix PS2521 which is equipped with a GPIB interface. The SVX chip is extremely sensitive to the order in which these supplies are presented. AVDD1 is first, AVDD2 is second, and DVDD is third. During normal operation the Port Card is activated after the SVX and then the crate (VRB). The current associated with each SVX supply was recorded after all three SVX supplies were on, again after the Port Card was activated, and a third reading was recorded after the crate was activated. The rise time of the power supplies were measured to be 22.4 ms for AVDD1, 29.9 ms for AVDD2, and 50.14 ms for DVDD. The following table shows the total current for 26 SVX chips as well as a per chip current and power calculations. AVDD1 current increases and DVDD current decreases after the Port Card is activated. AVDD2 remains fairly constant throughout the process. The histograms show the overall distribution of the 20 samples.

Figure 1: Summation of SVX Power Supply Current for 20 Samples

26 CHIPS	INITIAL (A)	AFTER PC	AFTER CRATE
AVDD1	.634	.734	.734
AVDD2	.567	.572	.572
DVDD	1.060	.624	.656

POWER/CHIP (W)			
AVDD1	.127	.147	.147
AVDD2	.065	.066	.066
DVDD	.212	.125	.131
TOTAL POWER	.404	.338	.344

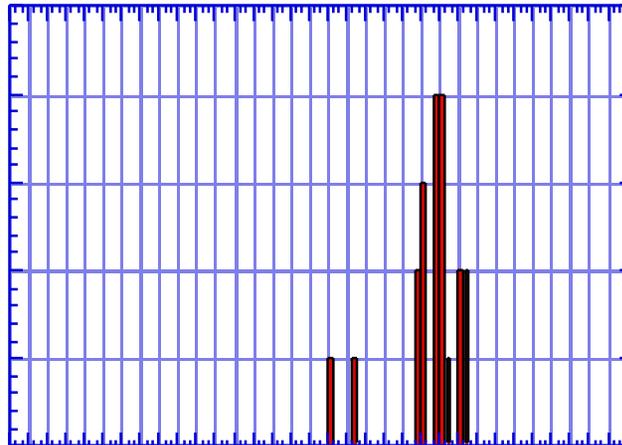
Figure 2: Histogram of AVDD1 power supply current before and after Port Card initialization.



AVDD1 is used for the initialization of the shift register and powers the preamplifier, integrator, and ramp circuitry within the SVX. The 633 mA grouping corresponds to the current of AVDD1 prior to the activation of the Port Card. The current increases ~100 mA after the Port Card and crate are powered. The 790 mA occurrence was recorded after the Port Card was activated. The following table summarizes the statistics for 26 SVX chips.

Mean	0.634	0.734
Median	0.634	0.732
RMS	0.634	0.734
Std Deviation	0.00279	0.0134
Skewness	0.817	3.90

Figure 4: Histogram for AVDD2 power supply current before Port Card initialization.



AVDD2 provides power to the input gain transistor for the integrator. The histograms show that the current for AVDD2 after the Port Card is powered remains approximately the same at 570 mA.

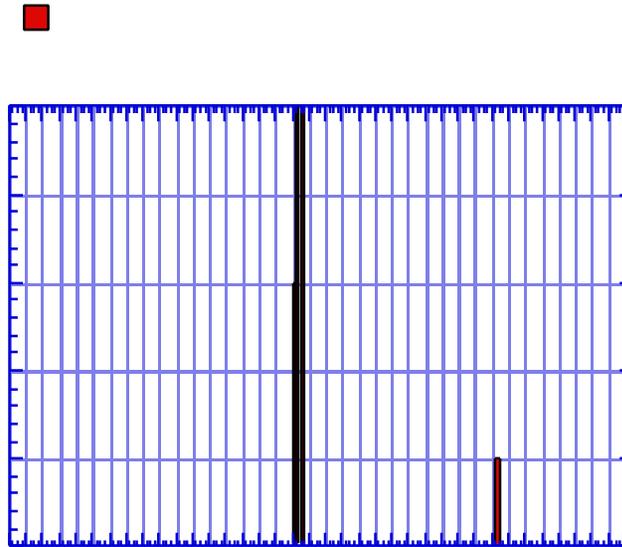
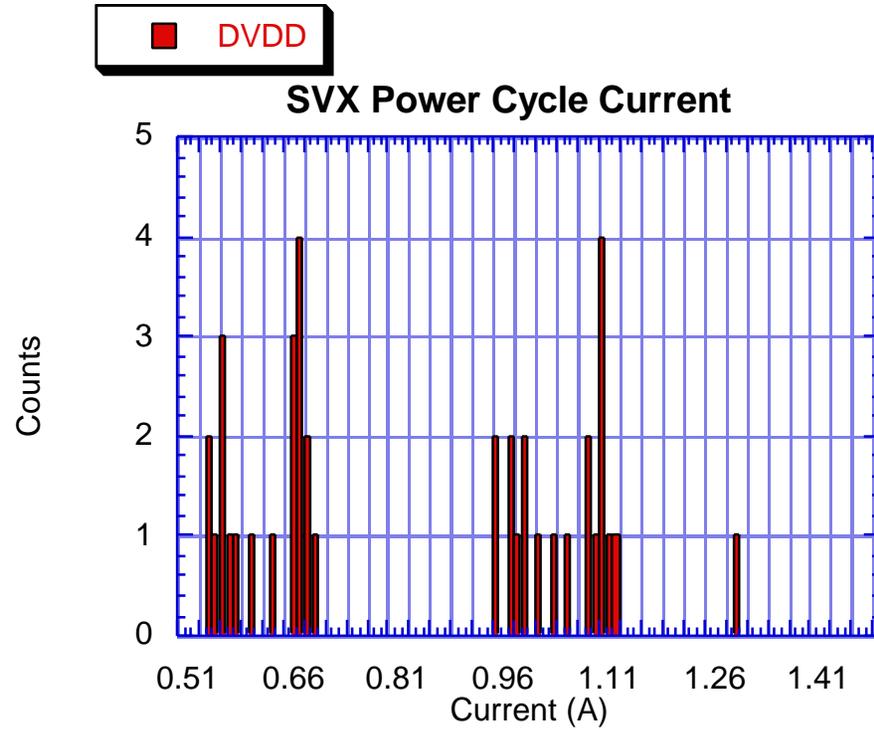


Figure 6: Statistics for AVDD2 power supply current.

Statistics	AVDD2 (A)	AVDD2 after Port Card
Minimum	0.552	0.568
Maximum	0.573	0.618
Sum	11.4	11.4
Points	20.0	20.0
Mean	0.567	0.572
Median	0.568	0.570
RMS	0.568	0.572
Std Deviation	0.00528	0.0108
Skewness	-1.87	4.05



DVDD provides power to the back end comparator, pipeline drivers, and all other digital circuitry. DVDD current decreases ~400 mA after the Port Card is activated. DVDD current, after the crate is activated, varies from .559 mA to .720 mA.

Figure 8: Histogram for DVDD power supply current after the crate is activated.

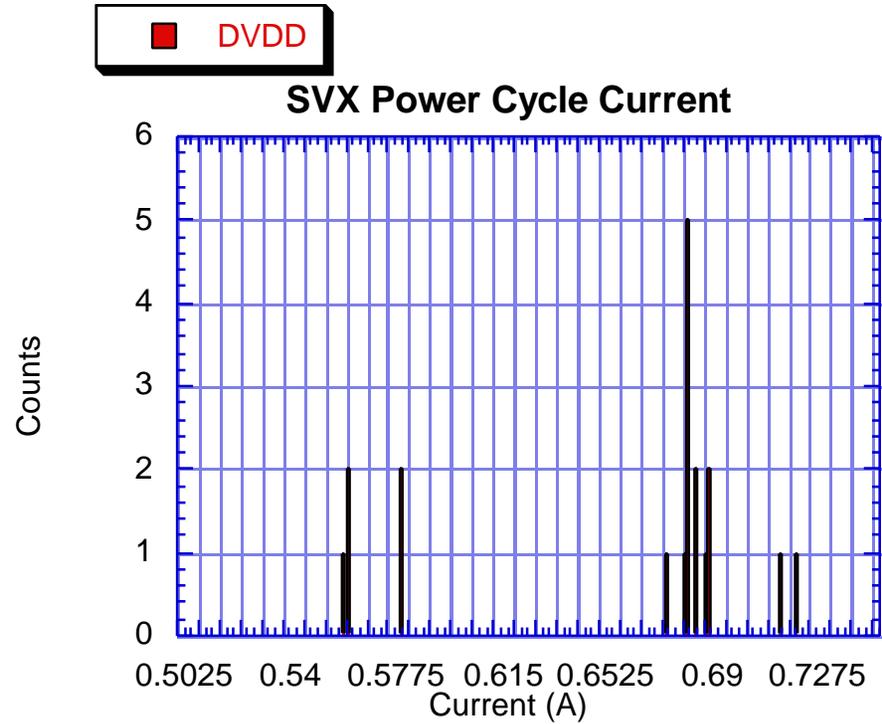


Figure 9: Summarization of statistics for DVDD.

Statistics	DVDD (A)	DVDD after Port Card	DVDD after Crate
Minimum	0.960	0.54000	0.55900
Maximum	1.30	0.70000	0.72000
Sum	21.1	12.472	12.473
Points	20.0	20.000	19.000
Mean	1.06	0.62360	0.65647
Median	1.07	0.65000	0.68200
RMS	1.06	0.62604	0.65872
Std Deviation	0.0810	0.056653	0.055794
Skewness	1.12	-0.26130	-0.95950

AVDD2 (3.0V)	20.3 ms	3.27 s
DVDD (5.2V)	24.8 ms	3.45 s

Figure 10: SVX power supply current without ramped supplies.

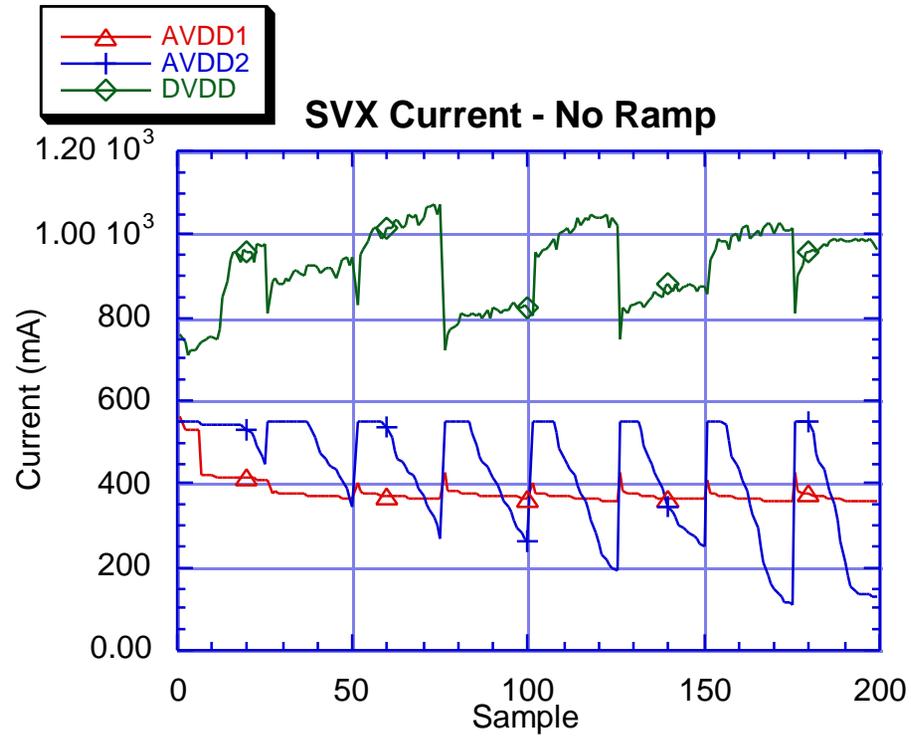
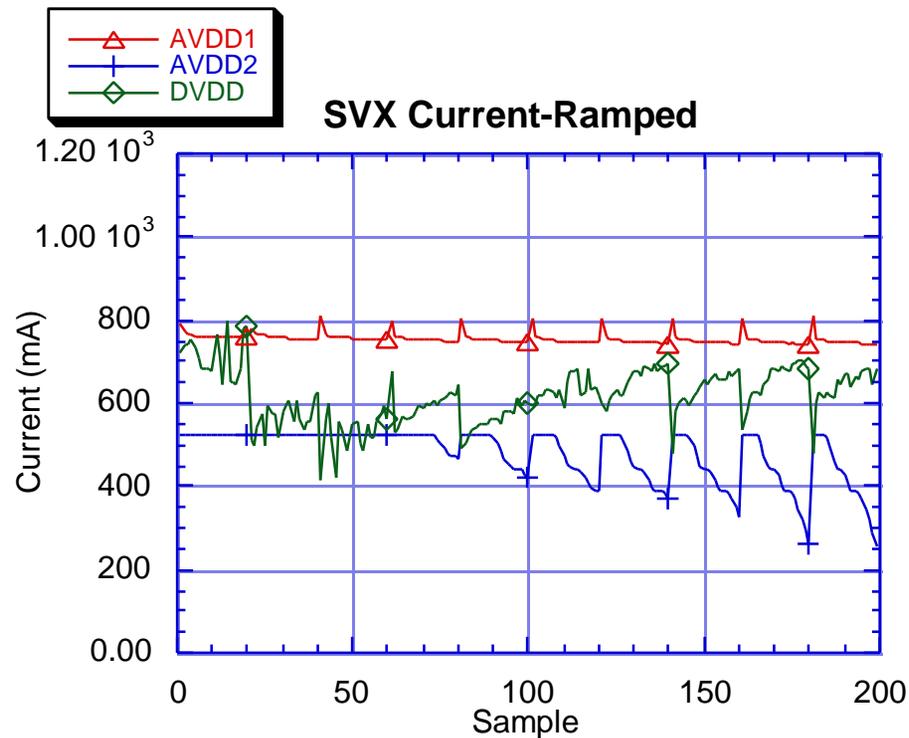


Figure 11: SVX power supply current using ramped supplies.



We discovered an interesting feature by taking several current samples during a given interval. We found that the AVDD2 current decreases over time. Long term data shows that this current eventually decays to ~6 mA at a rate of ~200 uA/s after a 45 s delay. Each upward trend of AVDD2 indicates the beginning of the next power cycle. These plots also show that DVDD tends to increase over time and AVDD1 decreases slightly and much more rapidly than AVDD2. These measurements were taken without the SVX chips downloaded.

Figure 12: Minimum and maximum current measurements with ramped and non-ramped supplies.

	Minimum Current (A)		Maximum Current (A)	
	No Ramp	Ramp	No Ramp	Ramp
AVDD1	.360	.739	.425	.810
AVDD2	.129	.230	.550	.526

nonramped, were taken with the same .5 second sample interval, the maximum current measurements for AVDD1 are twice as high when ramping the supply. AVDD2 remains approximately the same and DVDD is about 200 mA lower. More data needs to be taken to determine if ramping the supplies at a very slow rate will help or hinder the power requirements of the system.

There is a substantial difference in the power supply current when the Port Cards are downloaded. The following plots were generated from data taken without ramping the supplies. AVDD1 current increases 23 mA/chip when downloaded, DVDD decreases 38 mA/chip. AVDD2 current decreases from 32 mA on initial power-up to 26 mA after download, a difference of 6 mA.

Figure 13: SVX power supply current with and without download.

	Without Download		Downloaded	
AVDD1	424 mA	23 mA/chip	834 mA	46 mA/chip
AVDD2	572 mA	32 mA/chip	465 mA	26 mA/chip
DVDD	941 mA	52 mA/chip	259 mA	14 mA/chip
TOTAL	1.94 A	107 mA/chip	1.56 A	86 mA/chip

Figure 14: Power supply current without SVX downloaded.

5s sample interval
18 SVX chips

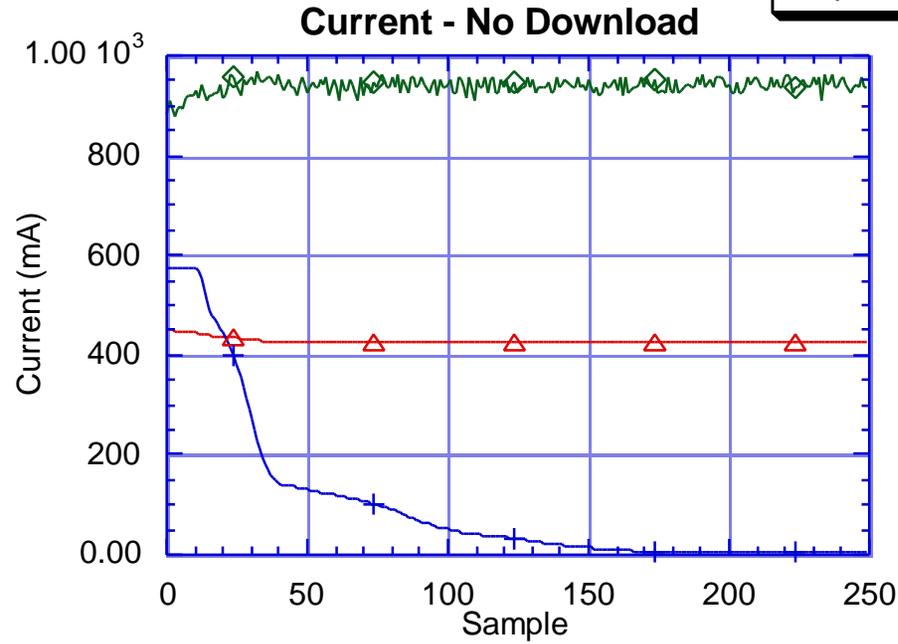
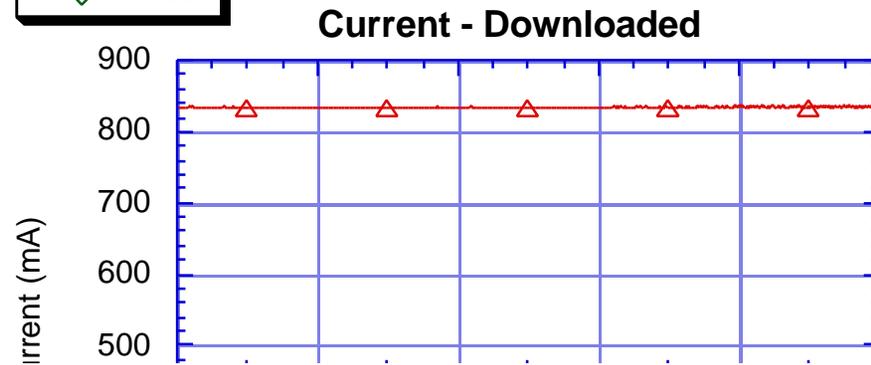
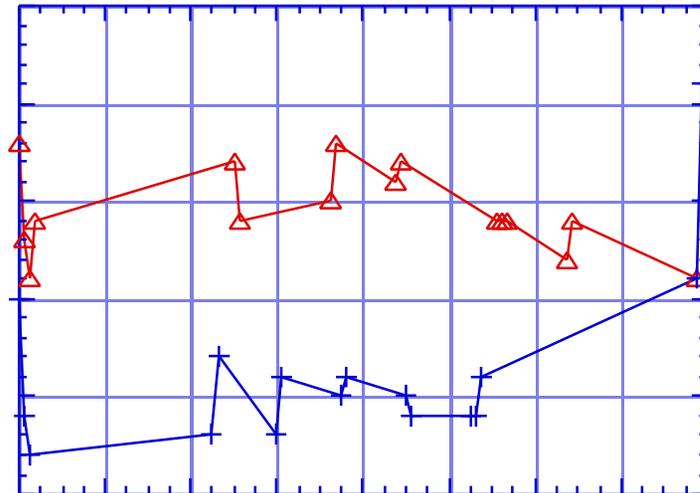


Figure 15: Power supply current with SVX downloaded.



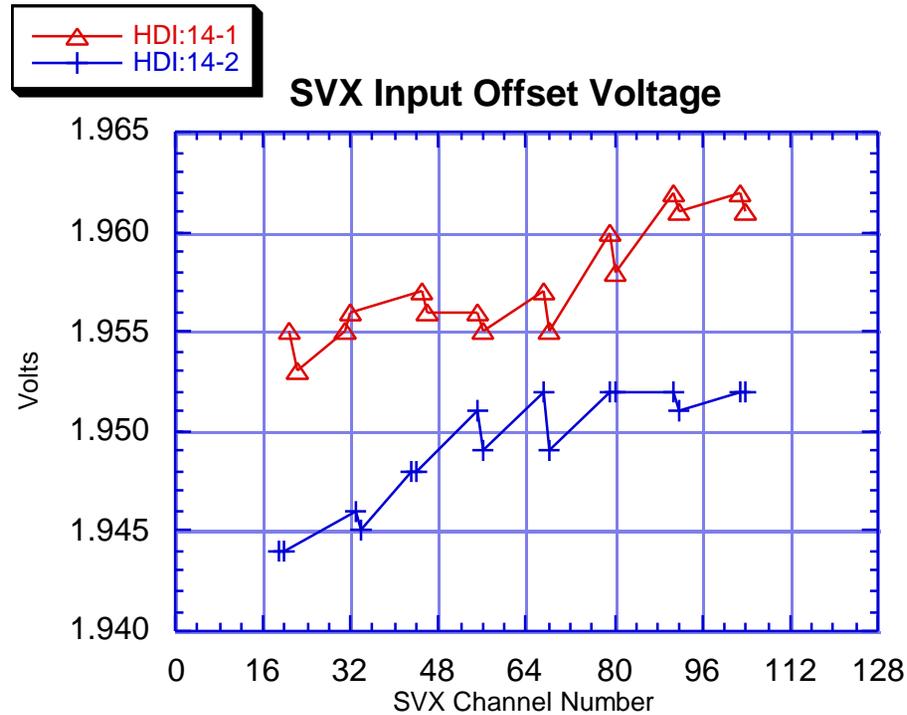
The SIFT (Scintillating Fiber Trigger) chip will provide a “fast” trigger for the D0 experiment. This device contains a preamplifier (Q out to SVX) and a discriminator which provides a 3V logic level trigger signal. At NWA the SIFT chips were temporarily installed between the VLPC detectors and the SVX. The SIFT chip has a CDS (Correlated Double Sample) feature which was meant to compensate for the SVX input offset voltage of $\sim 2\text{V}$. The thought was to bond one SVX input channel to a pin (VREF) of the SIFT. This signal provides the compensation for all 16 SIFT channels. The accuracy of the compensation then depends on the linearity of the offset voltages across the SVX. We measured the input offset voltage for 16 channels on 6 SVX chips, Figures 16-18.

Figure 16: High Density Interconnect #10 - SVX Input Offset Voltage



HDI #10-1 had the lowest variance of the 6 devices measured, 7 mV.
HDI #10-2 had a variance of 19 mV.

Figure 17: High Density Interconnect #14 - SVX Input Offset Voltage



The offset voltages tend to gradually increase from left to right on HDI #14. The variance for HDI #14-1 was 8 mV, HDI #14-2 was 8 mV. HDI #16-1 variance was 14 mV and HDI #16-2 was 23 mV.

Figure 18: High Density Interconnect #16 SVX Input Voltage Offset

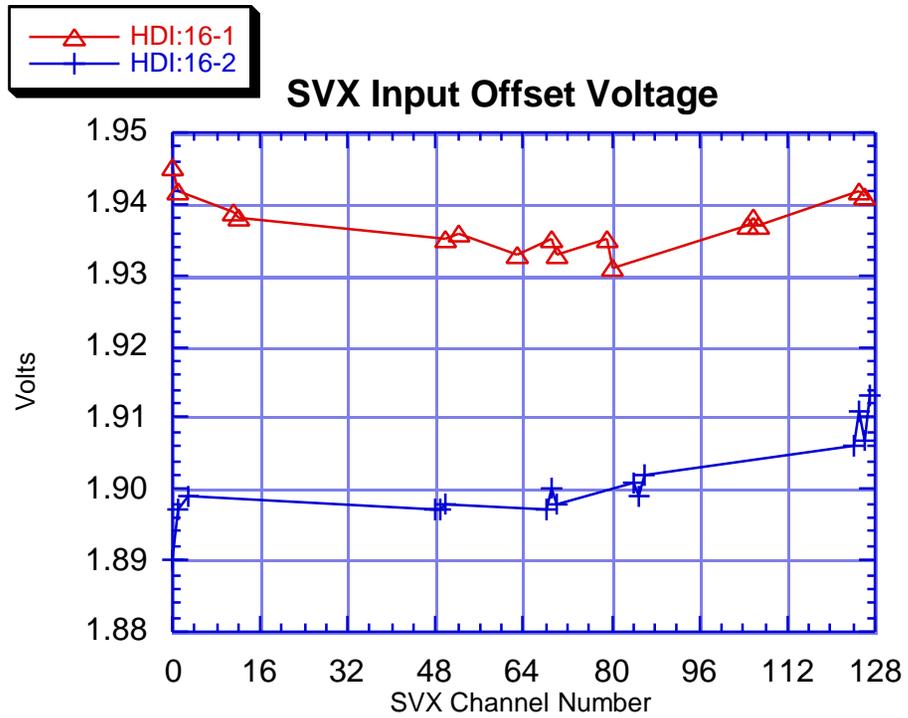


Figure 19: Average Offset Voltage with error bars for 16 channels per SVX chip.

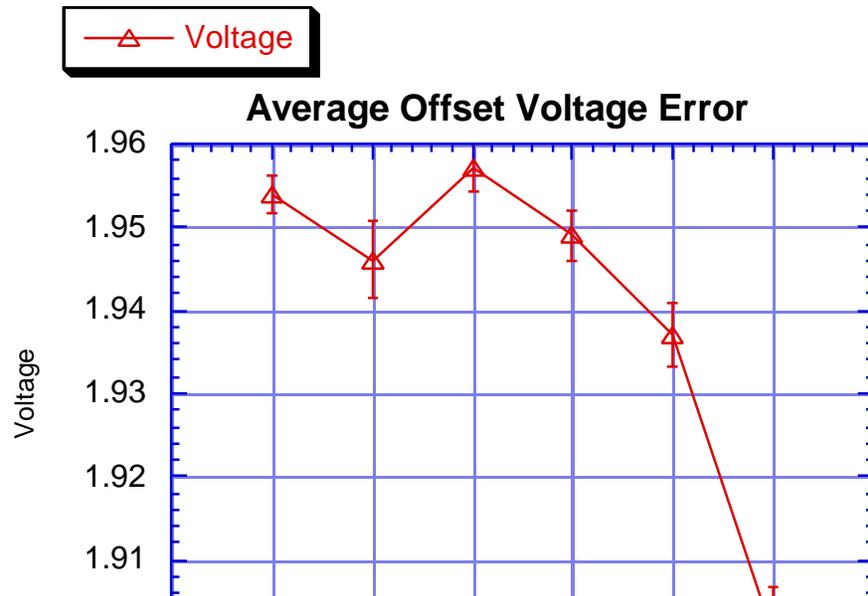
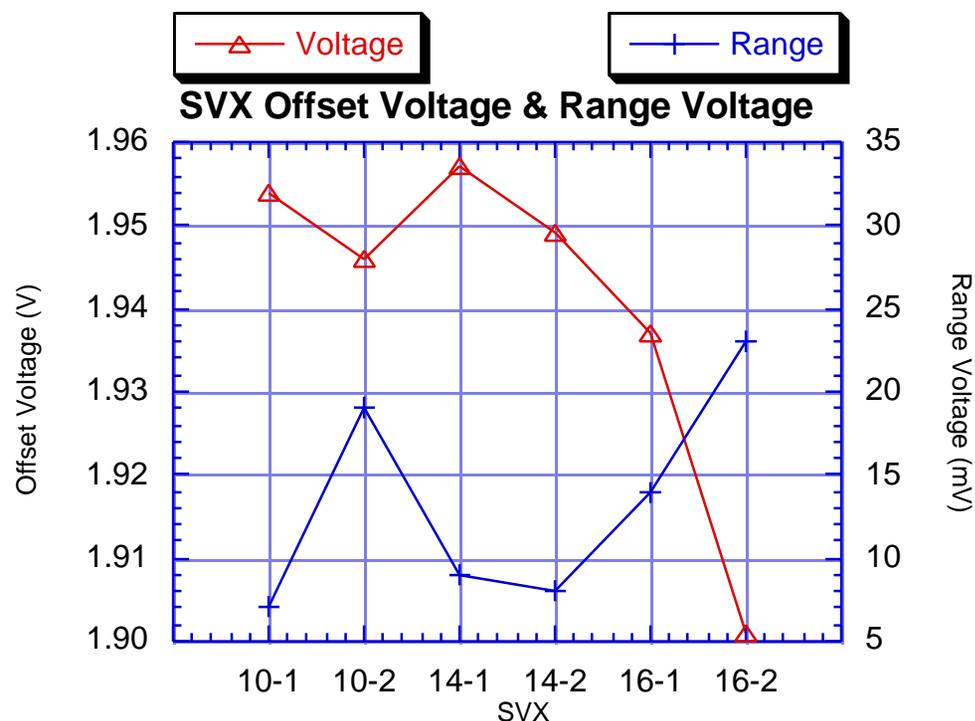


Figure 20: SVX Average Offset Voltage and Range Voltage per chip.



Summary

The run away current mode occasionally experienced at NWA could not be duplicated during this power supply current study. We found that the current associated with AVDD2 decreases at a rate of ~ 200 $\mu\text{A/s}$ ($11\mu\text{A/s/chip}$) when the SVX is not downloaded. AVDD1 and DVDD remain fairly constant at 23 mA/chip and 52 mA/chip. After the SVX has been downloaded the total current for the chip decreased by 21 mA/chip and is very stable. More studies need to be conducted to determine if ramping the supplies reduces the total current load prior to downloading the SVX chips.

The SVX input offset voltage measurements show that using one channel of an SVX to determine the compensation voltage for 16 SIFT channels is not acceptable. We measured as much as a 23 mV input offset voltage difference across one SVX. We are currently investigating the use of a sample and hold device which would sample each SVX channel connected to a SIFT chip. The sample and hold would be part of the SIFT chip. We plan to test this theory by incorporating a sample and hold device on the Multi-Chip