The VA1’

Specifications v0.92
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1 General

- Description:
  The VA1’ ASIC is a 128 channel low-noise/low power charge sensitive preamplifier-shaper circuit, with simultaneous sample and hold, multiplexed analogue readout and calibration facilities. The part is a pin compatible replacement for VA1.

- Application Areas:
  Silicon strip, or other semiconductor, detectors of higher capacitance (20-100 pF)

- Vendor:
  Ideas ASA
  Veritasveien 9, 1322 Høvik, Norway.
  Phone: +47-67 81 65 00
  Fax: +47-67 81 65 01
  e-mail: Sales@ideas.no, http:/www.ideas.no/

- Availability:
  Available as unpackaged, wafer tested dices or mounted on hybrids (dedicated or standard designs). Normal stock goods.

2 Physical

- Process: 0.8 µm N-well CMOS, double-poly, double metal.
- Die size: 6.12 mm x 4.04 mm, thickness: ~ 600 µm

Recommended chip pitch when several chips are mounted in cascade on a hybrid: 6.4 mm or more. That is; fits well with true 50 µm pitch strip sensors.

- Input bonding pads:
  Four rows. Normal connection to rows 1 and 2, redundant pads in rows 3 and 4.

  Pad size: 50 µm x 90 µm
  Pad pitch: 91.2 µm
  Row pitch: 170 µm (see. fig. 2&3)

- Output, control and power pads:
  Single row.

  Pad size: 90 µm x 90 µm
  Pad pitch: 200 µm (see fig. 2)

- Radiation hardness:
  1 Mrad
3 Electrical

Power rails:  \( V_{dd} = +2.0\, \text{V}, \ V_{ss} = -2.0\, \text{V} \)

Each with separate connections for analogue (avdd and avss) and digital sections (dvdd, dvss) of the chip.

Back contact:  metalized, connect to avss (-2 \text{V})

Current draw:  Quiescent (typical values):

- dvdd:  \(< 10 \ \mu\text{A}\)
- dvss:  \(< 10 \ \mu\text{A}\)
- avdd:  11.5 \text{mA}
- avss:  -73 \text{mA}
- gnd:  61.5 \text{mA}

Input bias currents:  Nominal values

<table>
<thead>
<tr>
<th>(all driven to devices (e.g. resistors) referred to avdd)</th>
</tr>
</thead>
<tbody>
<tr>
<td>pre_bias:  500 \mu\text{A}</td>
</tr>
<tr>
<td>sha_bias:  22 \mu\text{A}</td>
</tr>
<tr>
<td>ibuf:      140 \mu\text{A}</td>
</tr>
</tbody>
</table>

(ibuf only during readout)

Peaking time:  Nominal:  1\mu\text{s}

Adjustable:  1\mu\text{s} - 3\mu\text{s}

Power dissipation:  Typical values

Quiescent:  170 mW (1.3mW/ch)  Minimal:  68 mW

1 at this conditions performance may vary from nominal specs
ESD Protection: Inputs: None
Analogue out p & m: None
Controls (include shift out b): 
~ 300Ω series resistor and protection diodes to Vdd and Vss.

Input stage: Input device: PMOS referenced to gnd
Signal input potential: ~ -1.2 V to -1.3 V

Gain: ~ 12.5 mV/fC nominal with differential outputs each driving 500 Ω. Current gain is about 10 µA/fC. The gain depends on setting parameters like VFS, Sha_bias etc.

Linear range: ± 35fC (approx ± 10 MIP in 300um Si) (can handle both signal polarities) 70fC in single polarity can be used with adjustment of VREF.

Noise (ENC): Typical values:
180 + 7.5/pF e_rms for 1 µsec peaking time
165 + 6.1/pF e_rms for 2 µsec peaking time

Readout: Controlled via 128-bit (output) shift register.
Analogue outputs (outp, outm) of two or more chips can be connected in parallel to drive the inputs of an external, differential, transimpedance amplifier.
Max. read-out is 10 MHz, here care has to be taken not to load the output buffer with too high capacitance and resistance.

Calibration/test: Voltage step applied via external 1.8 pF capacitor to the cal-input. 2 mV step represents 3.6fC.
(1 MIP in 300um Si = 22400 e⁻ or 3.6 fC).
Some additional noise has to be taken into account in test mode due to serial resistance and additional capacitance.
Calibration signal can be given to one channel in a given chip at a time. The channel is selected via a 128-bit (input) shift register.
4 Pad Description

The output, control and power pads are listed below from top to bottom. (see chip plot on next page (Fig. 1.)

<table>
<thead>
<tr>
<th>Pad name</th>
<th>Type</th>
<th>Description</th>
<th>Nominal value</th>
</tr>
</thead>
<tbody>
<tr>
<td>gnd</td>
<td>p</td>
<td>signal ground</td>
<td>0 V</td>
</tr>
<tr>
<td>dvdd</td>
<td>p</td>
<td>digital vdd</td>
<td>+2.0 V</td>
</tr>
<tr>
<td>dvss</td>
<td>p</td>
<td>digital vss</td>
<td>-2.0 V</td>
</tr>
<tr>
<td>delay_adjust</td>
<td>ai</td>
<td>not in use</td>
<td></td>
</tr>
<tr>
<td>delay_on</td>
<td>di</td>
<td>not in use</td>
<td></td>
</tr>
<tr>
<td>holdb</td>
<td>di</td>
<td>used to hold analogue data, see fig. 3</td>
<td>Logical</td>
</tr>
<tr>
<td>dummy (hold)</td>
<td>di</td>
<td>*)</td>
<td>Logical</td>
</tr>
<tr>
<td>dreset</td>
<td>di</td>
<td>reset of digital part</td>
<td>Logical</td>
</tr>
<tr>
<td>dummy (dreseth)</td>
<td>di</td>
<td>*)</td>
<td>Logical</td>
</tr>
<tr>
<td>shift_in_b</td>
<td>di</td>
<td>start pulse for read-out</td>
<td>Logical</td>
</tr>
<tr>
<td>dummy (ck)</td>
<td>di</td>
<td>*)</td>
<td>Logical</td>
</tr>
<tr>
<td>ckb</td>
<td>di</td>
<td>clock for read-out register, see fig. 3</td>
<td>Logical</td>
</tr>
<tr>
<td>shift_out_b</td>
<td>do</td>
<td>Signalling end of read-out. Can be used as shift_in_b for next chip.</td>
<td>Logical</td>
</tr>
<tr>
<td>test_on</td>
<td>di</td>
<td>Turns chip into test-mode</td>
<td>Logical</td>
</tr>
<tr>
<td>avss</td>
<td>p</td>
<td>Analogue vss (+ chip backplane)</td>
<td>-2.0 V</td>
</tr>
<tr>
<td>pre_bias</td>
<td>ai</td>
<td>Bias current for pre-amplifiers.</td>
<td>500 µA</td>
</tr>
<tr>
<td>sha_bias</td>
<td>ai</td>
<td>Bias current for shaper-amplifiers.</td>
<td>22 µA</td>
</tr>
<tr>
<td>vref</td>
<td>ai</td>
<td>not in use. (recommended connected to decoupling capacitor).</td>
<td>Logical</td>
</tr>
<tr>
<td>ibuf</td>
<td>ai</td>
<td>Bias-current for output-buffer.</td>
<td>140 µA</td>
</tr>
<tr>
<td>outm</td>
<td>ao</td>
<td>Negative output signal (current)</td>
<td></td>
</tr>
<tr>
<td>outp</td>
<td>ao</td>
<td>Positive output signal (current)</td>
<td></td>
</tr>
<tr>
<td>vfs</td>
<td>ai</td>
<td>Control voltage to feedback resistance in shaper-amplifier</td>
<td>700 mV</td>
</tr>
<tr>
<td>vfp</td>
<td>ai</td>
<td>Control voltage to feedback resistance in pre-amplifier</td>
<td>-0.2 V²</td>
</tr>
<tr>
<td>cal</td>
<td>ai</td>
<td>Test input signal</td>
<td>1 MIP</td>
</tr>
<tr>
<td>avdd</td>
<td>p</td>
<td>Analogue vdd</td>
<td>+2.0 V</td>
</tr>
</tbody>
</table>

p = power, di = digital in, do = digital out, ai = analogue in, ao = analogue out

*) These ‘dummy’ signals are recommended for high performance. They should be used to add complementary signals to the effective ones in order to minimise digital signal-feedthrough to the analogue output.

2 see chapter ‘Useful Hints’
The VA1’ circuit.
Fig. 2 Chip geometry & pad placement (Not to scale - all dimensions in µm. Please note that the referred co-ordinates are layout co-ordinates. Add 50-100 µm on each side for scribe/cutting tolerances).

Fig. 3. Definition of input pad size and pitch.
5 Functional Description

As shown in Fig. 4 the chip consists of 128 identical parallel charge sensitive amplifiers. The output of all amplifiers enters corresponding inputs of a 128 channel multiplexer. The switches in the multiplexer are controlled by a bit-register which runs in parallel. The output of the mux. goes directly out of the chip via the output buffer (signal = ‘outp’ - ‘outm’). Only one of the switches in the mux can be “on” at a time. That is one amplifier (channel) at a time can be seen on the output of the chip. The bit in the register ripples in sequence from the top- to the bottom- channel by clocking ‘ckb’. The clock can be stopped at any point which will leave the connection between the current channel and the output, which remains enabled.

Fig 4. VA1’ Architecture
6 Normal mode of operation

The normal mode of operation is that the 128 inputs are connected to a detector from where the charge signal comes. After the physics event, each channel will integrate its eventual signal for 1µs. Usually, after the peak is reached (1µs), an external 'hold' signal should be applied to sample the value. Immediately after this a sequential read-out can be performed by activating the output bit-register using ‘shift_in_b’ and ‘ckb’. See fig. 5 for an example of the timing in this mode. The logic part of the chip can be reset either by applying the ‘dreset’ or, simply by running through a normal read-out once.

![Example Normal Readout Sequence of one chip](image)

**Fig 5. Read-out timing of VA1’**
7 Operation in test mode

Each of the inputs of the amplifiers can be accessed via the input pads on the left side, see Fig. 4. In test mode, it is not necessary to connect any of these. Instead, the test facility of the chip can be turned on (‘test-on’). This will enable another mux./bit-register on the input to run exactly in parallel with the output mux./bit-register. This input mux. connects all the inputs to the ‘cal’ pad via a switch controlled by the bit-register. Also, in this case, only one connection at a time is possible and this connection will always correspond to the same channel as is connected in the output mux.

Fig. 6: VA1 circuits on a ceramic-PCB hybrid board
8 Useful hints

Use of ‘cal’-input
When the ‘cal’-input is used in test mode an external capacitor (as close as possible to the pad) should be connected in series before the signal enters into the ‘cal’ pad. A capacitor value of 1.8 pF is recommended. A voltage step of 2 mV gives hence an input signal charge of 3.6 fC (~ 1 MIP).

Generation of bias-currents/-voltages
Fig. 7. shows a possible approach for generating the necessary bias currents and voltages.

Adjustment of VFP
VFP adjusts the feedback resistor of the pre-amplifier. Lower values result in a higher feedback resistor thus at too negative values the pre-amplifier will stop working.

Termination of outputs
Fig. 8 shows a possible solution for termination of the outputs ‘outm’ and ‘outp’.

Decoupling of power and bias lines
It is recommended to decouple the power and bias lines to GND.

9 Bias current generation

![Fig 7. Bias current & Voltage generation](image1)

![Fig 8. Analogue-Out termination](image2)

- Document Nr. VA1’ version 0.92 date 03May2004.
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