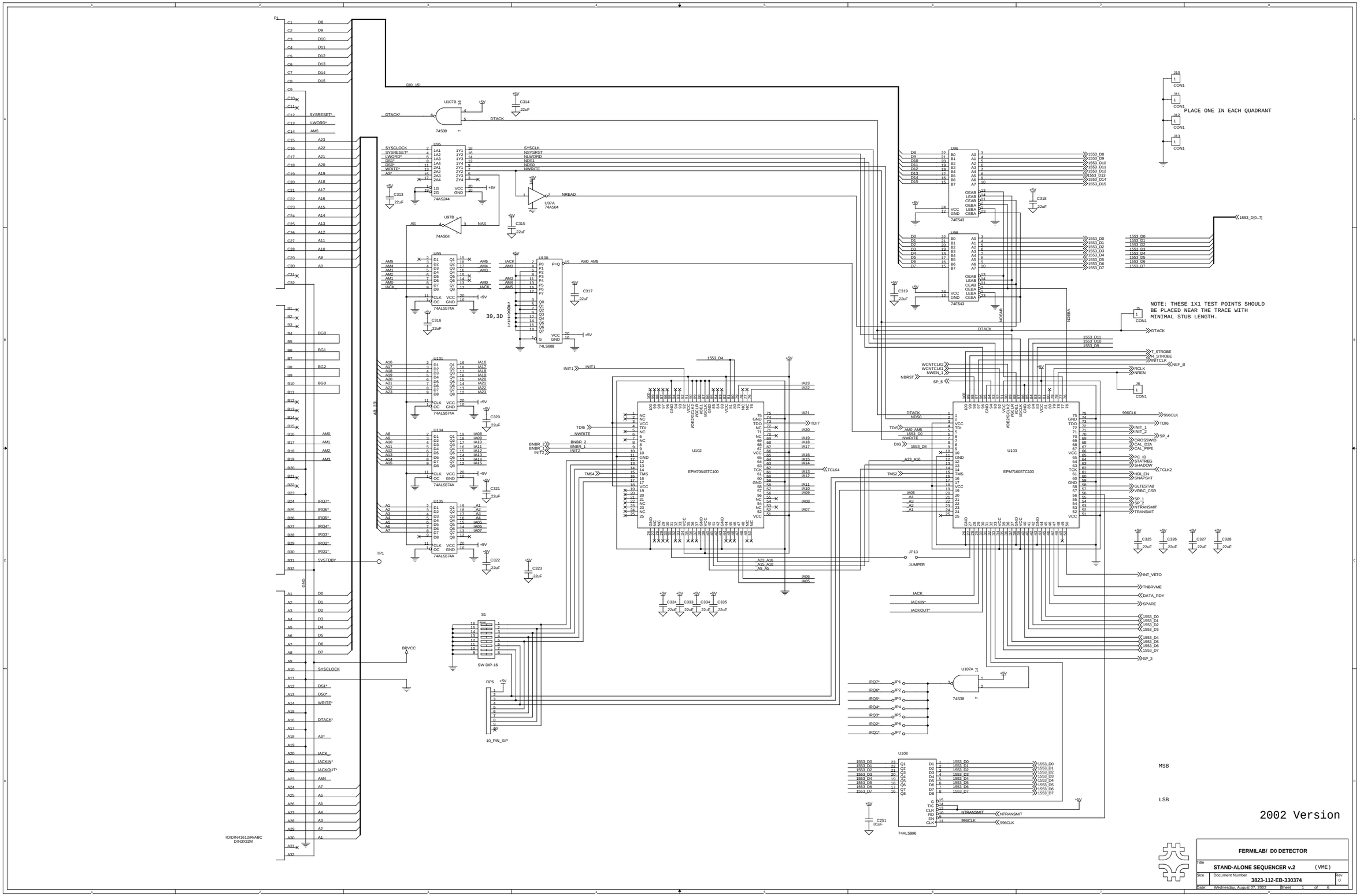
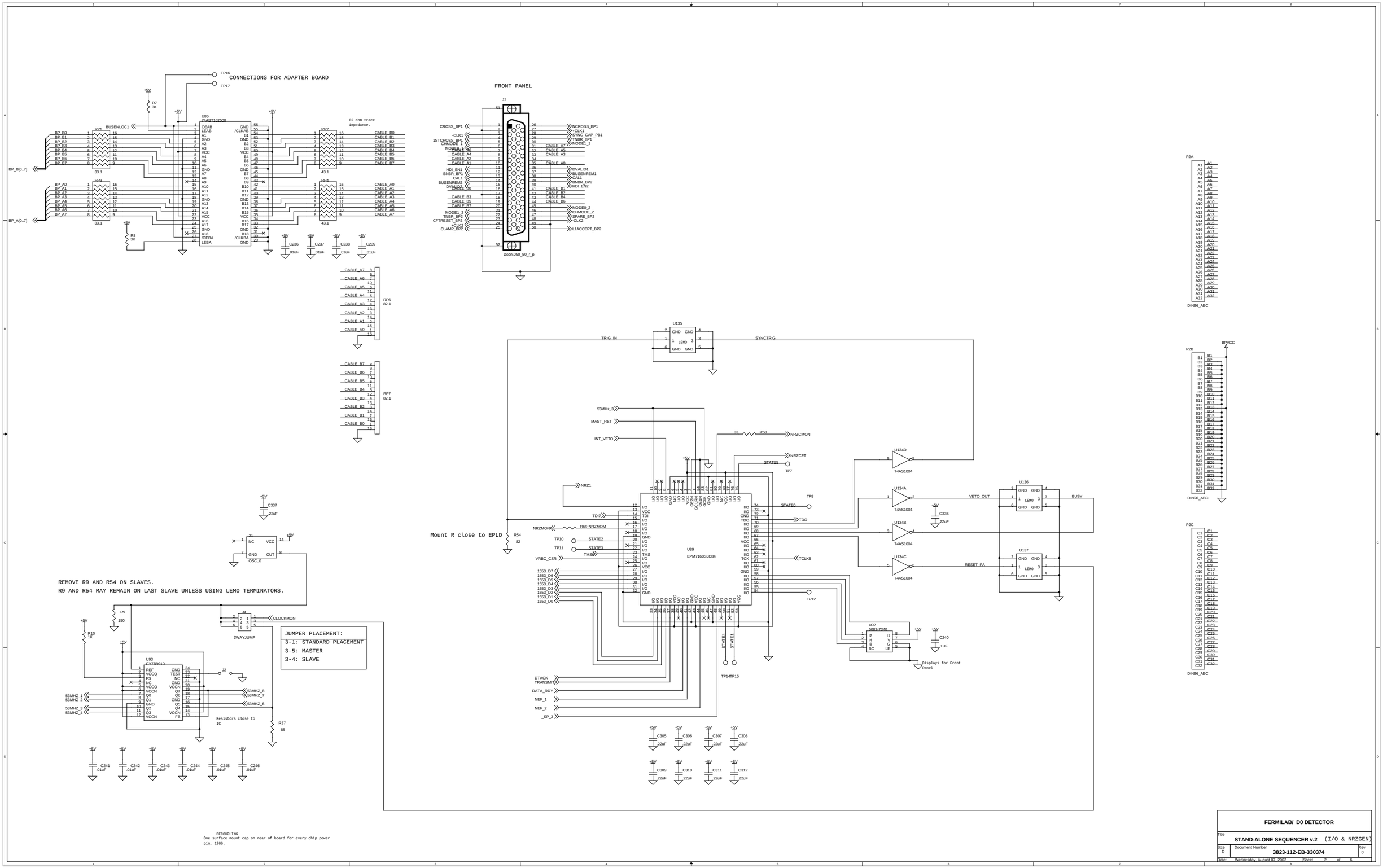

PLACE ONE IN EACH QUADRANT
NOTE: THESE 1X1 TEST POINTS SHOULD BE PLACED NEAR THE TRACE WITH MINIMAL STUB LENGTH.
39,3D
EPM7064STC100
EPM7160STC100
74F543
74LS688
74ALS574A
74AS244
74AS04
74AS38
74ALS996
SW DIP-16
10_PIN_SIP
JUMPER
MSB
LSB
2002 Version
FERMILAB/ D0 DETECTOR
STAND-ALONE SEQUENCER v.2 (VME)
3823-112-EB-330374
Wednesday, August 07, 2002
VME


CONNECTIONS FOR ADAPTER BOARD
TP16
TP17
U86
74ABT162500
BUSENLOC1
RP1
RP2
RP3
RP4
33.1
43.1
82 ohm trace impedance.
BP_B[0..7]
BP_A[0..7]
CABLE_B0
CABLE_B1
CABLE_B2
CABLE_B3
CABLE_B4
CABLE_B5
CABLE_B6
CABLE_B7
CABLE_A0
CABLE_A1
CABLE_A2
CABLE_A3
CABLE_A4
CABLE_A5
CABLE_A6
CABLE_A7
R7 3K
R8 3K
C236 .01uF
C237 .01uF
C238 .01uF
C239 .01uF
RP6 82.1
RP7 82.1
FRONT PANEL
J1
Dcon.050_50_r_p
CROSS_BP1
-CLK1
1STCROSS_BP1
CHMODE_1
MODE1_1
HDI_EN1
BNBR_BP1
CAL1
BUSENREM2
DVALID1_NO
MODE1_2
TNBR_BP2
CFTRESET_BP2
+CLK2
CLAMP_BP2
NCROSS_BP1
+CLK1
SYNC_GAP_PB1
TNBR_BP1
MODE0_1
DVALID1
BUSENREM1
CAL1
BNBR_BP2
HDI_EN2
MODE0_2
CHMODE_2
SPARE_BP2
-CLK2
L1ACCEPT_BP2
P2A
DIN96_ABC
P2B
DIN96_ABC
P2C
DIN96_ABC
BPVCC
U135
TRIG_IN
SYNCTRIG
LEMO
53MHz_3
MAST_RST
INT_VETO
R68
NRZCMON
NRZCFT
STATE5
TP7
TP8
STATE0
TDO
TCLK6
TP12
NRZ1
TDI7
NRZMON
R69 NRZMOM
TP10
STATE2
TP11
STATE3
TMS7
VRBC_CSR
1553_D7
1553_D6
1553_D5
1553_D4
1553_D3
1553_D2
1553_D1
1553_D0
U89
EPM7160SLC84
STATE4
STATE1
TP14TP15
DTACK
TRANSMIT
DATA_RDY
NEF_1
NEF_2
_SP_3
Mount R close to EPLD
R54 82
U134D
U134A
U134B
U134C
74AS1004
VETO_OUT
RESET_PA
BUSY
U136
U137
C336 22uF
U92
5082-7340
Displays for Front Panel
C240 1UF
C337 22uF
X1
OSC_0
REMOVE R9 AND R54 ON SLAVES.
R9 AND R54 MAY REMAIN ON LAST SLAVE UNLESS USING LEMO TERMINATORS.
R9 150
R10 1K
J4
3WAYJUMP
CLOCKMON
JUMPER PLACEMENT:
3-1: STANDARD PLACEMENT
3-5: MASTER
3-4: SLAVE
U93
CY7B9910
J2
53MHZ_1
53MHZ_2
53MHZ_3
53MHZ_4
53MHZ_8
53MHZ_7
53MHZ_6
Resistors close to IC
R37 85
C241 .01uF
C242 .01uF
C243 .01uF
C244 .01uF
C245 .01uF
C246 .01uF
C305 22uF
C306 22uF
C307 22uF
C308 22uF
C309 22uF
C310 22uF
C311 22uF
C312 22uF
DECOUPLING
One surface mount cap on rear of board for every chip power pin, 1206.
FERMILAB/ D0 DETECTOR
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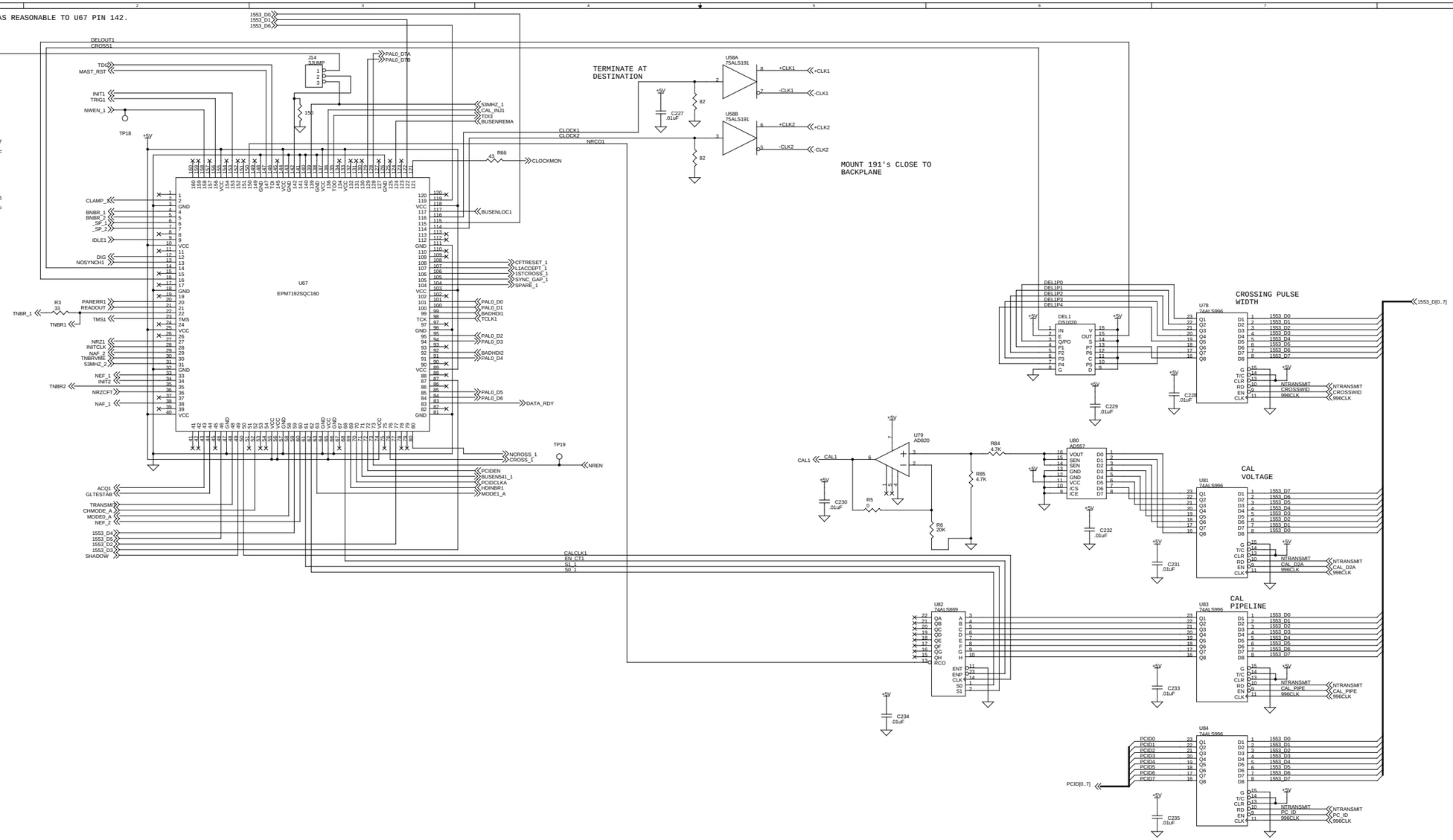
PLEASE PLACE 3JUMP AND OSCILLATOR AS CLOSE AS REASONABLE TO U67 PIN 142.



FERMILAB/ D0 DETECTOR	
Title: STAND-ALONE SEQUENCER v.2 (CONTROL)	
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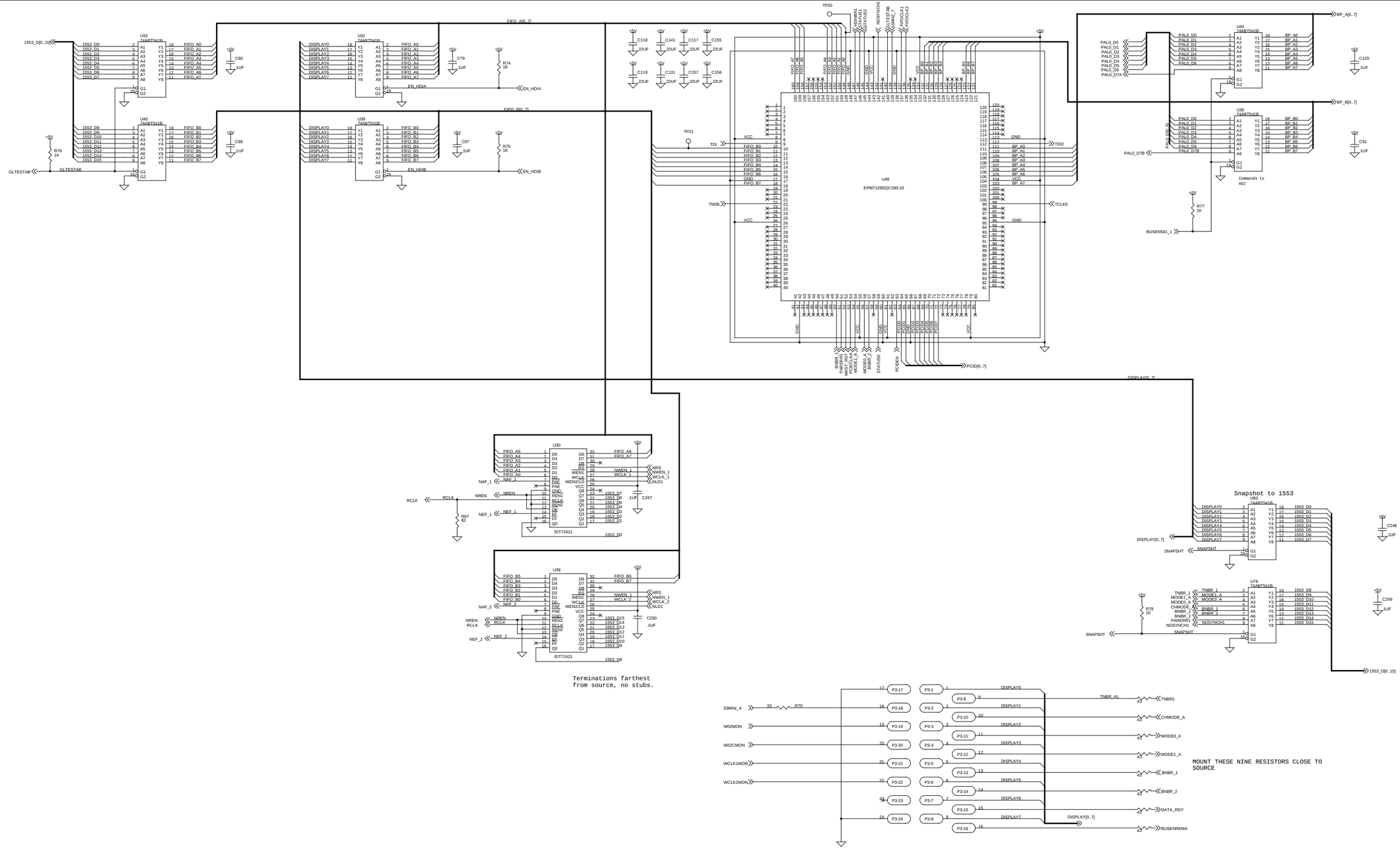

FERMILAB/ D0 DETECTOR

Title: **STAND-ALONE SEQUENCER v.2** (DATAPATH)

Size: D | Document Number: **3823-112-EB-330374** | Rev: 0

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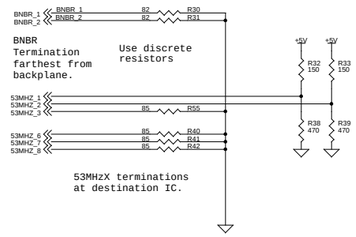
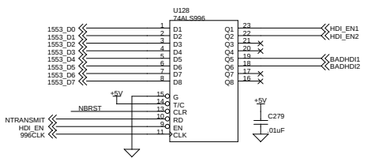
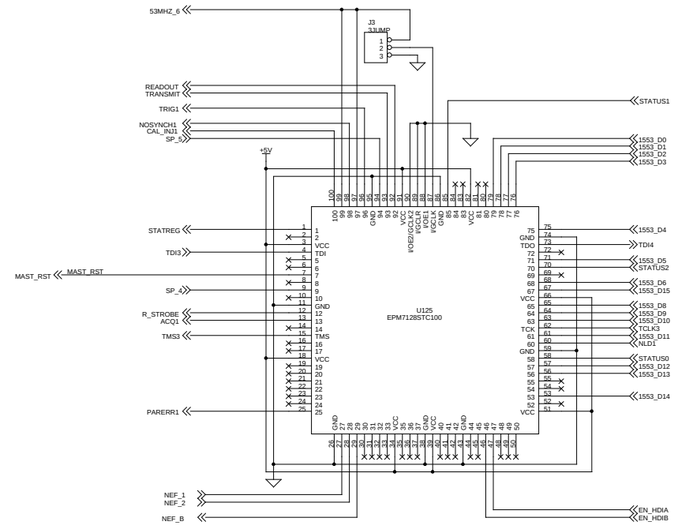
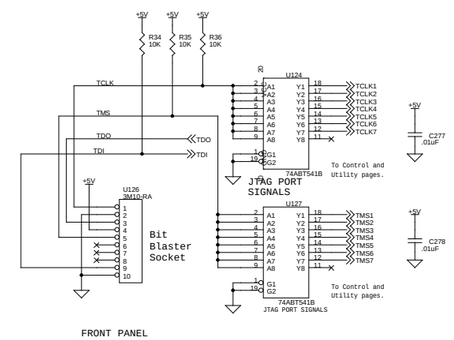
Generates RESETs, selects the HDI that goes to the Logic Analyzer, etc

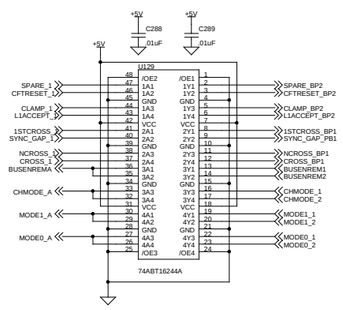
Controls Status Bits that show up in the Port Card's Status Word.

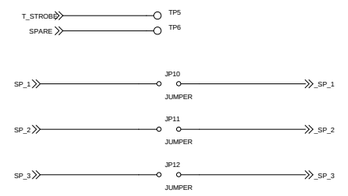


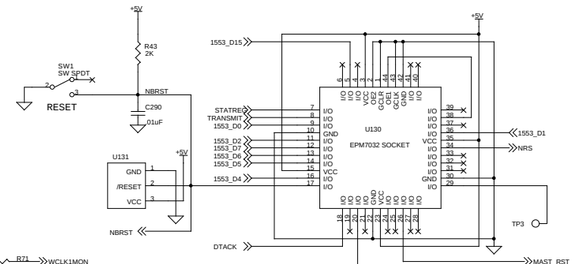


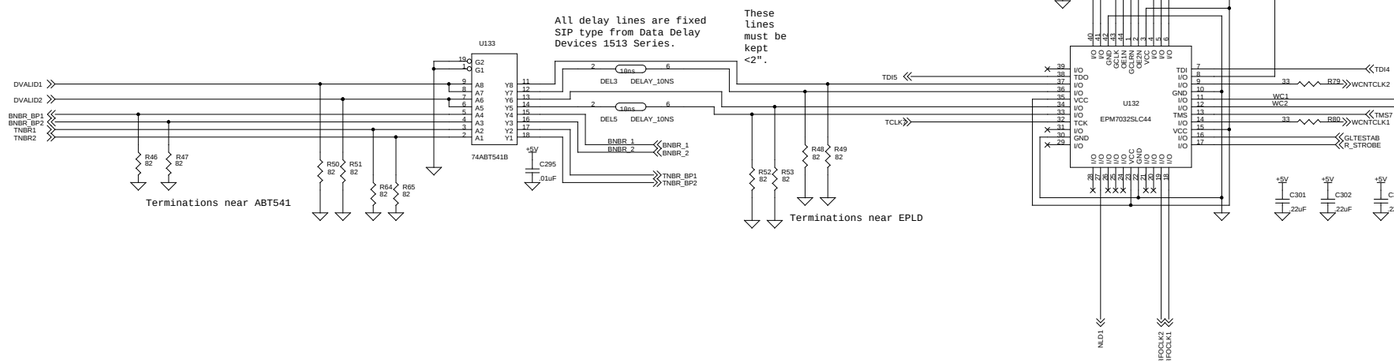












FERMILAB/ D0 DETECTOR	
Title	STAND-ALONE SEQUENCER v.2 (UTILITY)
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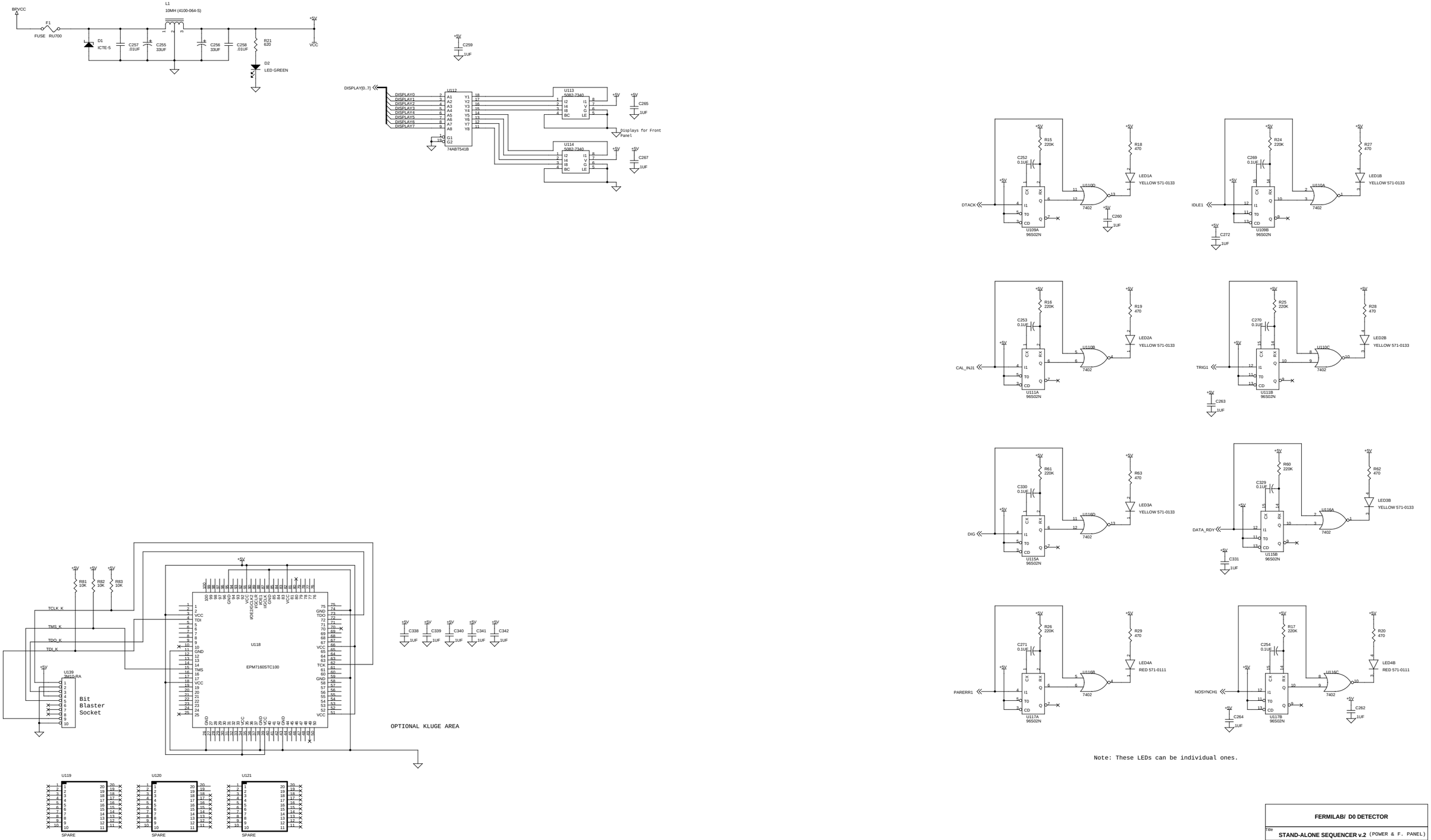

Note: These LEDs can be individual ones.

FERMILAB/ D0 DETECTOR	
Title: STAND-ALONE SEQUENCER v.2 (POWER & F. PANEL)	
Size: D	Document Number: 3823-112-EB-330374	Rev: 0
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