

# Zeroes in data

- Improper power levels
- Wrong polarity bit setting
- Bad pipeline readout sequence
- Chip needs to be downloaded
- Chip is exposed to light
- Grounding problems/noise
- Wrong ADC pedestal/Ramp rate
- Temperature dependence
- Needs Idle mode before Acquiring

# Unstable Pedestals

- AVDD too low
- AVDD2 dependence?
- Crossing Width set too low
- Pipeline settling time too short
- Improper grounding
- Needs Idle mode before going to Acquire
- CHMODE not straddling Mode line changes
- Sampling too soon after a Preamp Reset
- Reasons yet to be found

# Pedestals jump to high value and stay

- Ring Counter problem: Make chip go to IDLE after readout and before going to Acquire
- Increase the width of Acquire Clock.

# Noisy data

- AVDD too low
- AVDD2 dependence?
- Acquire clock high time too short,  
(adjust Crossing Width)
- Improper grounding
- Bad digitize clock
- Reasons yet to be found

# No Download?

- No Chip power
- Talking to wrong subaddress
- Poor Hirose Connection
- TNBR not  $> 2.5$  V
- Cable length problem
- Bad fuse
- Probe: TNBR, CLKs, Mode lines, BNBR

# No Readout?

- Probe Chip: Bus lines, TNBR, CLKs, DVALID, CHMODE, MODE1, MODE0, BNBR
- 5us per chip readout?
- If data and DVALID are present, probe Sequencer FIFO
- If not, check chip power, Hirose connections, fuses
- Check for proper setting of Ignore register
- Check for proper SVX control signals from Sequencer (as in Beginner's Guide), if bad try another Sequencer channel
- Also check Sequencer voltage, +5V, -5.2V
- Check NRZ phasing. Rising edge of CLK should occur between 2ns before and 7ns after a rising or falling edge of NRZ. (Prototype front panels have NRZ/CLK labels reversed)
- Correct VRB channel chosen?
- Restart spreadsheet
- Readout of Chip ID only (=80) indicates no download (clock or Tnbr) or no shadow pulse. Check for corrupted spreadsheet, Subad A.

# No Readout in Sparsify Mode

- In the CFT system it was found that the phasing of the digitize clock with respect to one or more SVX control signals had an effect on whether the chip would fail to read any channels in sparsify mode.

# Improper readout

- **Channel ID errors:**
- WCLK (DVALID) occurs at wrong time
- Wrong setting of Glink speed range on either Sequencer or VTM
- poor connections
- bad SVX chip
- Improper voltages
  
- **More data being read than expected from chips:**
- VRBC setup incorrect
  
- **Channel 7F data output on bus for three bytes:**
- DIGITIZE mode slightly too short
- Needs to be in Digitize for 22 NRZ states

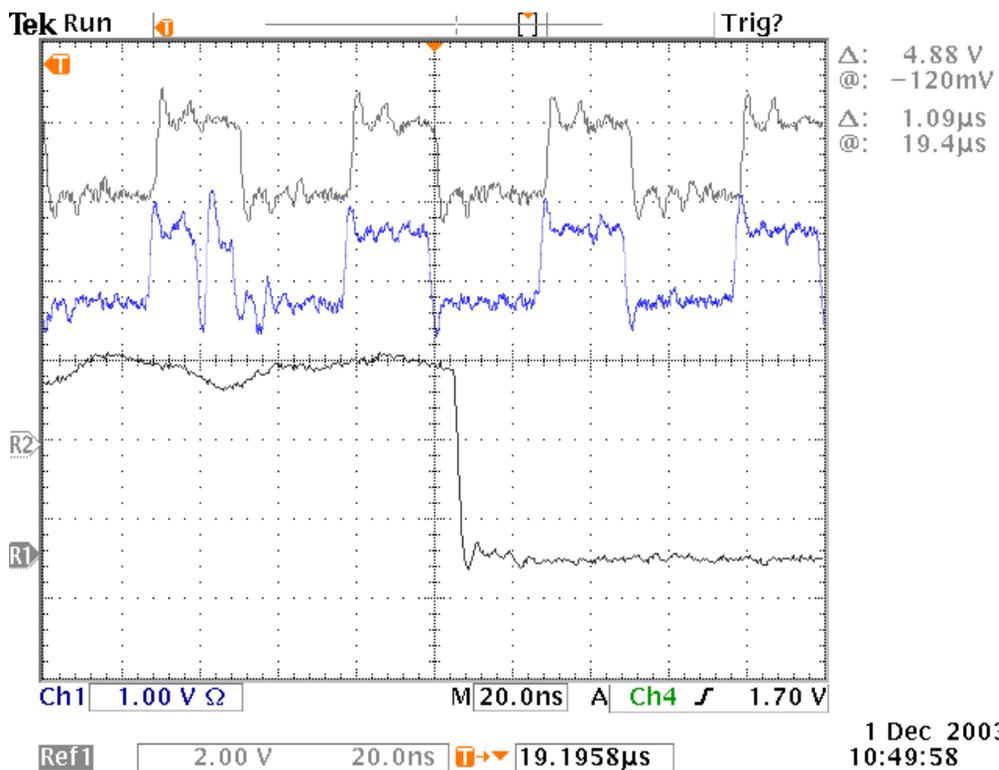
# Flying Geese

## **Channel IDs and Data reversed, caused by the Gray-decoding of monotonically increasing channel IDs**

- WCLK (DVALID) occurs at wrong time; this timing error could come from a variety of causes.
- Poor DVALID quality leads to occasionally one missed WCLK into FIFO
- Rare SVX bug whereby it skips one channel ID during readout. This is most often seen when the data value for that channel ID is the same number as the channel ID itself.

# Early end of readout

- Caused by a glitch in the readout clock going to the SVX



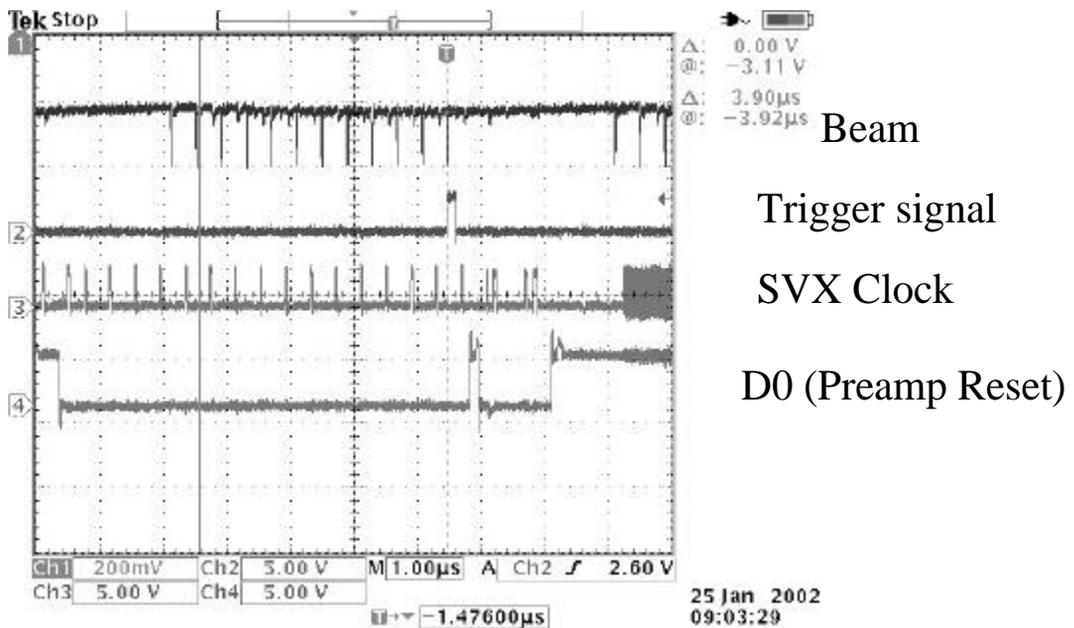
Blue trace is SVX clock, Bottom trace is the resultant Priority-Out.

# Channel ID 40 reads back as 00

- This problem occurred when we used 74F543 transceivers as buffers for the SVX chip. The problem was cured by changing to 74ABT543s. It sometimes occurred to channel 41<sub>hex</sub> which read back as 01<sub>hex</sub>. It is likely that the problem occurred during FIFO collapse since this byte of data was stable for the full byte duration. The mechanism for this error is still not known.

# No charge seen in correct pipeline

- **Cause: Presence of Preamp Reset (data line D0) occurs near end of Acquire cycle, adversely affecting “ring counter.”:**



- **Fix logic to prevent preamp reset during this time**

# Double Pedestals

- Make sure that, at the chips, CHMODE straddles changes in mode lines
- Sampling too soon after a Preamp Reset
- Lengthen IDLE mode before Acquire mode.

# Charge being shared by two adjacent pipelines

- Lengthen the IDLE mode after Readout and before Acquire mode.
- Make sure CHMODE pulses are wide enough after readout and entering Acquire mode.
- Possible explanation: Two adjacent pipeline switches are operating in Acquire mode, caused by unwanted chip currents occurring because Acquire mode was not entered properly.

# Other Peculiarities

- Very sensitive to clock edge quality
- Amplitude of inputs must be  $> 1/2$  DVDD
- Needs DIG clocks after Readout mode
- Likes Initialize mode before Acquire mode
- Needs good AVDD for stable pedestals
- Needs cap on Ramp Ref pad
- Needs time to recover from Preamp reset
- Photons erase output FIFO

## Data Readout 0x00

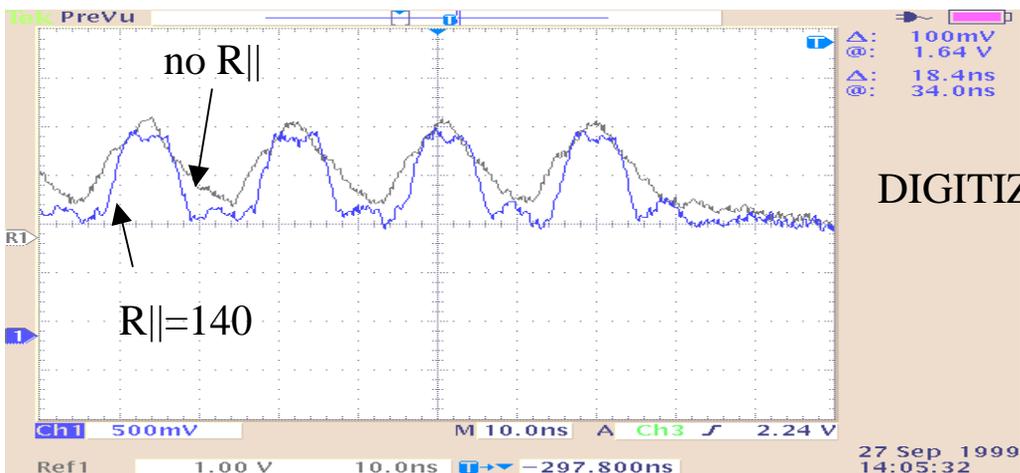
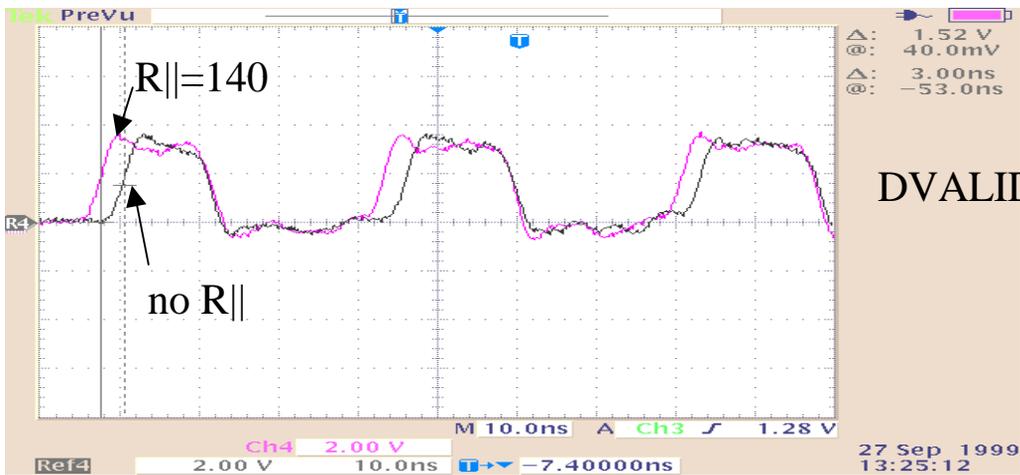
At the 10 % Test we normally ran by forcing the readout value from the SVX to hex 65 by setting counter modulo to 65 and adjusting ADC pedestal and ramp for high output, but we randomly obtained readout 0x00 from the SVX. Sometimes it occurred on a few channels, sometimes whole chips. Many things were tried: chip voltage dependence, filtering power supplies, temperature dependence, chip sensitivity to light, grounding problems at the sequencer backplane connector, etc. Finally the problem was traced down to a download mistake (spreadsheet corruption) in the CompPol bit. This behavior is still not understood.

## Channel ID and Data reversed after Channel 1C of First Chip

There is a good chance that the Almost Full flags of the Sequencer's FIFOs have not been set. The most common cause has been the initialization programs setting these flags separately for the top half and bottom half of the board. Since the reset line (necessary for the FIFOs prior to setting these flags) is common to both halves, the second reset prior to loading the flags for the second half of the board wipes out the flag settings for the first half. The proper procedure is to write to subaddress 9 for both halves of the board (both RTs), then write the values to subaddresses 14 and 15 for both halves of the board, then write bit D14 and bit D09 low for both halves.

# Too narrow DVALID

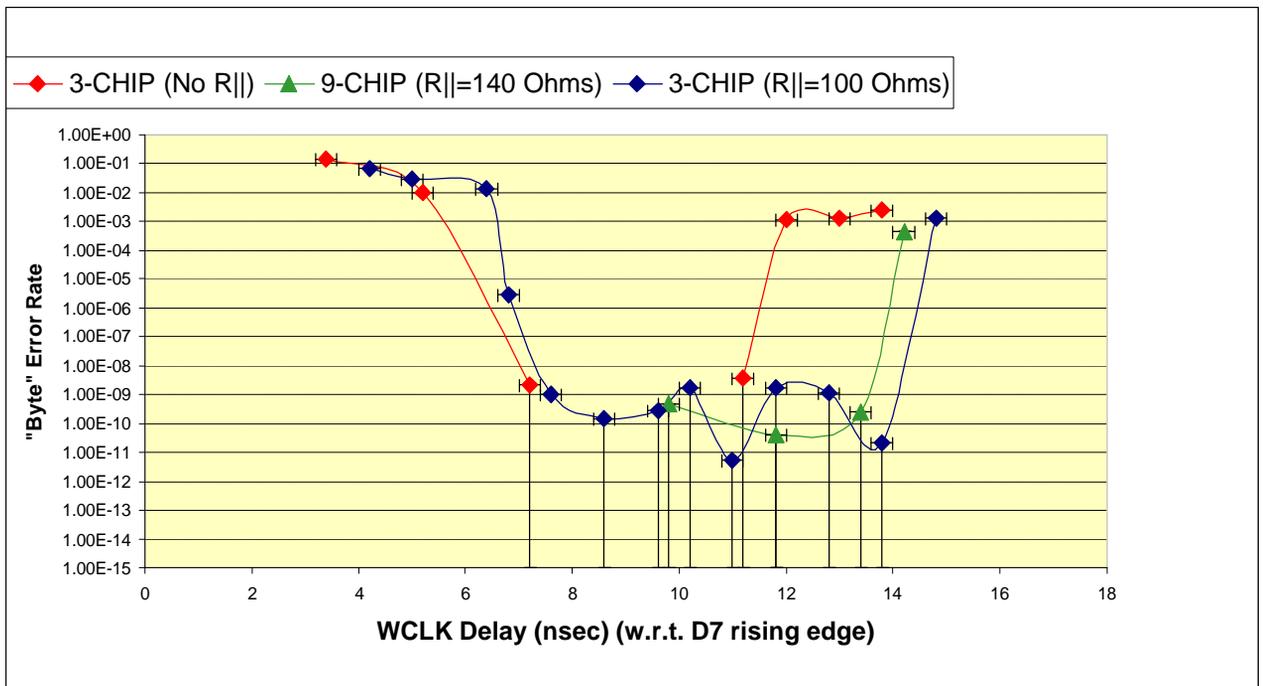
1st few DVALID cycles delivered by the SVX narrower than nominal 18.8 ns (at 53 MHz). One of the reasons is bad CLK quality for unterminated CLK line. 1st DVALID width improves from 11ns to 14ns by adding 140Ohm parallel resistor between CLK-CLKB at HDI. Still 1st DVALID narrower than nominal. Associated with SVX driver limitations when trying to drive the 75 Ohm data bus at beginning of readout. Improvement by CLK and/or data bus precharging only marginal.



# Data Strobing at Sequencer FIFO

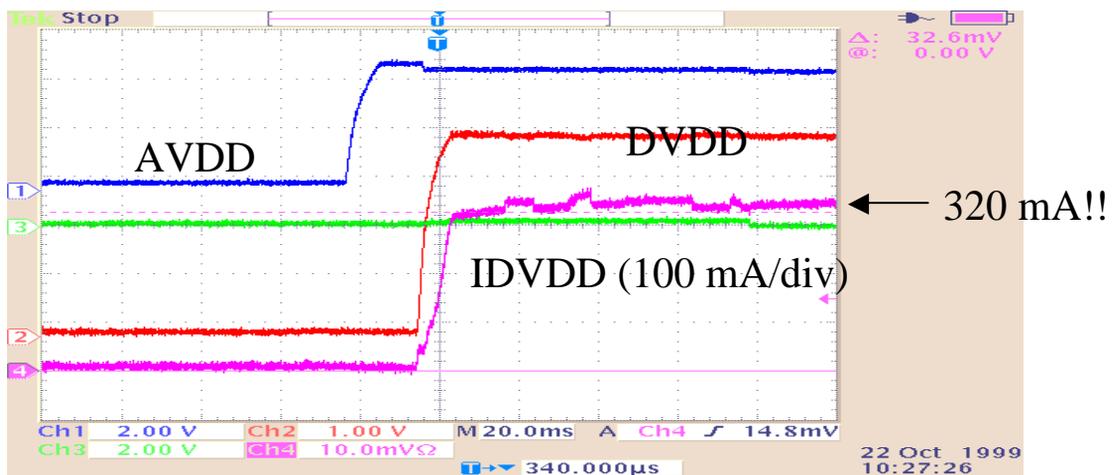
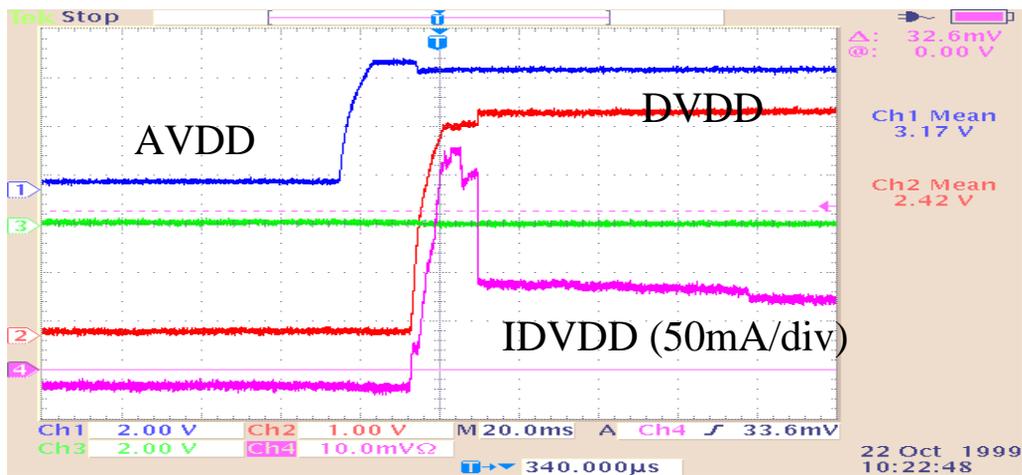
Significant improvement in dynamic range for data strobing at the sequencer FIFO by properly terminating CLK lines at the HDI ( $R_{||} = 140$  Ohms between CLK-CLKB).

1st DVALID width lower for a 9-chip HDI as compared to a 3-chip HDI presumably due to larger capacitive load.



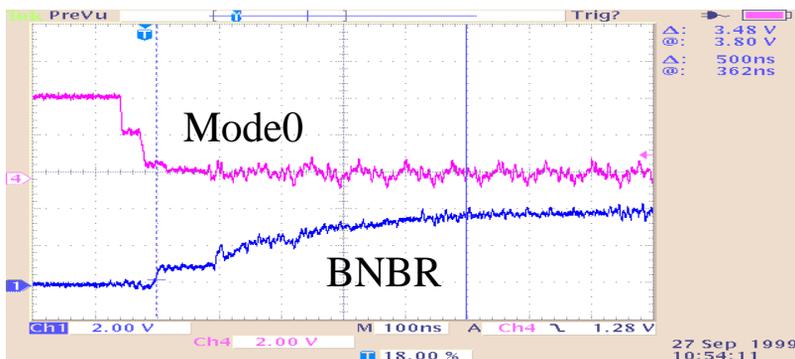
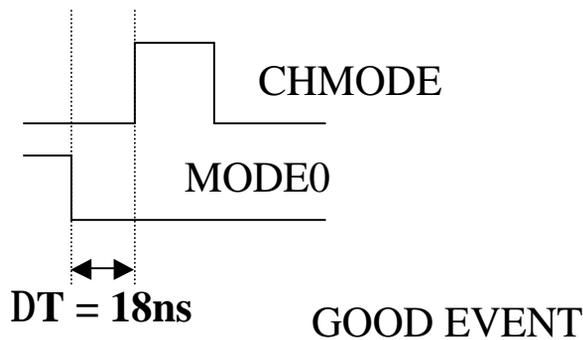
# SVX current draw

Large IDVDD draw at turn on. Seems to be a chip feature.  
For instance, for a 9-chip HDI onto low-mass cable:

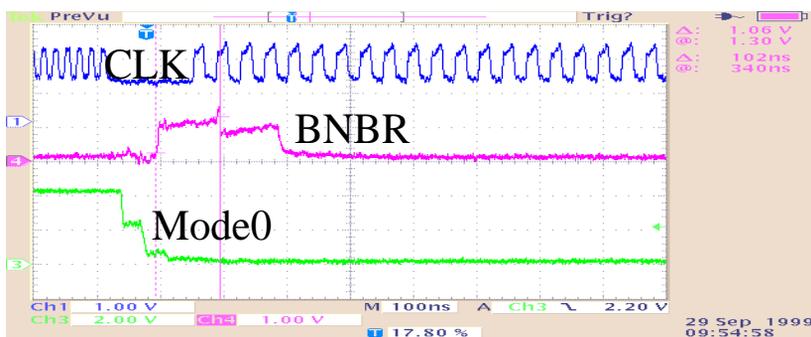


# BNBR problem

Aborted readout (BNRB goes LOW) just ~100ns after strobing readout. Typically happening in the first 1-2 events after power-up (high DVDD current mode). Need BNBR comparator threshold at KSU IB low enough so as to not get stuck, because the chip will recover by itself if it is allowed to get next readout. Can also happen if readout not properly strobed. This is cured by moving the CHMODE pulse AFTER the falling edge of MODE0:



## BAD EVENT



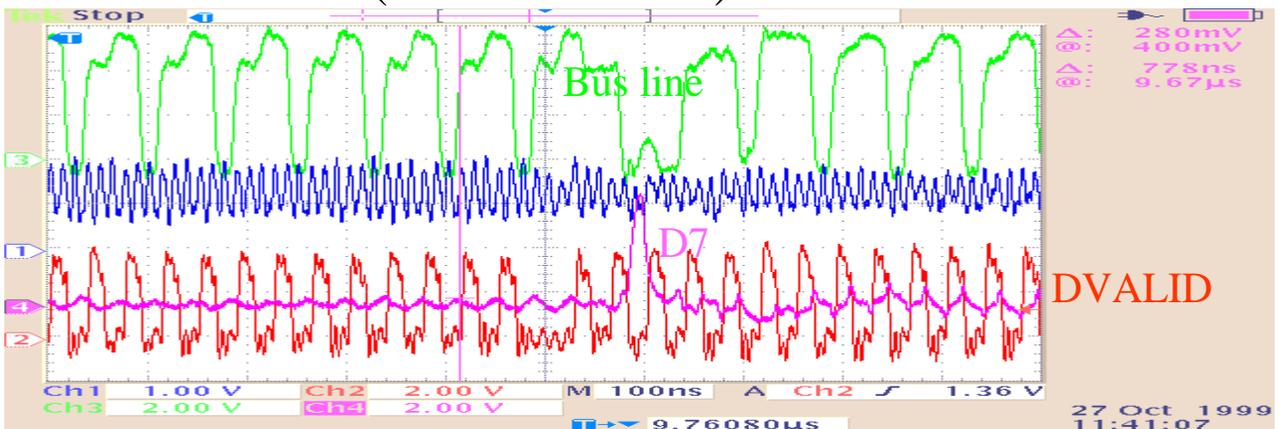
This problem can also be cured in some cases by starting the digitize clock before dropping ramp reset and counter reset.

# PERPETUAL READOUT problem

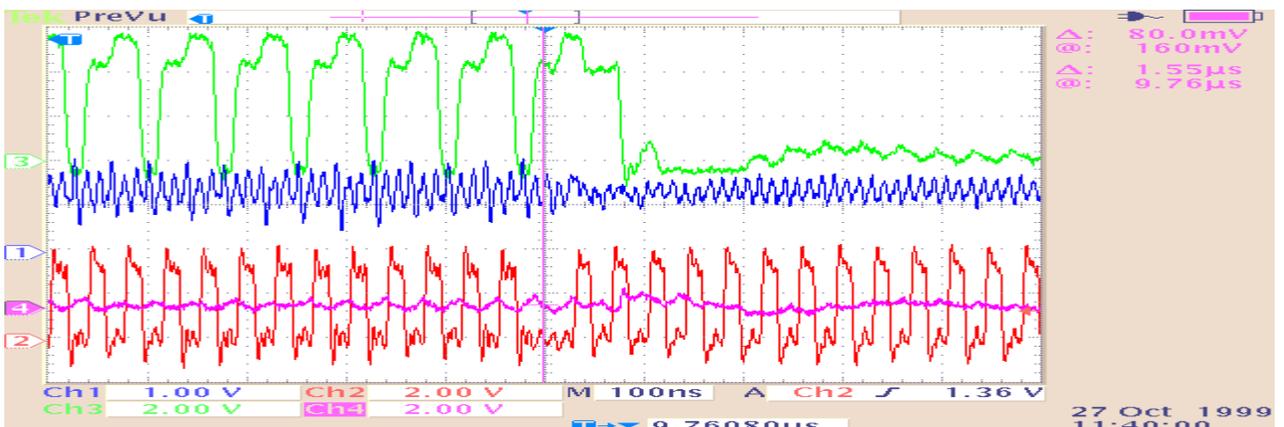
Chip will enter in perpetual readout mode due to failure in properly strobing DIGITIZE. Had to lower series resistance for CHMODE and MODE1 at KSU IB sending end in order to get sharper edges. However, the real fix was to extend CHMODE falling edge by +18.8 ns with respect to nominal. The failure was observed when increasing DVDD (changing thresholds at SVX receiver).

## 9-chip HDI readout at beginning of 3rd chip

Normal readout (DVDD=4.70 V)

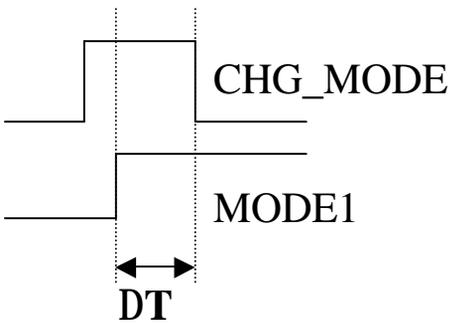
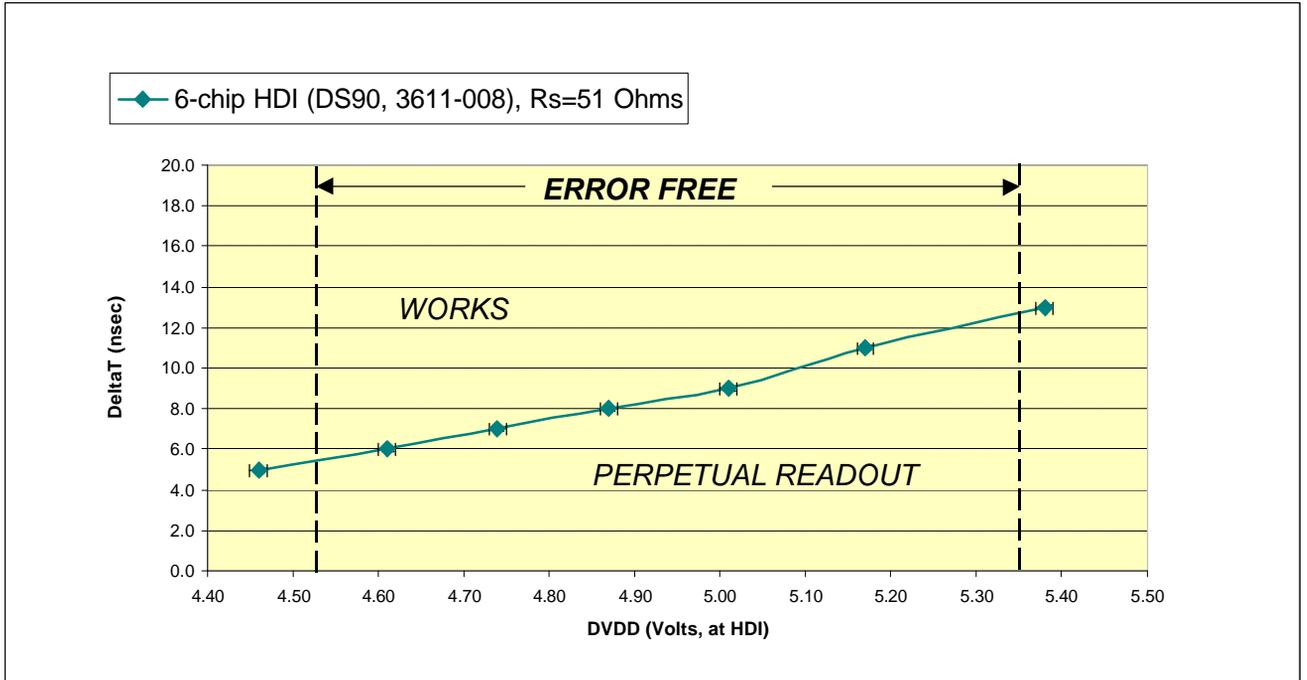


Perpetual readout (DVDD=4.85 V)



# PERPETUAL READOUT problem (cont'd)

To prove that it is a timing problem...

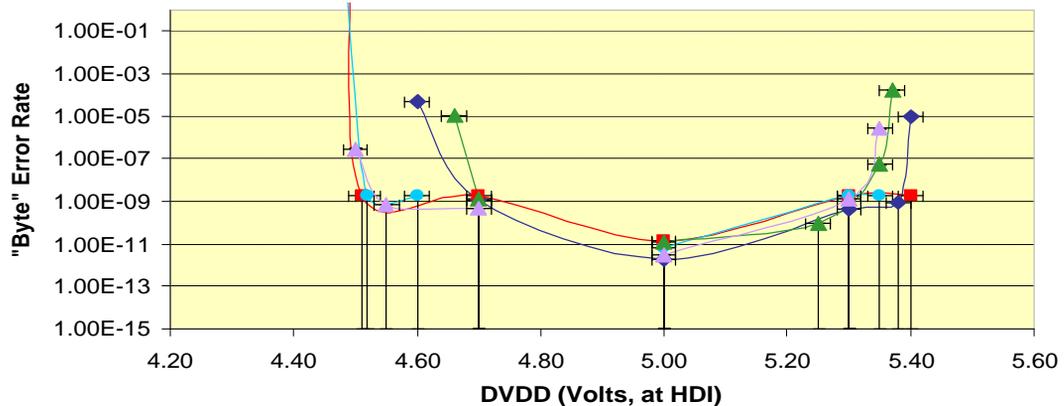


# DVDD range

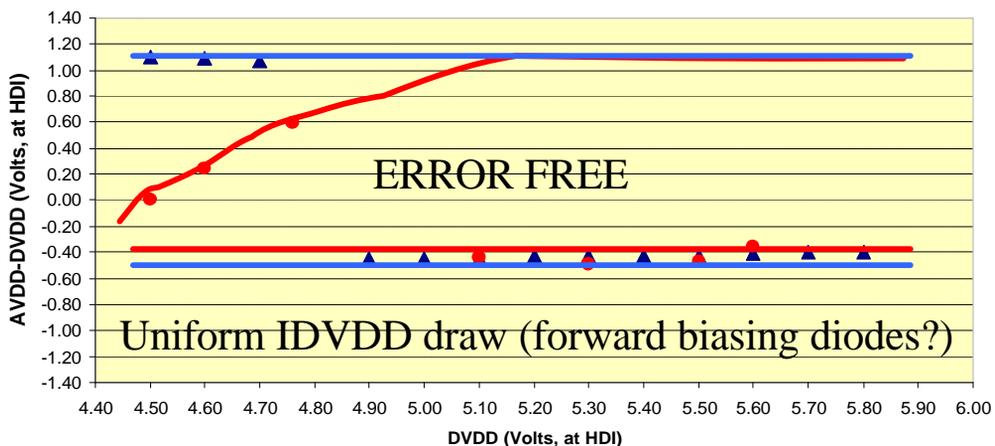
Finite DVDD operating range (after fixing BNBR and PERPETUAL READOUT problems) for the digital part of the chip (we run with fixed data, with normal pedestals the operating range might be different, need to study it).

**Rs = 51 Ohms for CNTRL lines at IB, AVDD = 5.0 Volts (at HDI)**

- ◆ 9-chip HDI (3953-35), R|| = 140
- 6-chip HDI (H-DISK, 116-C-J3), R|| = 140
- 6-chip HDI (DS90, 3611-008) R|| = 140, doubled CHG\_MODE
- ▲ 6-chip HDI (F-DISK, FA-008), R|| = 140
- ▲ 8-chip HDI (F-DISK, FA-023), R||=140



- ▲ 3-chip HDI (R||=140), Rs=51
- 9-chip HDI (R||=100), Rs=51



# Beginner's Guide

- Please refer to the Beginner's guide for some of the other figures used in this discussion.
- <http://www-d0.fnal.gov/~lipton/svx2e/svxe.html>