

- ? Enter readout with first chip PRI_IN high; PRI_IN must remain high for 2 clocks under readout high; issue 1st chip PRI_IN low after beclk falling edge—avoid early bus driver enable; emulates correct chip-to-chip operation; avoid corrupted data if 1st chip has only a high-address hit in sparse mode
- ? In contrast to the above entry, we saw that if the falling edge of Priority_In is late at the beginning of Readout mode, the first chip will not read out Channel 127 and its data.
- ? Exit readout before raising PRI_IN—potential for chips to assert OE and DVOE
- ? Change modes only around beclk rising edge, not falling edge—avoids metastable address register
- ? Rd63 --- avoid potential data corruption due to asynchronous condition created in data fifo when read sparse with only a high-address hit (?)
- ? Upward curve in pedestals fixed by making clock under PRD2 wider.
- ? Double reads of channel 7F in sparse mode—slow readout frequency to 48 MHz or set bit to force read of Channel 63.
- ? Zeroes in data -- Need enough digitize clocks to reach data value; otherwise get zero.
- ? Zeroes in data -- PRD2 not present in beam gaps
- ? Bipolar pedestals - - PRD2 not present in beam gaps
- ? Zeroes in data - - PA_RST not present in beam gaps
- ? Bipolar pedestals - - PA_RST not present in beam gaps
- ? Power oscillation at end of readout mode --
- ? Noisy pedestals - - have at least 590ns before falling edge of Ramp_Rst
- ? Cal Inject disappear - - PRD2 edge too near Acquire clock
- ? Initializing chips produces all ones (FFFF) during readback. - - AVX connector on HDI tail could be rotated 180 degrees.
- ? Zeroes in data OR No SVX readout - - Polarity of CLK and /CLK reversed.