# The HDI Recovery Effort

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## Introduction

On August 30, 2006 part of the D-Zero Trigger Framework tripped off. During the next few minutes the crew in the control room noticed high current alarms in many of the SMT High-Density Interconnects. The part of the Trigger Framework that failed is responsible for providing the silicon detector electronics with "heartbeat" pulses, each pulse causing an acquisition cycle to occur in the electronics. These pulses are needed in order to prevent the SVX chip from entering a mode where it draws large currents on the DVDD power line. After this incident, there were 41 additional HDI's that didn't download or read out data. An effort began to determine what happened and to devise a recovery plan if possible.

After months of investigation following the incident, we determined that the most common failure was either a fused or broken wire bond that carried +5 Volts to the DVDD pad of one of the SVX chips on the HDI. A large portion of these failures were in the last chip in the readout chain. The cause of the high chip currents was a system clock failure, which caused a large increase in chip current. Part of the increase in chip current came from the known current increase when there are no clocks. This known current increase is not sufficient to fuse the chip wire bonds. The precise mechanism for the added current to fuse the wire bonds is not known.

All inputs on the SVX 2 chip have protection diodes to prevent damage from Electrostatic Discharge (ESD). The data bus and mode control line diodes go to the DVDD power bus so it occurred to us that we might be able to use the data bus lines to restore power that was lost due to the broken wire bond. Extensive bench tests showed that this does work so we designed a new Adapter Card using FET switches and some logic to intercept bus lines D0, D1, D4, D5 and Mode_1 and apply +5 Volts to these lines instead of the typical TTL high level they normally see.

There are four operating modes in the SVX 2. In three of the modes (Initialize, Acquire, and Digitize) the new adapter card provides enough power on DVDD to completely operate the chip. In Readout mode there is enough power to pass priority so long as the chip is in sparse data mode and has a high threshold so that readout is suppressed. This allows the readout of any chips on the HDI that are downstream of the failed chip.

Section I describes the design features of the SVX 2 which cause the high current draw with no clock. Section II gives the evidence for a power wire bond failure as the cause for a large number of SVX 2 failures. Section III describes the alternate powering method and the new adapter card. Section IV describes the increased noise caused by the new adapter cards and the solution to the noise problem and Section V presents the results of the 2007 shutdown repair effort.

# I. High Current Draw on the DVDD power line

The SVX 2 chip has had a history of large current draw on the digital supply (DVDD) both at initial turn on and also during normal running when no readout cycles occur (the "loss of clock" problem). All of these problems can be traced to the use of CMOS dynamic memory in the readout section and operating the chip at low temperature.

Dynamic memory in CMOS devices refers to the use of a capacitor to hold the state of a flip flop rather than transistor gates. Fig. 1 shows a sketch of a dynamic CMOS gate. Charge is stored on the capacitor during one half of a clock cycle and evaluated on the second half of the clock cycle. That is, the top transistor conducts during the first half of the clock cycle and puts charge on the capacitor. On the second half of the cycle, the bottom transistor conducts. If the logic is such that the flip flop should be 0, the logic also conducts and the charge is drained off the capacitor leaving it in logic state 0. Otherwise the charge remains on the capacitor leaving it in logic state 1.

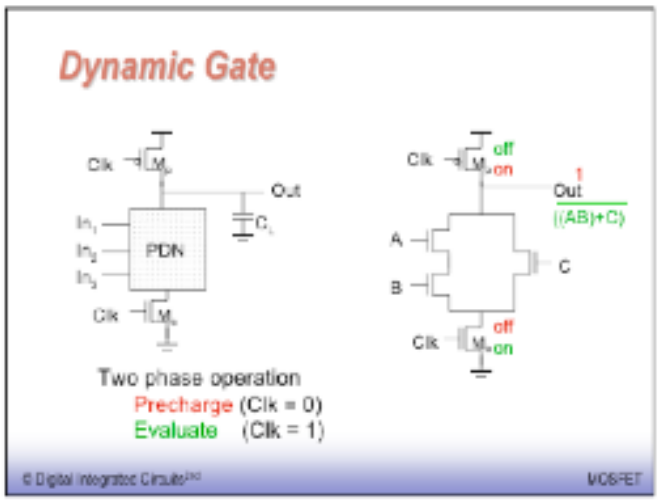



Fig. 1. Sketch of a CMOS dynamic gate showing both the precharge and evaluate functions.

A common problem with this type of circuit is leakage current that can either charge or discharge the capacitor. Since the output of the dynamic memory is usually connected to a CMOS gate, this change in charge can cause the gate driven by the capacitor to go to an intermediate state where both the NMOS and PMOS transistors are conducting. This results in a much larger than normal current draw. We believe that this is the fundamental mechanism responsible for all the high current states in the SVX 2. There are, however, several interesting details that control this current draw.

A portion of the SVX 2 schematic containing the dynamic memory cell is shown in fig. 2. There is no circuitry that can detect power on so at initial turn on, the capacitor will be at some arbitrary voltage. One clock to this circuit will set it to a known state and thus reduce the current draw. We tested this by sending clocks to the chip in its various

modes. Since the dynamic memory is used only during the Digitize cycle, we would not expect clocks in other modes (acquire, download or readout) to have any affect. This is what we observed. Sending one clock pulse to the chip in digitize mode reduced the turn on current to the normal low runtime current. Thus, we believe that this is the cause of the high initial current at chip turn on.

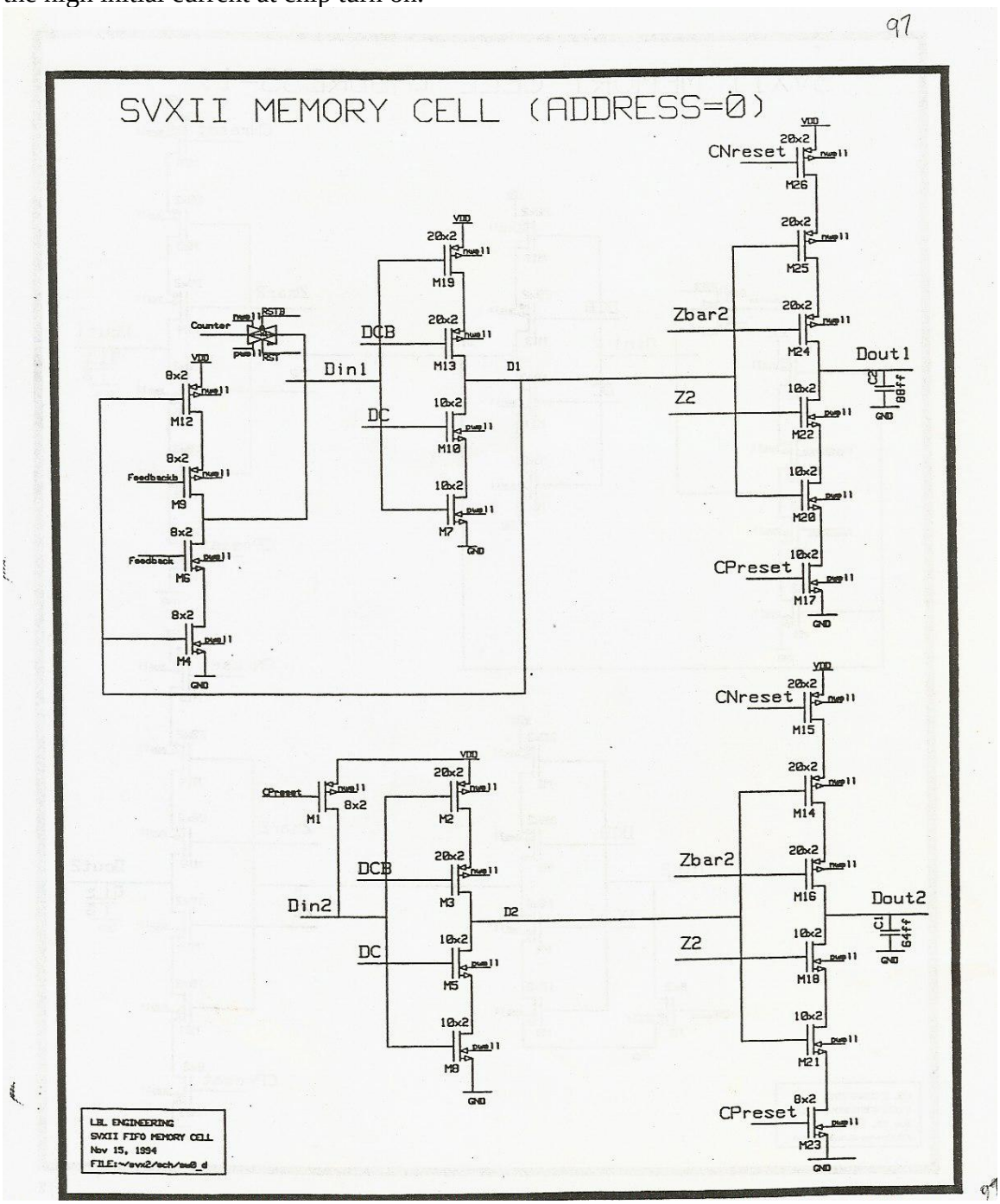



Fig. 2. This is a portion of the SVX 2 schematic showing the dynamic memory cell.

## Increase in Current Draw When No Clocks Are Present

When we first tested the chip at room temperature, we saw little increase in current. This indicates that the larger currents occur only at lower temperatures. Thus, we set up a test system to test the chips down to –20 C.

We converted a 3 chip HDI to single chip operation by reworking some of the wire bonds on a standard 3 chip HDI. The HDI was then mounted in a standard black plastic transport box that was mounted to a copper cold plate. The cold plate was installed in a freezer and also connected to a freestanding chiller. In addition, we installed two 60 watt light bulbs inside the freezer and a resistor heater that was connected to a variable power supply. This allowed us to cool the chip to about –15 C and to heat it to about +40 C.

Figs 3 -5 show DVDD current and temperature for 3 typical runs. These runs were independent of clock pulses as long as the chip was not in readout mode (the chip is not in readout mode for these runs except for an occasional CALINJECT cycle). Fig 3 shows a warm up cycle from about –10 to plus 16 degrees Celsius and a cool down to about –15 degrees Celsius. The warm up was done using the resistor heater on the cold plate and the cool down was done with the chiller (heater turned off). The striking thing about the plot is the large amplitude oscillations in the current during both the warm up and cool down cycle. Fig. 4 shows a cool down from 0 to about –15 and then a warm up to +26 Celsius. We again see the striking oscillations during warm up but also a very sharp drop to low currents at 26 Celsius. The small drops at the beginning and around 600 seconds are the results of CALINJECT cycles. That is, the current value in these regions is the normal operating current right after a CALINJECT cycle. Note that after the sharp drop at the end of the plot the current stabilized at the same value as with CALINJECTs even though no digitize clocks were sent.

Fig. 5 shows another run where we cooled the chip down. The difference is that in the middle of the oscillations (around 1700, 2200, 3000) we turned on the two 60 watt light bulbs. The black plastic box is not perfectly light tight because of the exit port for the HDI tail. We clearly see the effect of the light. It stops the oscillation completely. Moreover, it reduces the current to exactly the same value as the normal operating current after a CALINJECT cycle.

There are three properties of CMOS circuits and one feature of the SVX 2 that are important to understand this data.

1. CMOS leakage current increases approximately linearly with temperature. Also, reverse diode current doubles every 8 C but leakage current through CMOS transistors is somewhat less than this.
2. Hole mobility is around one third that of electrons. Notice in the schematic in fig. 2 that the nwell devices have a factor of 2 larger gate area to account for this.
3. The carrier mobility increases with decreasing temperature as T^-1.5. That is, carrier mobility increases with decreasing temperature but leakage current decreases with decreasing temperature.
4. The power distribution in the SVX 2 has relatively high impedance – perhaps as much as 10 ohms.

On the left side of fig. 3 we see that the current starts to rise and then breaks into oscillation as the temperature increases. The CMOS leakage current increases with temperature so the charge (and voltage) on the dynamic capacitor also increases. This increasing voltage causes both the nwell and pwell transistors that are controlled by the capacitor to turn on more and we have increasing current. This is the same as for the initial turn on current draw. However, this larger current draw causes increased chip heating because of bus resistance. We hypothesize that this heating is occurring some distance from the dynamic memory so that it takes some time for the heat to reach the transistors controlling the capacitor voltage. When the heat pulse arrives, it excites a large number of electrons into the conduction band so that the pwell devices become good conductors and drain the voltage off of the capacitor. This stops most of the chip current. Once the current stops, the chip rapidly cools, the electrons leave the conduction band turning off the pwell transistors and leakage current starts charging the capacitor again. Thus the cycle repeats. There are 2 experimental results that support this hypothesis. First, if it is heat, one should be able to heat the chip up externally and see the current drop. The right side of fig. 4 shows exactly this behavior. As noted above the current settles down to the very same value as achieved with CALINJECT indicating that the capacitor is completely reset. The second result is the effect of light. Light should also populate electrons into the conduction band so it should behave like a heat pulse. Fig. 5 shows that the light stops the oscillation and also that the current settles down to the CALINJECT value.

An obvious question is why does this not increase the conductivity of both the nwell and pwell parts. The reason the circuit discharges rather than charges (or stays the same) is the difference in mobility between the electrons and holes. The heat pulse populates the pwell transistors more than the nwell.

The decreasing amplitude of the oscillations during cool down as shown in the right part of fig. 3 can be understood as follows. As the temperature decreases, the leakage current decreases so the slope of the rising part of the oscillation should decrease. Fig. 6 shows the slope from the data in fig.3. The slope was computed from the point where the signal starts to rise to the peak of the signal for that cycle. One can see that the slope does decrease substantially and that the slope is linear with temperature. CMOS leakage current should be linear with temperature. The speed of the heat pulse propagating through the chip has almost no temperature dependence. Thus, the voltage on the capacitor when the heat pulse arrives decreases with temperature.

If one looks carefully at the right hand oscillations in fig.3, one sees that the steeply falling part develops a shoulder around 4200 seconds. This is most likely due to the decreasing amplitude of the heat pulse. There is less current to start with and the chip is colder so that more of the heat is dissipated before it reaches the dynamic memory. There is still enough energy to increase the pwell conductance so it still discharges. However, at the end of the cycle, there is not enough energy to fully discharge the capacitor and the current settles down to an equilibrium point above the CALINJECT

value. Essentially the nwell and pwell transistors are acting as a voltage divider that sets a constant voltage on the capacitor.

Note the flat bottom on pulses that starts around 4000 seconds. This is due to the finite threshold of the CMOS transistors. That is, until the gate voltage reaches around 0.3 volts, there is no conduction in the CMOS transistors. As the temperature is lowered and the leakage current decreases, it takes longer and longer for the leakage current to charge the capacitor to the threshold voltage. From this argument one would expect that the width of the flat bottom would depend on the leading edge slope. Fig. 7 shows a plot of the inverse of the width of the flat bottom and the slope of the rising edge of the oscillation (the same data as in fig. 6) as a function of cycle number. The plot shows a clear linear relation between the width of the flat bottom and the leading edge slope. This effect is undoubtedly present in all the cycles but it is hidden in the sampling period for the first few cycles.

The threshold voltage does decrease about 2.3 mV per degree C or about 50 mV over this temperature range. Since it is a decrease in threshold, it acts to narrow the flat bottom rather than widening it. Thus, we conclude that the leakage current decrease dominated the change in threshold.

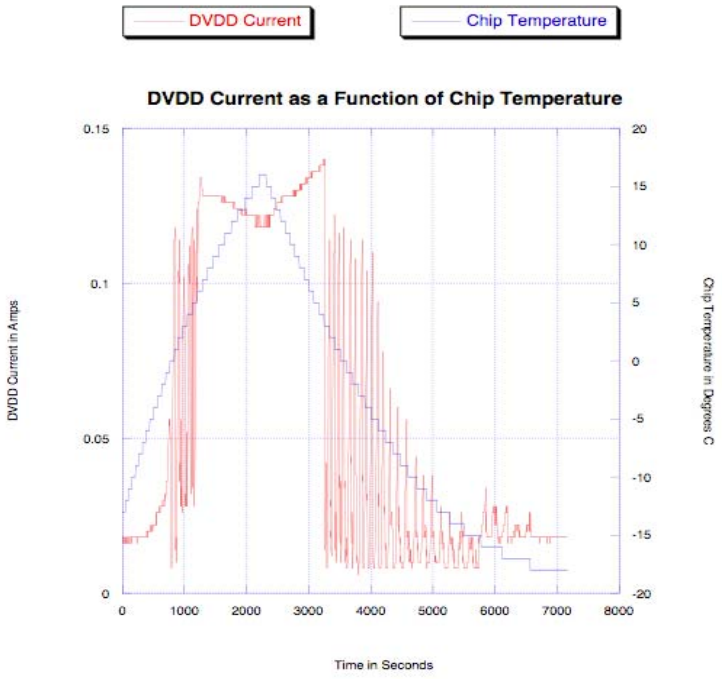


Fig. 3. DVDD current as a function of temperature. This plot shows the start of oscillations with both increasing and decreasing temperature.

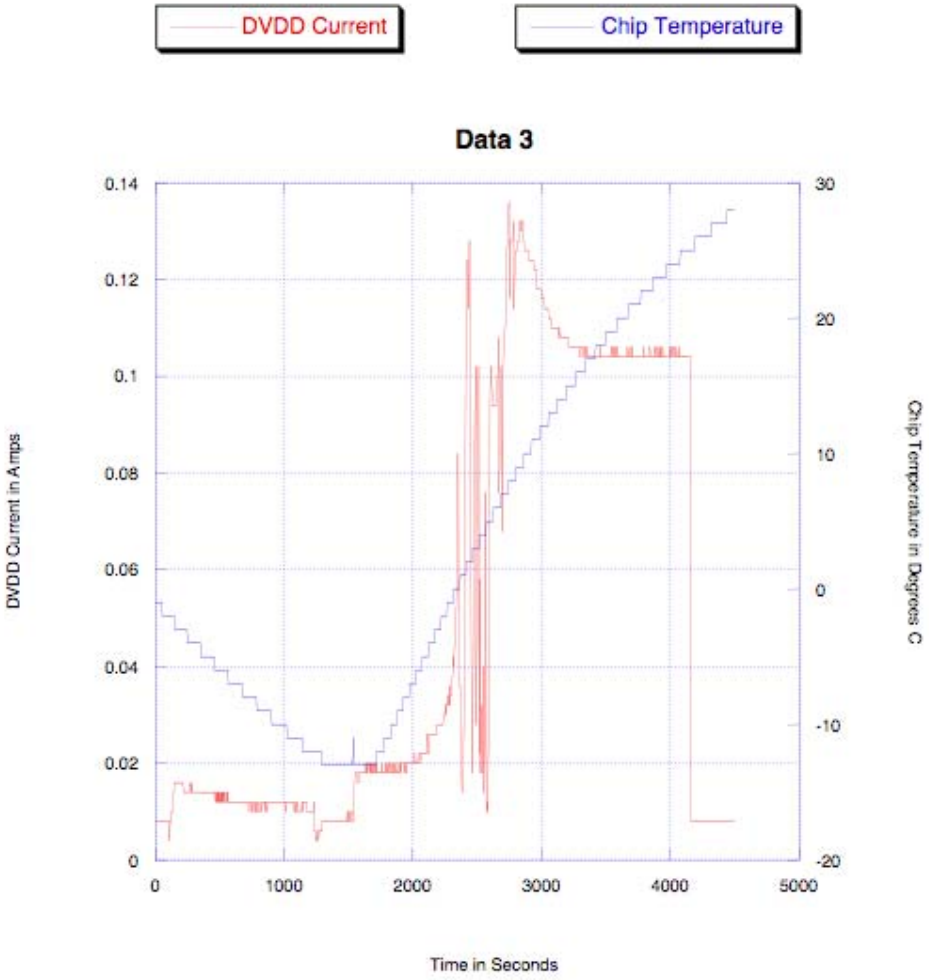



Fig. 4. DVDD current as a function of elevated temperature.

Note the sharp drop at 26 degrees.

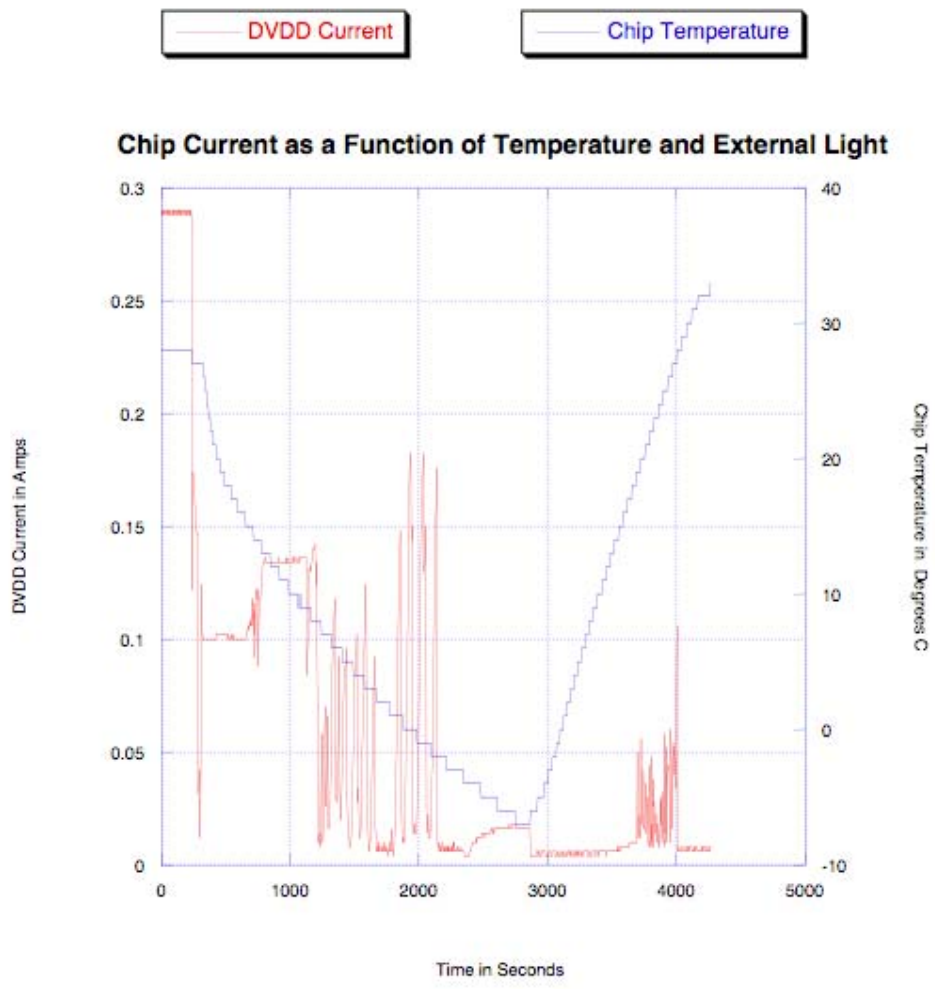



Fig. 5. DVDD current as a function of temperature and external light. Two 60 watt light bulbs were turned on around 1700, 2000 and 3000 seconds. Note that the light stops the oscillations and returns the current to normal current draw.

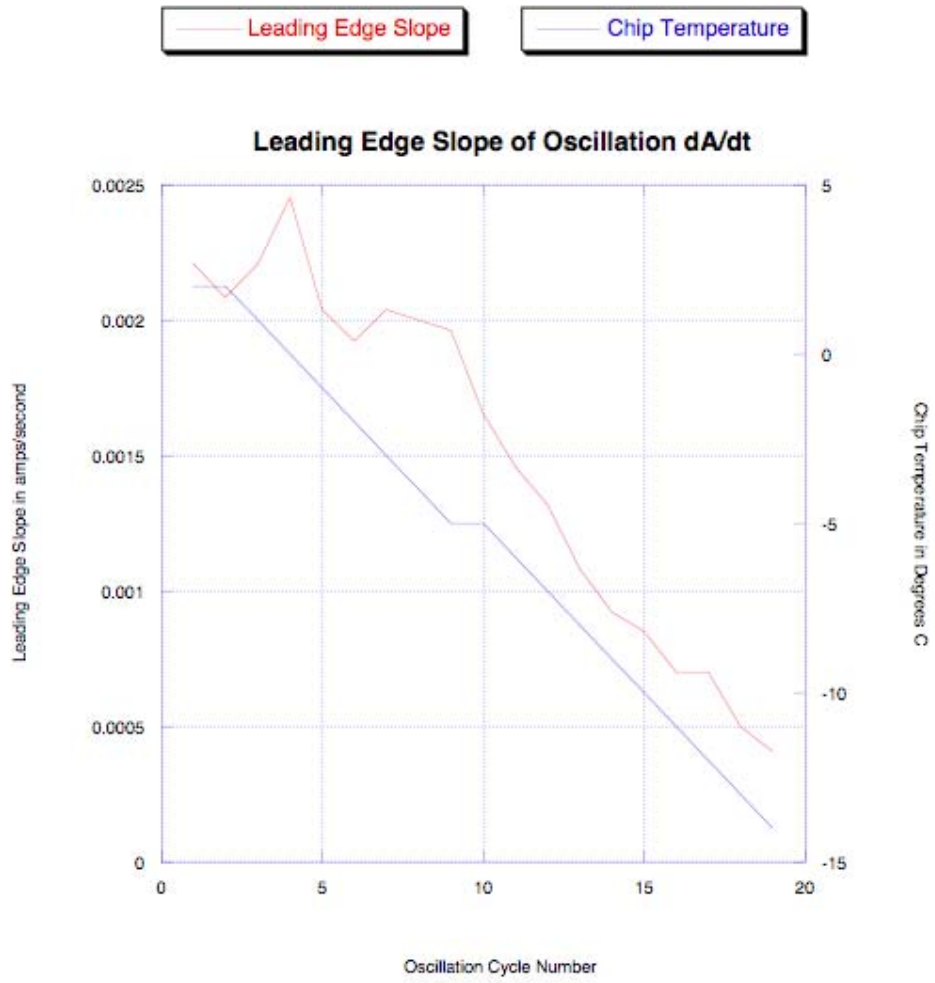



Fig. 6. Slope of the leading edge of the oscillations in fig 4 starting at 3300 seconds. Note that the slope decreases linearly with cycle number.

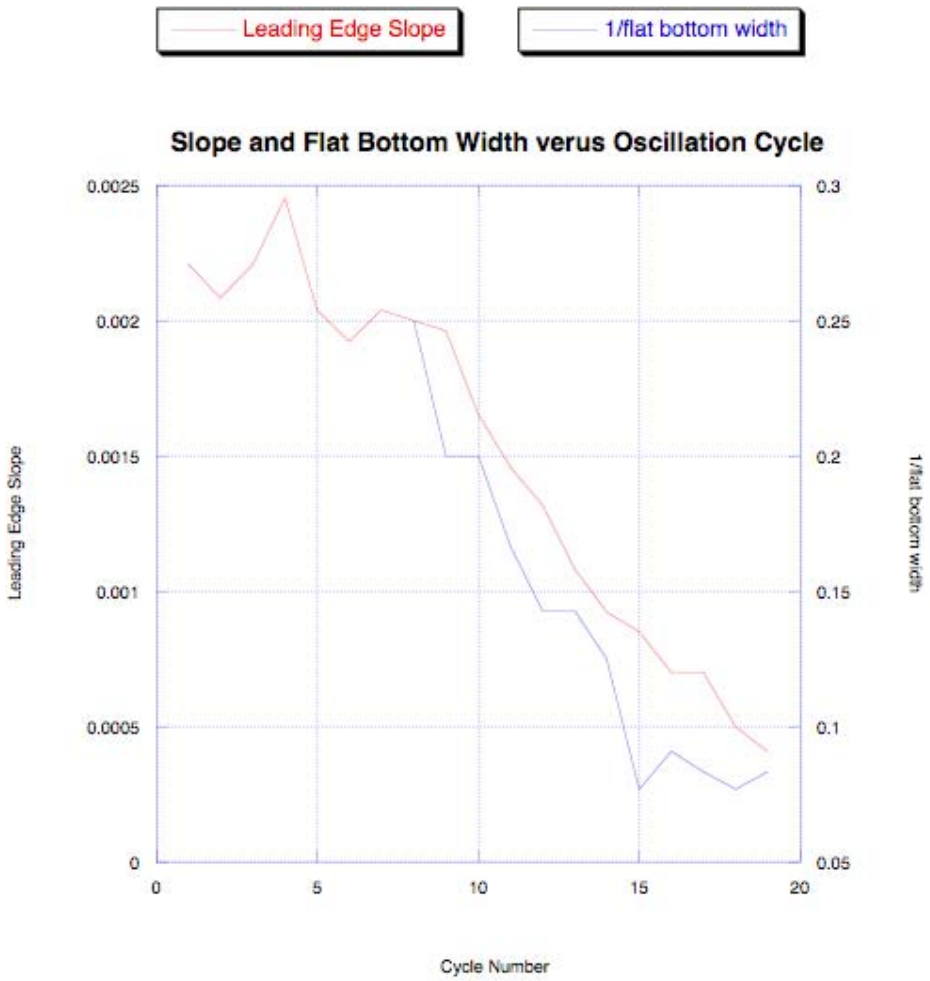



Fig. 7. Slope of the leading edge of the oscillation and the inverse of the flat bottom width of each cycle versus cycle number. This shows that smaller slopes are correlated with wider flat bottoms on the oscillation cycles.

## II. HDI Failure studies

During the first half of 2007 we made two accesses to the cathedral to test some of the HDIs that failed during the August 30 accident. One access was to the east side and the other was to the west side. During these accesses we set up a stand-alone sequencer and tested the HDIs with a completely independent test system. We were not able to read

back the downloaded data from any of the failed HDI's but we were often able to read out a few of the chips. By checking the chip ID we verified that these chips had been correctly downloaded and the signals read out from a Cal-Inject pulse looked normal. However, the Priority-Out signal from the HDI (which is used to read back the down loaded data) was much smaller than from a normal HDI. Every failed HDI in the west platform that we tested had a small Priority-Out signal. We were also able to get a partial readout on many of them. The ones on the east side also had a small Priority-Out signal and very few of them read out any chips. Fig. 8 shows a typical scope trace from the west cathedral.

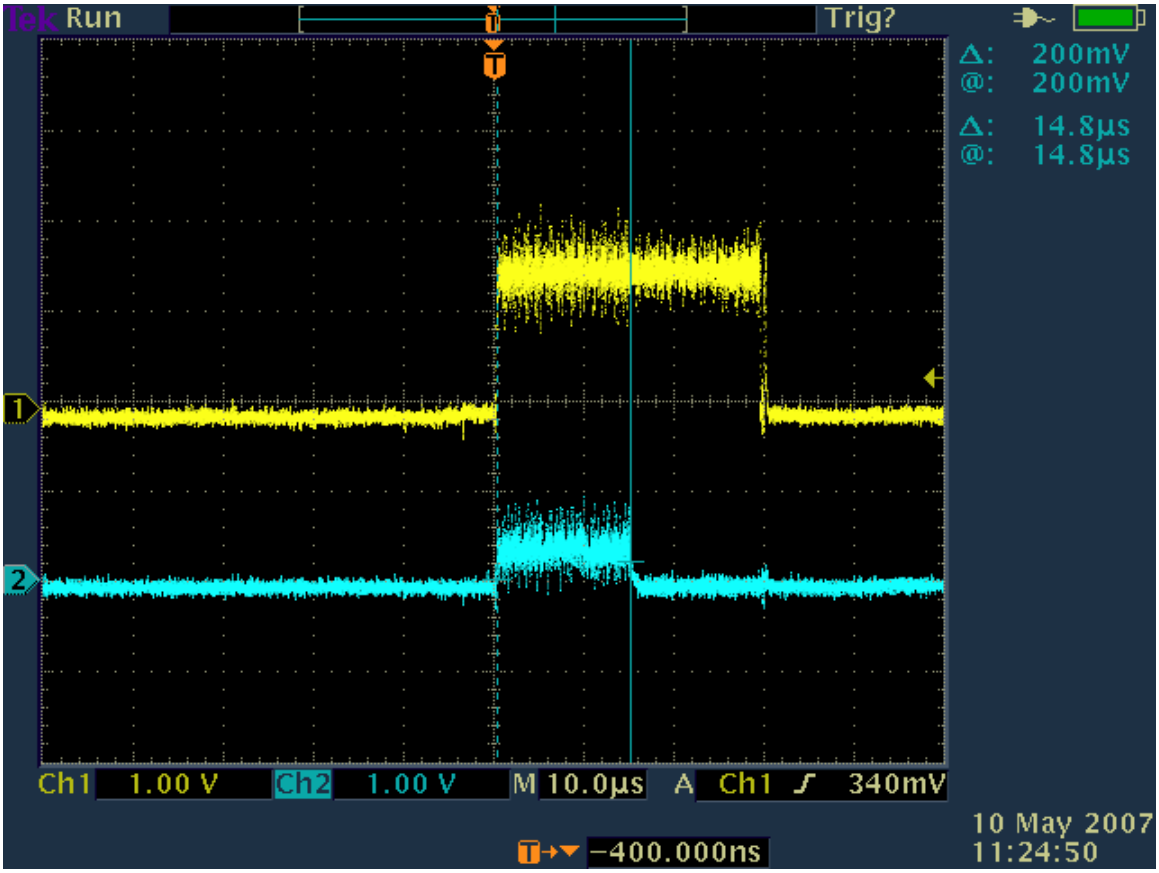



**Fig. 8. Oscilloscope trace of Priority-Out from a bad HDI (blue, lower) and a good HDI (yellow, upper). The amplitude of the bad HDI signal is about 500 mV.**

Because downloading an HDI uses only 6 lines (three mode-control lines, the priority passing daisy chain, DVDD power and ground) we decided to concentrate our studies on this operation. There are multiple grounds on the chip so a ground failure is unlikely. We have observed many broken priority passing lines in the H disk that was removed from the detector so this line is a possibility. The low amplitude Priority-Out signal suggests that DVDD power might be a problem. Thus, we decided to focus our tests on these two lines.

## Probe Station Testing

We set up a test system using the probe station on DAB 3 that was very similar to the cathedral test system. We took 2 good HDIs and removed a priority passing bond near the middle on one HDI and the DVDD power bond from a central chip on the other.

The HDI with the broken priority line did not download and it read out only 10 cycles of bad data before quitting. From the SVX 2 schematic we observed that an open Priority-In line on a chip floats low. A low Priority-In line causes the chip to start to read out. Thus, when readout started, we had two chips on the bus at the same time so that is the reason for the bad data. From past experience we know that non-downloaded chips read out only the chip ID and status. Since there were 3 chips after the break, each chip read out a few cycles and passed the readout token on to the next chip which repeated the operation. The last chip then terminated the readout by lowering its priority out line. This is the reason we saw only about 10 cycles.

This behavior rules out a broken priority line for three reasons. First, the amplitude of the Priority-Out line is not smaller than usual. Second, we could not read out an entire chip and, third, we did not get any good data. We conclude that the platform failure mode does not involve a broken priority passing line.

The HDI with the broken power line also did not download. However, we were able to read out all the chips before the broken bond with no problem just like the cathedral tests. We had to cycle the power after every read out but the data was OK. Fig. 9 shows a scope picture of the Priority-Out line from a chip with a broken DVDD line. The line termination was the same as in the platform and it looks very similar to the ones from the detector.

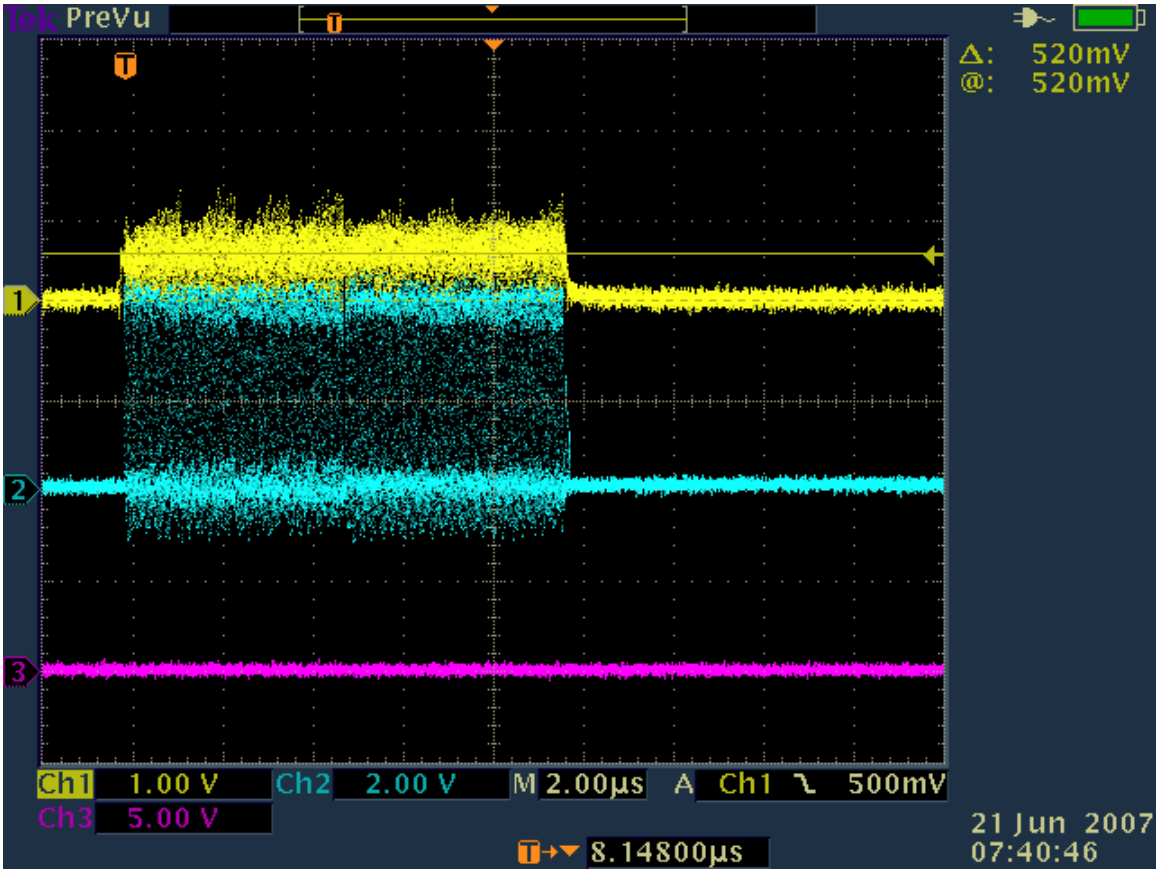



**Fig. 9. Oscilloscope trace for a three chip HDI with the DVDD wire bond broken on the last chip. The line termination is the same as in the platform. The yellow (upper) trace is Priority Out and the blue (middle) is data valid. This shows that Priority-Out remains high during the readout of the first two chips. Note that the amplitude of the yellow trace is very similar to that from a bad HDI on the platform.**

## HDI Recovery

All the digital lines on the SVX 2 have protection diodes both to ground and the DVDD power bus, as shown in Fig. 10. It is known that one can at least partially power an SVX 2 chip through the bus lines. If the bus lines are high and there is no DVDD power on the chip, the protection diodes conduct and raise the DVDD voltage to the bus line voltage less a 0.6 volt diode drop

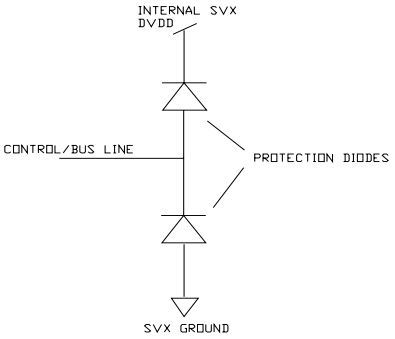



**Fig. 10. Schematic of the protection diodes on one bus line of the SVX2E. The mode control lines are similar but the diodes have series resistors.**

To test if the bus lines can provide enough power for download and readout we raised the voltage on the driver transceiver on the test card to 5.5 V from 5.2 V. This raised the voltage on the bus lines to the chip from 4.7 V to 5.0 V. Note that this is only 4.4 V on the chip after the diode drop. We were then able to download the HDI successfully and also to read out 8 of the 9 chips. Note that this test was done after removing the terminating resistor on the Priority-Out line so that the chip was more lightly loaded.

We did the same test with a 3 chip HDI where the DVDD wire bond was broken on the last chip. This chip required us to raise the transceiver voltage to 5.7 volts (5.2 on the bus line) in order to get error-free downloads. For the 9 chip HDI the chips downstream of the unpowered chip still had bad data. There is apparently enough power for the chip to pass the download signals but not enough to read out. The reason for the latter is evident from fig. 11. The blue trace shows the data valid signal at the point when the unpowered chip takes over the readout. Note the exponential fall off in the signal amplitude and the start up of large pulses. The bus is not able to provide enough power though the protection diodes to maintain the amplitude. At some point the downstream chip thinks that it has received a low Priority-In signal and starts transmitting its data. Both chips are on the bus at this time. The offset in the timing of the superimposed DVALID pulses is probably due to the fact that the Priority-Out signal falls slowly and is not determinate. In addition the number of clock cycles may not be an even number so there could be an offset in the data.

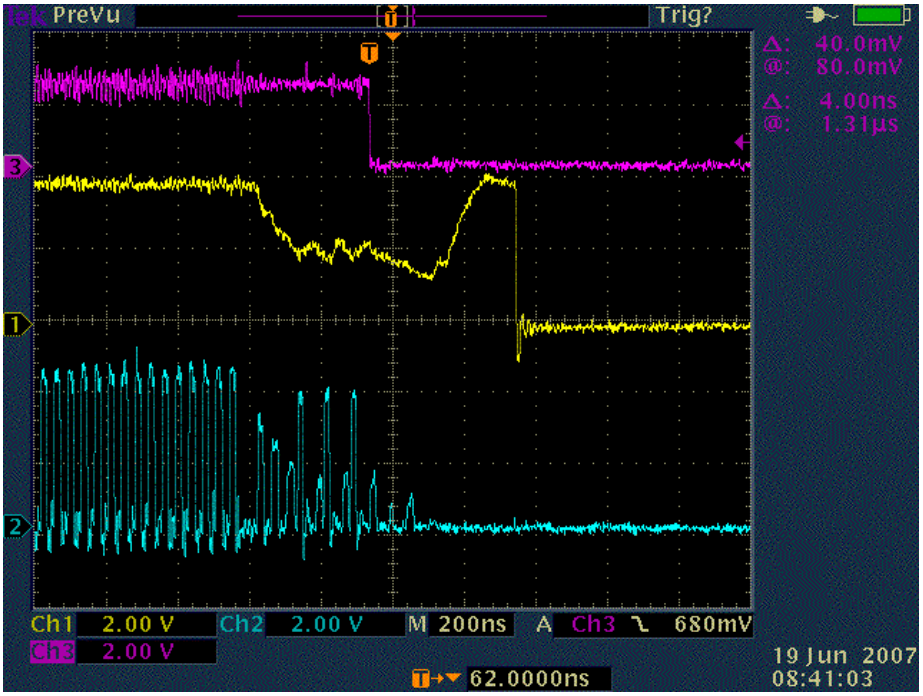



**Fig. 11. Oscilloscope trace from HDI with an unpowered chip.**
**Purple (upper) is the Mode_1 line. Yellow (middle) is Priority-Out of the unpowered chip and blue (bottom) is the Data-Valid trace. The unpowered chip is downloaded to read all. Note the exponential decay of the data valid pulses and the turn on of the next chip in line. Also note the recovery of the Priority-Out line after the chip stops sending and then the clean drop to transfer the readout control.**

The obvious solution to this is to set the unpowered chip to sparse mode (all tests were done in read-all mode) and set the threshold to 255 so that only the chip ID and status are read out. Fig. 12 shows the Data Valid signal for this combination. This works very well with good readout nearly 100% of the time. We did see a bad pulse but we were not able to reproduce it.

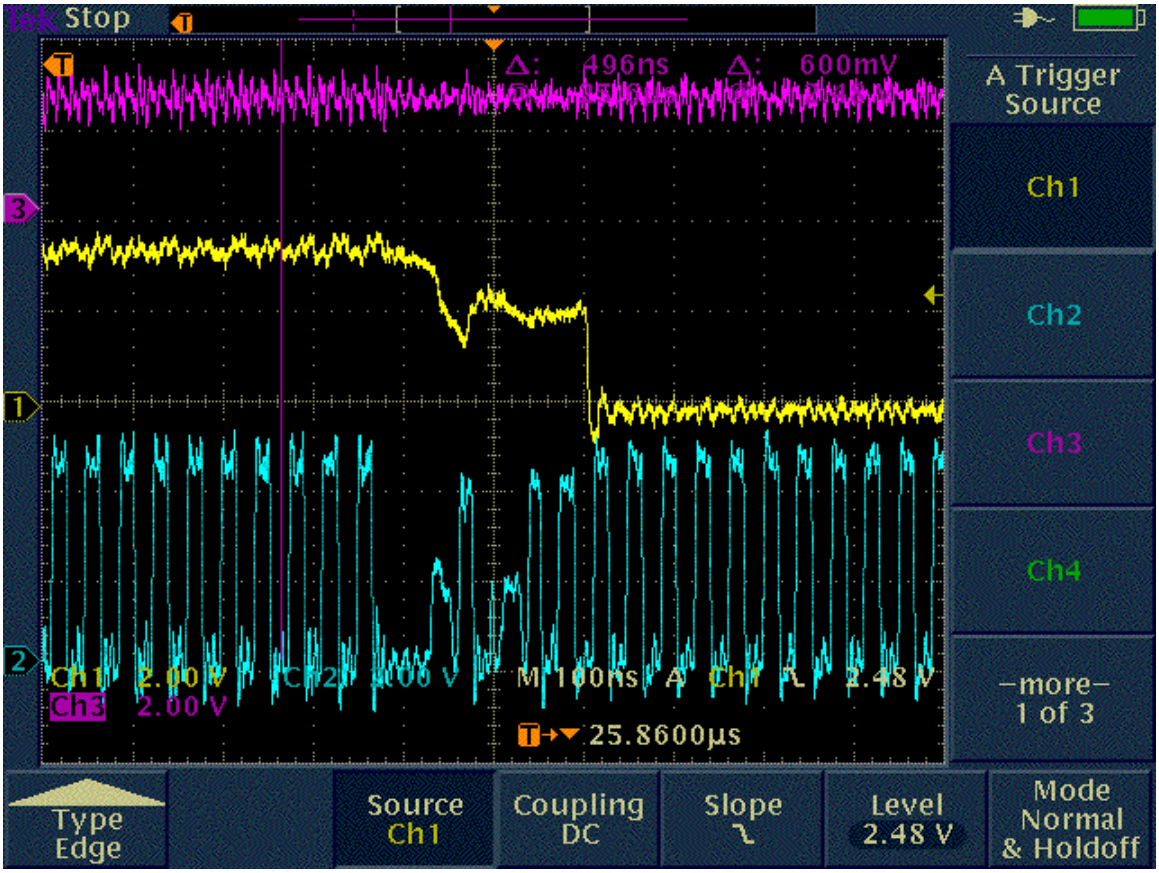



**Fig. 12. This is the same setup as fig. 2 except that the unpowered chip has been set up for sparse mode with a 255 threshold. Note the larger Data Valid pulses and the smaller sag of the Priority-Out line. This mode results in almost perfect readout of 8 out of the 9 chips.**

During readout, only the Mode_1 bus line is high so this is the only line powering the chip. We feel that if we raise the voltage somewhat above 5 volts, we will increase the voltage margin enough to recover all the chips except the failed one.

Fig. 13 shows the voltage (yellow trace) on the DVDD pad of the chip with the missing wire bond for the 9 chip HDI during initialization. There is very little voltage sag indicating that the parallel combination of four bus lines and large diodes is able to hold the voltage very well. Figs. 14 and 15 show the same as fig. 13 except that the data is taken during readout of the chip. Note that there is an exponential decay caused by the 200 ohm series resistor in the Mode 1 protection diode (see fig. 10). Also note that the voltage falls by 1.8 volts. This is the reason we cannot readout the chip with the broken bond.

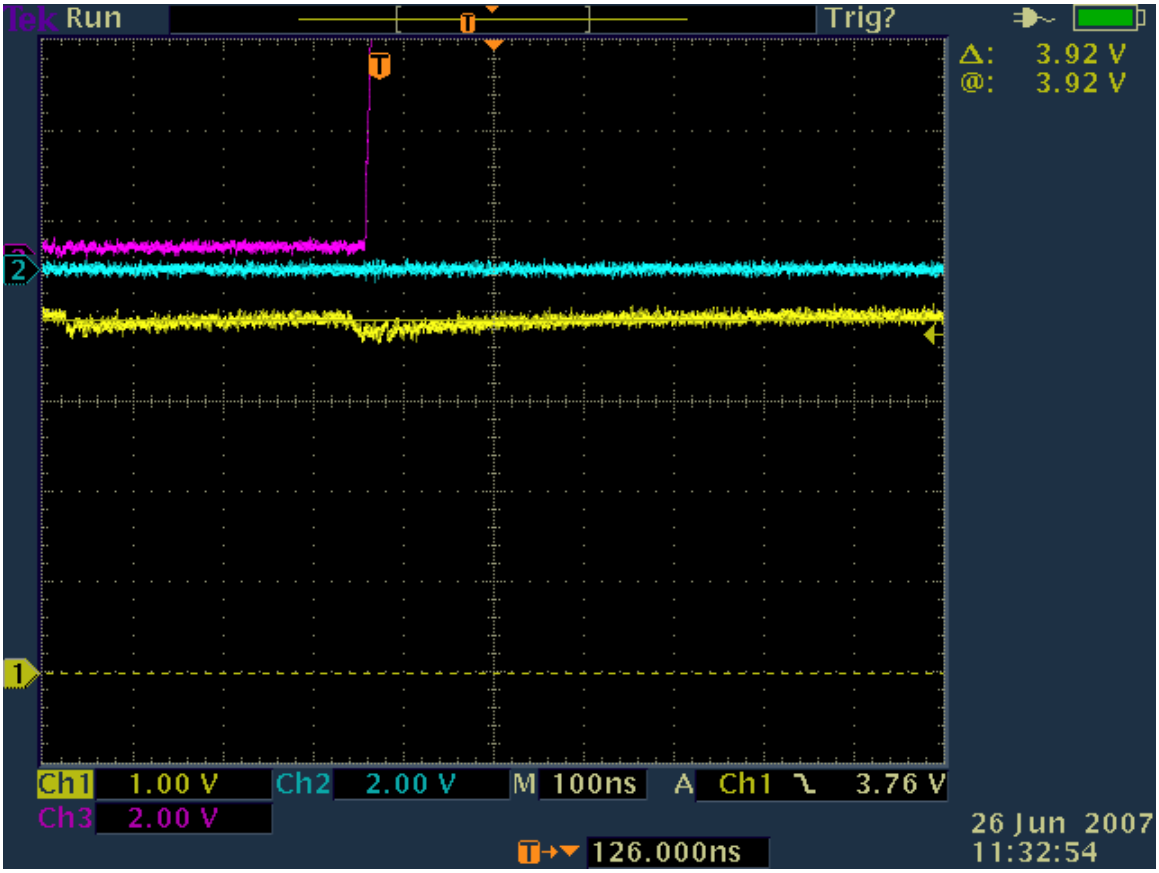



**Fig. 13. The yellow (bottom) trace is the voltage on the DVDD pad, during chip initialization, of the chip with the missing DVDD wire bond on a 9 chip HDI. Note that the nominal voltage is about 4 volts and the voltage drop is around 200 mV. This shows that the readout bus provides adequate power during down loading. The plot for digitize is similar.**

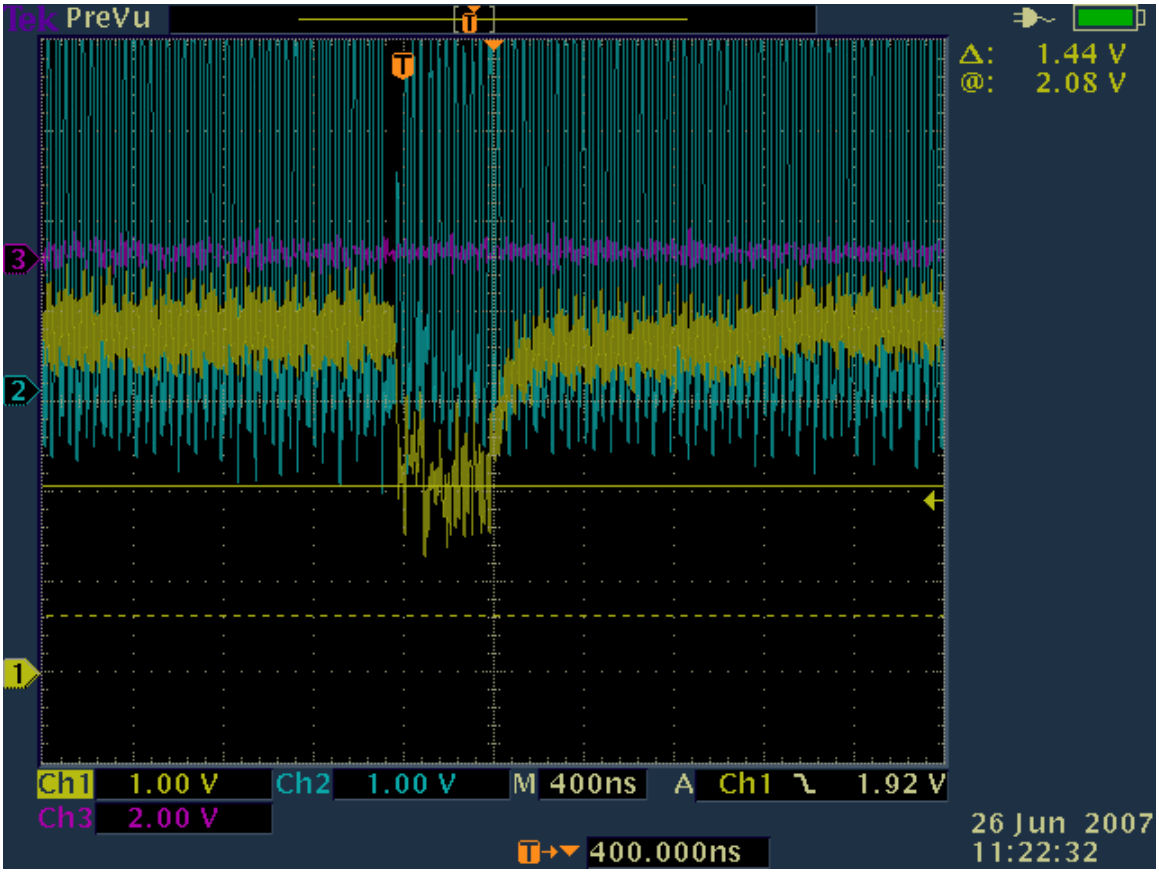



**Fig. 14. Voltage on DVDD pad (yellow, bottom trace) of chip with missing DVDD wire bond, during readout. Note the sharp voltage drop when this chip is enabled by the Priority-In line (1.8 V drop). The blue (middle) trace is the Data Valid line. The gap is the normal 2 cycle skip between chips. The next reduced amplitude pulse is the data valid for chip ID and status (both edges of data valid are used so there is only one pulse for both signals). Note the exponential decay in voltage when the chip is selected and the exponential rise when it is deselected. This is caused by the 200 ohm resistor before the protection diode in the mode line. The voltage when selected is 2.08 volts which is enough to transfer Priority-Out to the next chip.**

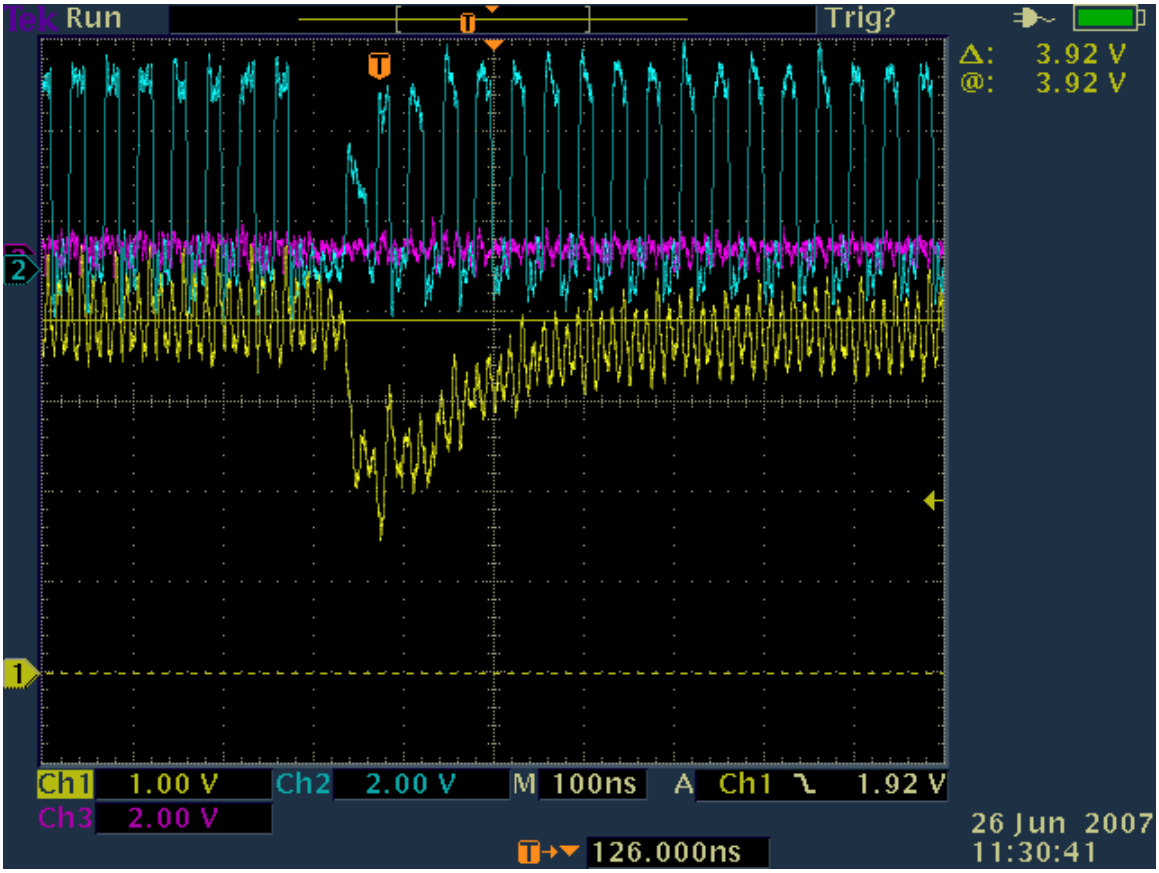



**Fig. 15. This is the same as fig. 6 except that the time base is faster. The time constant for recharge is particularly striking here.**

We also looked at the digitize period. Here both mode lines are high as are two bus lines. We do not see any significant voltage sag during digitize so the combination of the 4 lines provides adequate current.

The broken power bond fits all the platform data including the low amplitude Priority-Out line. We measured the voltage on a terminated Priority-Out line at .55 V for the unpowered line versus 2.6 volts for a good one. This is true only if the unpowered chip is the last one in the chain. If the last chip is unpowered, we are able to duplicate all the platform behavior at the probe station. If the first chip fails, we would get nothing out which was true for some of the east side HDIs that we tested.

During the access on June 25, 2007 we took 3 different HDIs that had failed during the Aug 30 incident and connected them to a stand-alone sequencer. We increased the voltage on the transceivers in the same manner as in the test stand and all 3 downloaded with no problem. Two HDIs read out all but the last chip. The third one read out only the first three chips even though it down loaded OK. We looked carefully at the output signals and we conclude that there is an additional problem with chip 4 that causes it not to pass priority correctly. The wire bonds are OK since we can successfully download.

All of the above results indicate that the cause of the August 30 failure is the opening of the DVDD wire bond on the edge chips.

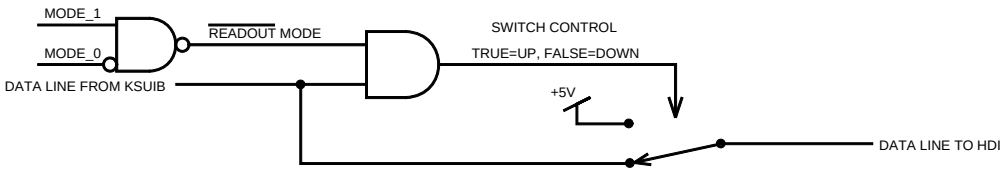
Tom Zimmerman has looked at the layout and he feels that the data bus diodes can take tens of milliamps of current. The mode control diodes have a 200 ohm series resistor so they are very well protected against over current. Because of the resistor in the mode lines, we must limit the current draw during readout, which means that we have to remove the terminating resistor on the Priority Out line. The best solution appears to be to modify the adapter card to provide both enhanced voltage on the bus and mode lines and also to have line drivers for the Priority-Out and Data Valid lines. The next section describes the new card.

## III. The Recovery

The original Adapter Card designed at Kansas State University was a passive junction point for the Low-Mass Cable coming from the HDI and the higher-quality "Gray Cable" which ran the rest of the way to the Interface Boards. All components on this version of the card are for filtering the three SVX voltages (AVDD, AVDD2, DVDD) and the sensor high voltage.

We designed a new Adapter Card to replace the KSU board for the failed HDI's. The new Adapter Card has a FET switch inserted into bus lines D0, D1, D4, and D5 as shown in Figure 16. In Readout mode, the switch is in the "normally closed" position and the signal from the SVX travels unmodified back to the Interface board. In all other modes, the switch is in the "normally open" position which connects +5 Volts to the lines going to the SVX if that line normally would have a logic high signal. This effectively increases the voltage to these bus lines enough to power up the DVDD net via the protection diodes. The position of the FET switch is controlled by the two mode lines using simple logic. During readout mode a similar technique is used on the Mode_1 line since this is the only line going to the chip that has a logic high value. This ensures that the chip has some power to adequately pass the Priority_Out signal on to the next chip or, in the case of the last chip, back to the Interface Board. Again, during download the chip is put in sparse data mode with the threshold high to insure that the chip passes priority immediately before it runs out of stored charge on DVDD. Thus we can successfully read out all but this chip on an HDI.

The new Adapter Card also has TTL buffer chips for Dvalid and Priority_Out signals. Since the low mass cable is fairly short we decided to decrease the termination load on these lines in order to lower the power drawn from the chip during readout mode. They are not matched terminations but work adequately in this configuration. A 47pF capacitor to GND on Priority_Out suppresses small glitches from the bus lines switching.




TRUTH TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| DATA LINE FROM I.B. | READOUT MODE | DATA LINE TO HDI |
| X | H | CONNECTS TO I.B. DATA LINE |
| H | L | CONNECTS TO +5V |
| L | L | CONNECTS TO I.B. DATA LINE |

Figure 16. Logic diagram and truth table of new Adapter card circuit.

## Test Procedure and Recovery in the Gap

Prior to the shutdown the SMT experts assembled a list of HDIs to investigate. This list included the HDIs that failed during the incident as well as those that were previously disabled because of various faults. Failures included those that didn't download, bit errors in readout, missing chips, etc. The Appendix shows this list along with results of the recovery effort and final status.

Each gap was worked on by a team of two people, one who worked on the Adapter Card and one to run the SMT GUI on a nearby laptop computer. The typical procedure was to first verify that the targeted HDI behaved as indicated in the list. We then would install a "walking HDI", which was known to be good, on the Adapter Card and if this worked as seen by the GUI we then would install a new Adapter Card. While we had the Adapter Card out, we would check for clock continuity on the detector HDI by measuring the resistance from CLK center conductor to that of /CLK. The nominal reading would be about 150 ohms due to the termination resistor. In most cases these tested fine, but in several cases the reading was intermittent, so we installed a new connector onto one or both of the clock coaxes. In some cases this was all that was needed to restore the HDI. In most cases where we installed one, the new Adapter Card fixed the problem. In a few of the cases we reconnected the old Adapter Card because it was clear that the HDI was damaged. If the new Adapter Card worked we could then look at the Dvalid signal and immediately see which chip had the broken wire bond, since that chip would only give a single DValid pulse as opposed to the 129 pulses that a good chip would send. We went through the list on a first pass and replaced 69 Adapter Cards. Second and third passes were conducted to more thoroughly scrutinize the HDIs that were not fixed the first time

to see if we could recover more channels. It was during these passes that a variety of remedies were tried, including replacement of Interface Boards, Sequencers, reseating of cards and connectors, and repairing of more clock cables.

## IV. Noise Caused by the New Adapter Card

Initial operation with the new adapter cards showed many channels with very large pedestals or large numbers of zero data readings. Most of this noise is caused by the preamp reset signal. If we remove this signal by modifying the sequencer firmware, all of the zero readings and almost all of the noise disappears. We made a substantial reduction in the noise by removing an unneeded preamp reset signal that occurred right before digitization and moving the once-per-turn reset earlier in the abort gap.

The added noise in preamp reset is caused both by the larger amplitude (5 volts) and the faster rise time. The old preamp reset signal is generated on the interface board so it travels through an additional 30 feet of cable, which degrades its rise time. The new preamp reset is created on the new adapter card.

The SVX 2 chip has a known problem with the counter that controls which capacitor receives the charge signal from a crossing (called the ring counter). This counter is composed of two physical counters - one for writing and one for reading. The sharp edges of the preamp reset signal appears to affect the read counter. Whenever the read counter fails, it connects a large positive voltage to the ADC. This voltage is constant and independent of any preamp signal. This causes a large ADC signal if the SVX 2 is set for positive signals or zero if it is set for negative signals. This data also shows that the noise data is not simple pickup in the front end. If it were, we would see equal noise signals for both input polarities.

Since we need the larger amplitude to power the SVX 2, the only easy solution is to reduce the rise time. We originally installed an inductive filter in the power line to the new adapter card. The purpose of this filter was to keep noise from the new adapter card. Since it is an inductive (reflective) filter, any noise generated on the adapter card side of the filter is made worse because the filter reflects the noise back to the source. In this case the source is the new adapter card. Because of this reflective affect, changing the adapter card power line filter from an inductive filter to a simple capacitor across the power lines reduced the noise. Figs. 17, 18 and 19 show the voltage at the adapter card side of the power supply for the inductive filter, a capacitor filter with 22 µF capacitors and a capacitor filter with 450 µF capacitors. Figs. 20, 21 and 22 show the affect of different filters on the test stand. Fig. 20 has one 22 µF capacitor across the power line. Figs. 21 and 22 are with a filter that has a 500 µF capacitor in parallel with the 22 µF one. Fig. 21 has the capacitor across the power leads and fig 22 has the filter to the test stand ground. There is a substantial reduction in noise with the larger capacitors connected to ground.

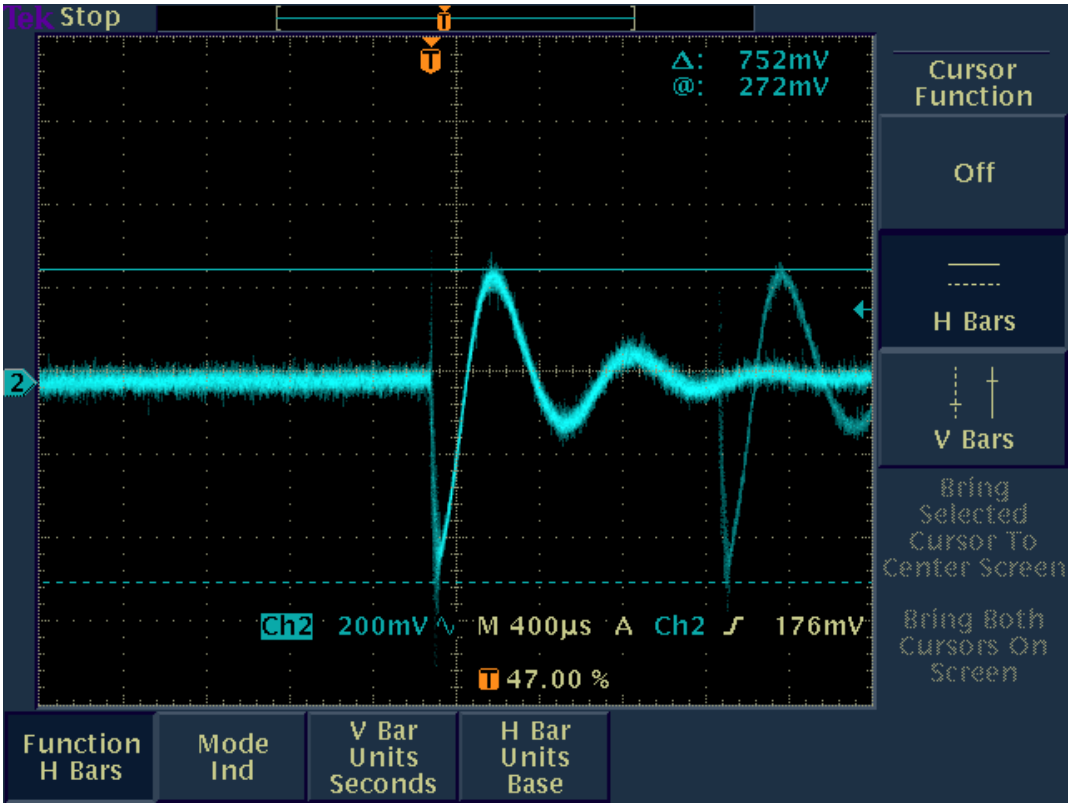



**Fig. 17. Supply voltage for the new adapter card measured on the adapter card side of the original inductive filter. The sharp voltage drop is at the start of the readout cycle which lasts about 50 µs.**

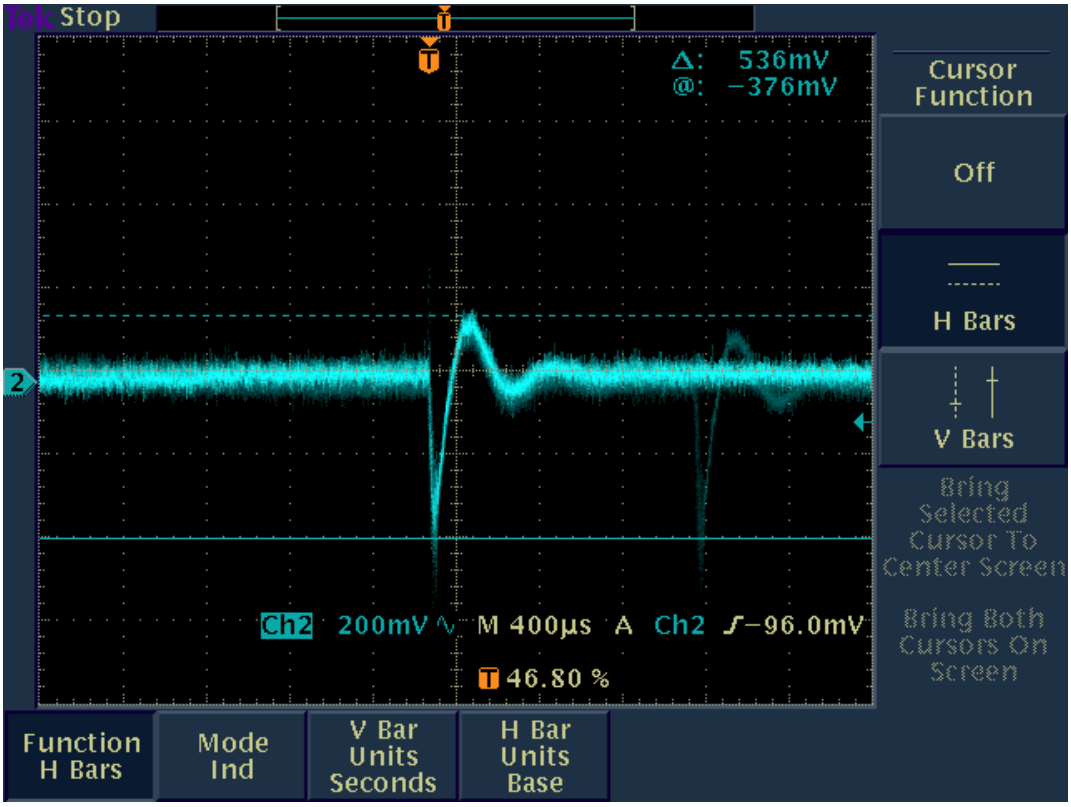


**Fig. 18. This is the same as fig. 17 but with a filter consisting of a parallel combination of a 22 µF tantalum and a 1.5 µF X7R capacitor. Note the reduction in the amplitude of the oscillation.**

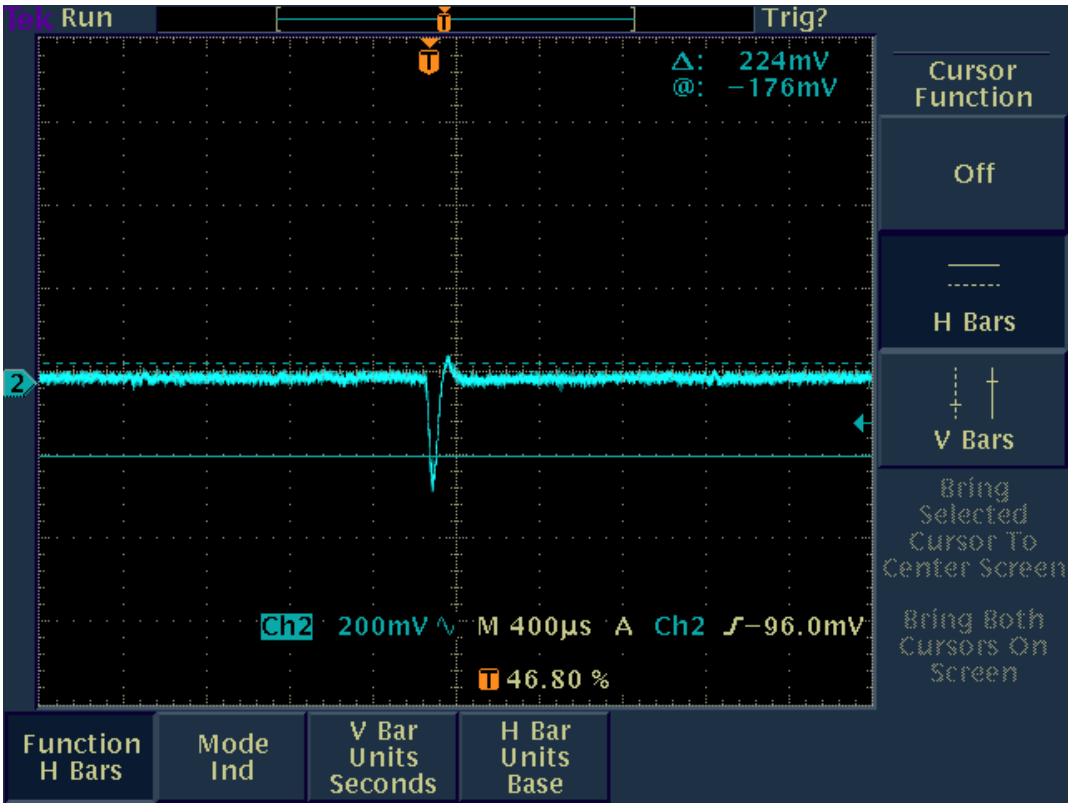



**Fig. 19. This is the same as fig 18 but with the addition of a 450 µF tantalum capacitor between the supply line and calorimeter ground. Note that the other capacitors are across the source and return lines so this capacitor is not directly in parallel with the other two.**

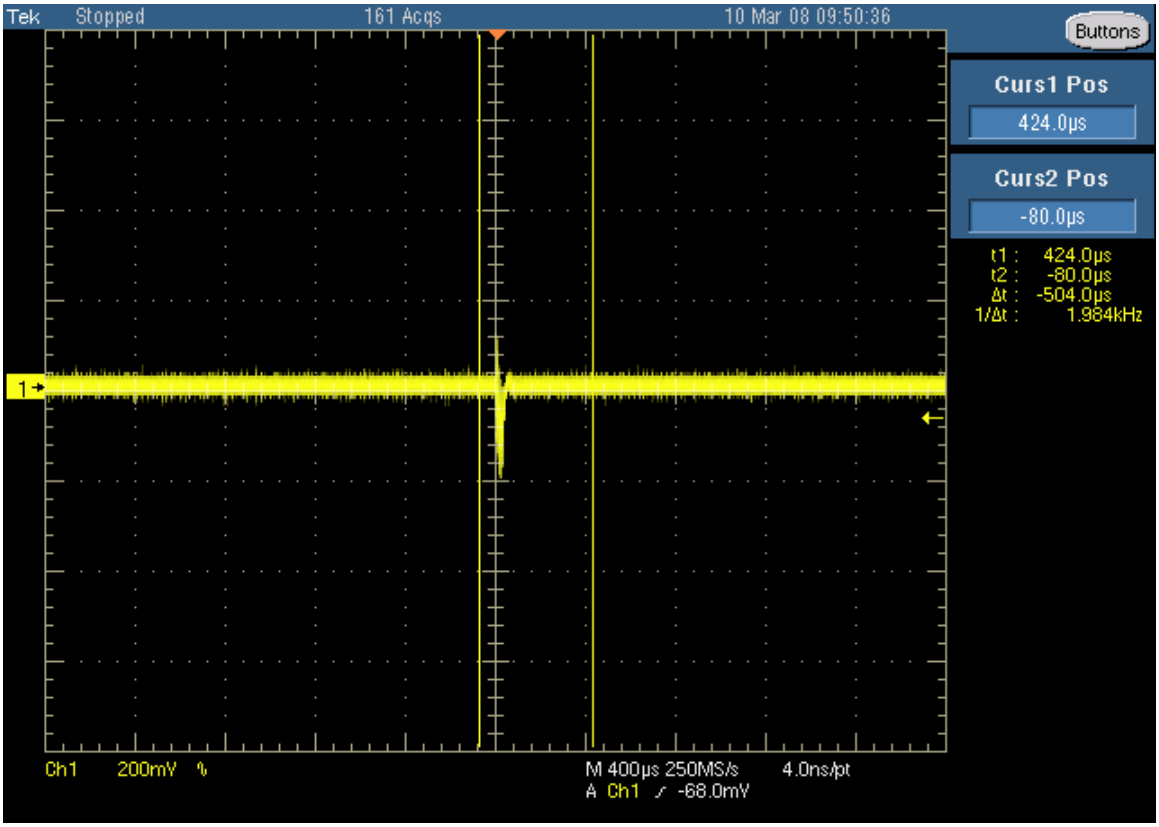



**Fig. 20. Signal with the 22 µF capacitive filter on the test stand. Note that this is the same scale as the other plots. The smaller noise signal is likely due to the much smaller load at the test stand. The test stand only has 2 adapter cards versus an average of 17 for the detector.**

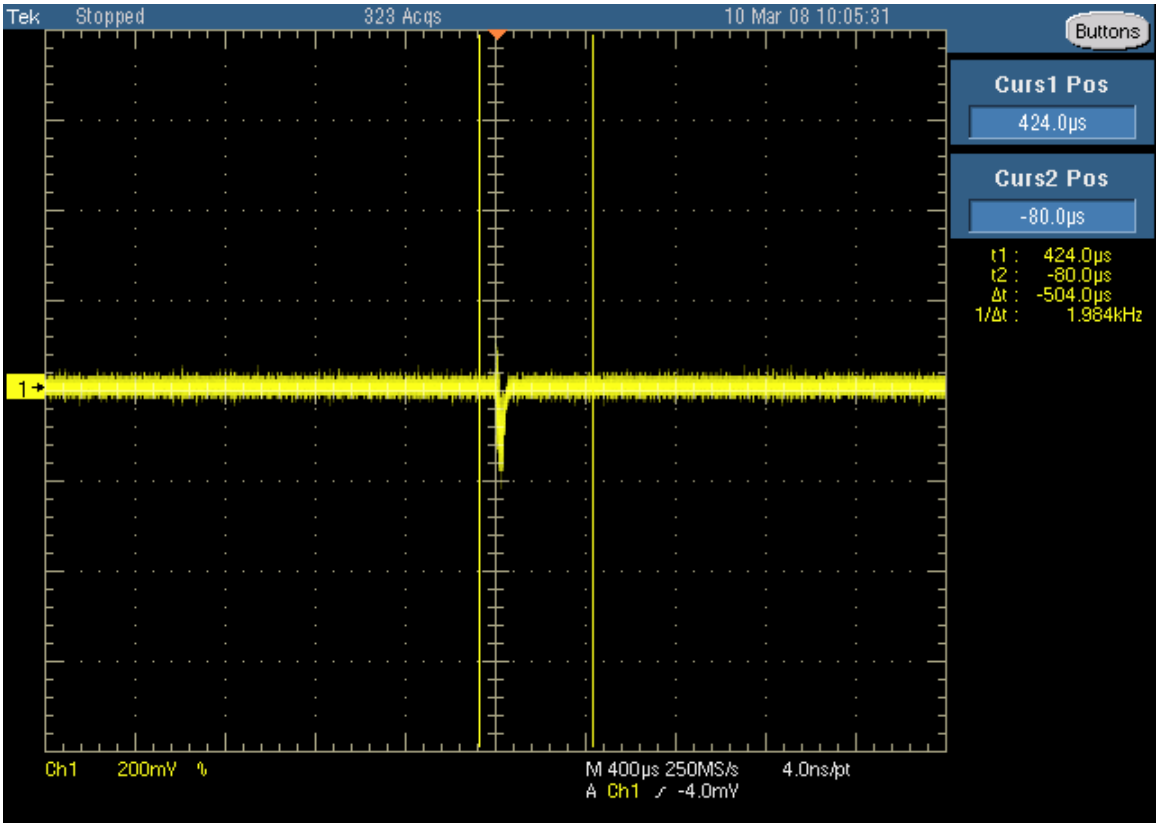



**Fig. 21. This is the same as fig. 20 except that a new filter with 500 µF capacitors in parallel with the 22 µF capacitors is installed. It is connected across the power leads.**

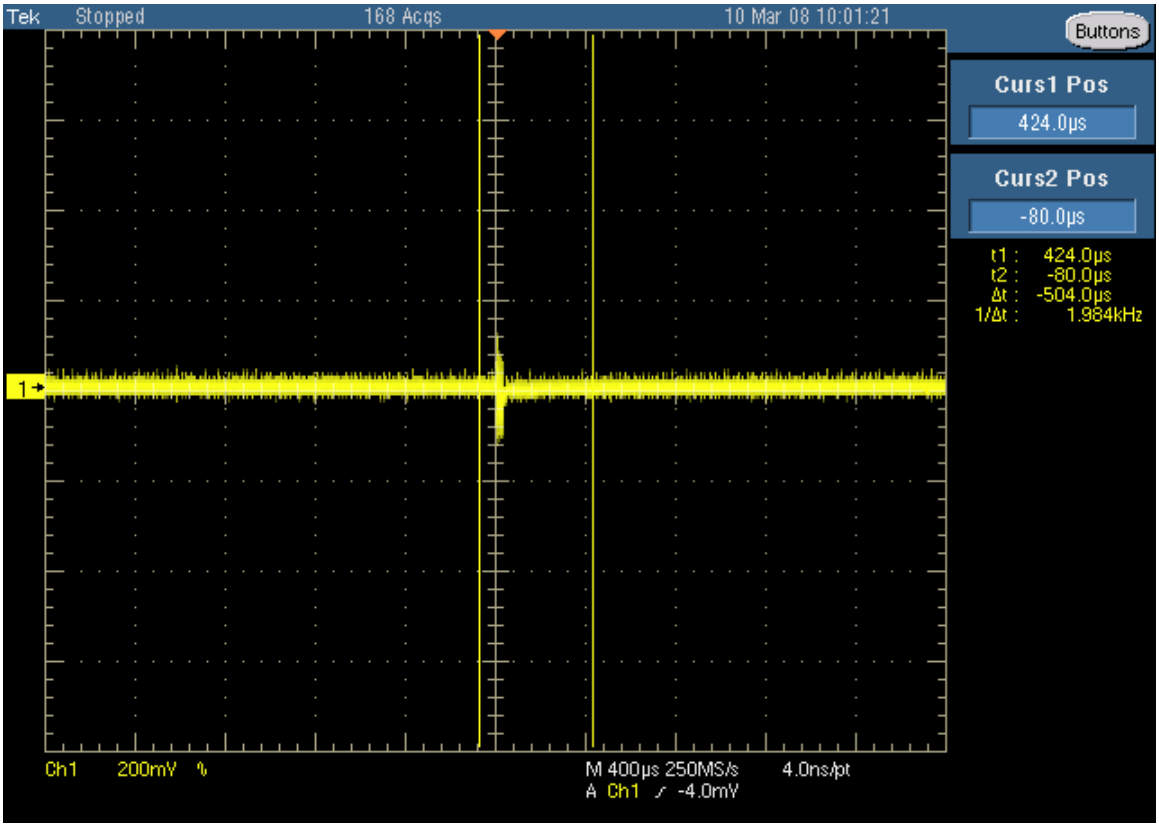



**Fig. 22. This is the same as fig. 21 except that the capacitor is connected directly to ground rather than across the power leads. The larger signal in fig. 20 shows that the inductance in the power return has a significant affect.**

The new capacitive filter eliminated most of the noise on the test stand. It had a much smaller effect in the detector – probably because the filter in the detector had to handle about 20 HDI's while the test stand one had to handle only two.

The above changes in the firmware and filter made substantial improvements in the data quality but did not eliminate large numbers of zero readings in the data. The zeros occur almost entirely on the pside readout (negative input signals). As mentioned above, they disappear if the preamp reset signal is eliminated in the firmware. We also found that certain values of the adapter card power supply voltage eliminated the zeros in the test stand. Fig. 23 shows a typical voltage scan. Fig. 23a shows the pedestal mean while fig. 23b shows the RMS of the pedestal mean. Note that the pside data (top row of 3 plots in both a and b) shows no increase in noise when the zero signals start. This indicates that it is a ring counter failure rather than coupling of noise into the front end. There is a small increase in noise on the nside detectors.

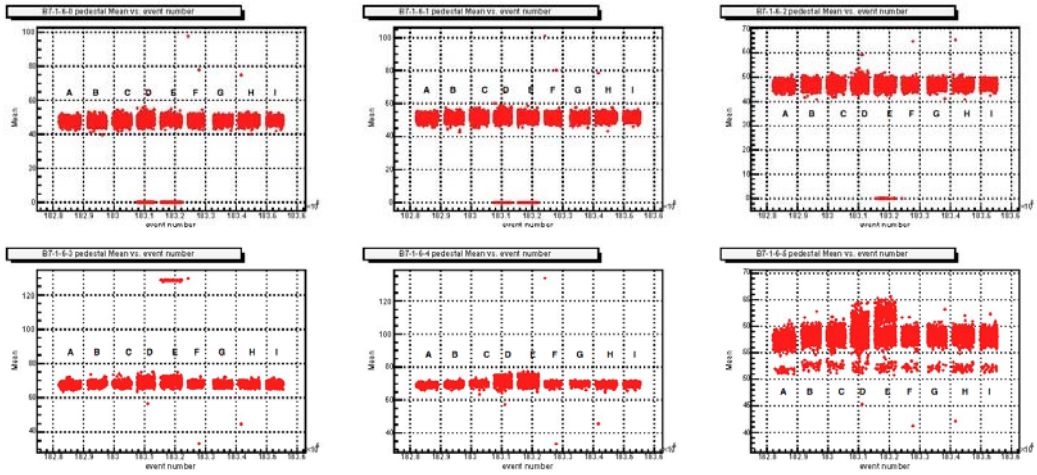


**Fig. 23a. Scan of the adapter card voltage from 4.6 to 5.4 volts in 100 mV steps. The x axis is event number which is proportional to time and the y axis is ADC counts. Each group corresponds to one setting of the voltage with group A at 4.6 volts, group B at 4.7 Volts, group C at 4.8 Volts and so on. One can see zeros in groups D and E (4.9 and 5.0 volts) on the pside detectors and increased noise for the nside ones.**

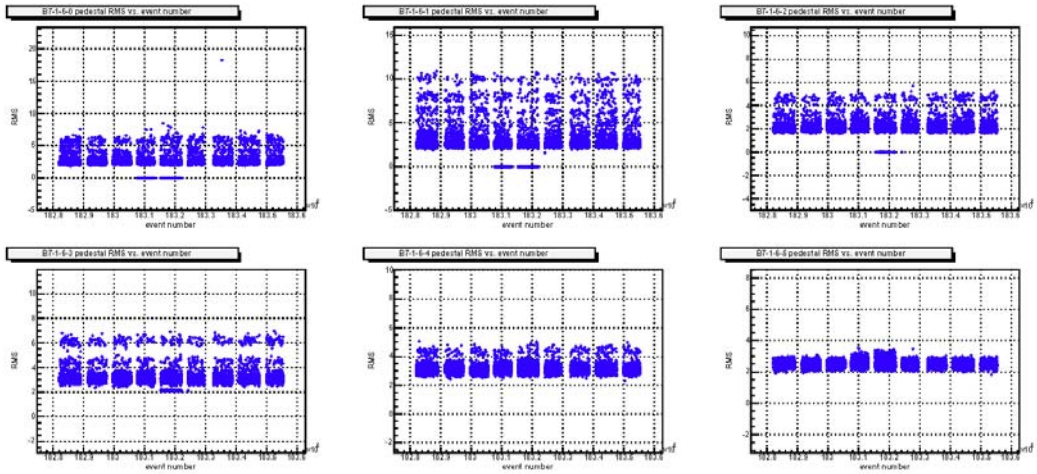


**Fig. 23b. RMS values of the data plotted in fig. 23a. Although some chips are noisier than others, only the lower right plot shows a clear indication of increased noise where the zero signals are.**

One striking feature of the data in fig. 23 is the disappearance of the noise with increasing adapter card voltage. One would normally expect that increasing voltage would lead to increasing noise which is what we see in the region leading up to the region with zeros. The disappearance at higher voltage is unusual. The cause is conduction of the protection diodes to DVDD. Fig. 24 shows a sketch of the preamp reset line on the SVX 2. The protection diode connects to the DVDD bus which acts as an AC ground for high frequency signals. When the preamp reset voltage is high enough (this voltage is controlled by the adapter card voltage setting), the diode starts conducting and drains away some of the signal to DVDD. This is very similar to adding the 20 pF capacitor on

the preamp reset line on the adapter card except that it only works for the positive edge of the signal.

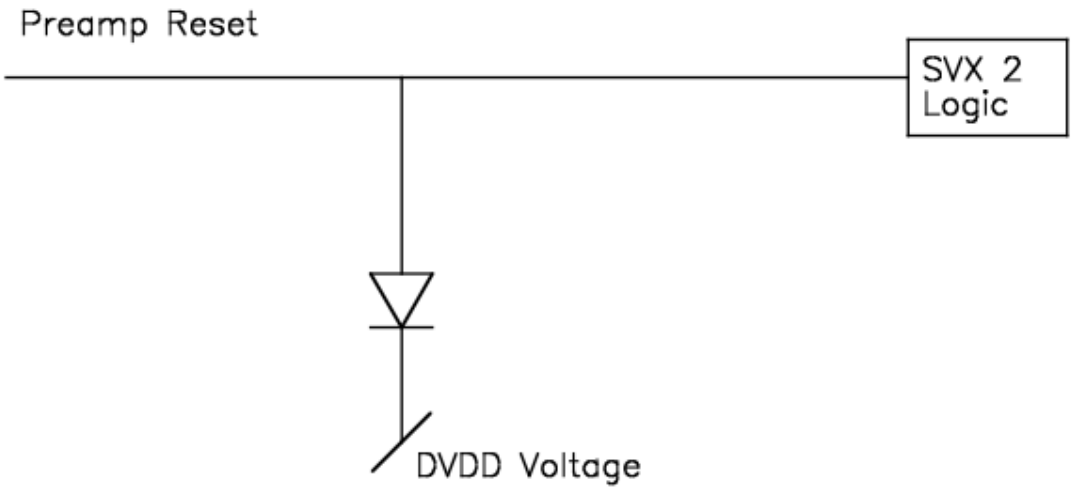



**Fig. 24. Sketch of the preamp reset input circuit on the SVX 2. When the preamp reset line voltage is high enough, the diode will conduct. This will shunt excess noise away from the SVX 2 logic.**

To test this hypothesis, we set up an HDI with the new adapter card on the test stand and set the adapter card voltage so that is was just above the zero region in fig. 23. We then raised DVDD by 100 mV. This should back bias the diode and cause the zeros to return and it did. Next we raised the adapter card voltage by 100 mV which should eliminate the zeros and it did. The diode is, indeed, providing an auxiliary ground. The mean of the pedestal for this test is plotted in fig. 25.

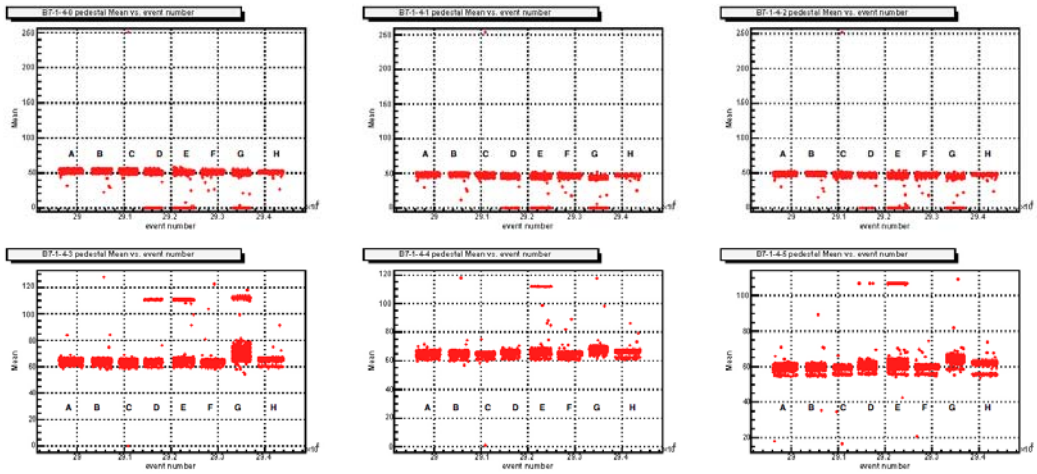


**Fig. 25. Plot of the mean value of the pedestal in ADC counts versus event number for different values of adapter card voltage and DVDD voltage. Groups D, E and F have Weiner voltages of 4.9, 5.0 and 5.1 volts. Note that the zeros go away at 5.1 volts as they do in fig. 23a. Group G has the**

**DVDD voltage raised by 100 mV and the zeros return. Group H has the Weiner voltage raised by 100 mV to 5.2 volts and the zeros again disappear.**

Tests with the actual detector were much less conclusive. The test stand data indicated that increasing the supply voltage gave the best results. When we increased the supply voltage in the detector we observed an increase in events with no zeros and an increase in events with nearly 100% zeros. The events with an intermediate number of zeros decreased. This indicated that there is still switching noise on the preamp reset line. We then installed a 20 pF capacitor between the SVX2 side of the switch and ground. This eliminated all of the zeros in the test stand. The results of a typical scan are shown in fig. 26. In fact, it eliminated the zeros on a second new adapter card that was connected to the same power supply. The most likely explanation for this is that the coupling noise is small and eliminating it on half of the adapter cards reduces the level on the other half to below threshold.

In summary changing the inductive filter to a capacitive one and adjusting the voltage improved but did not eliminate the zeros in the data and the other noise. The only thing that always works is to put the preamp reset back to the old signal. We used 4 lines originally because 4 were available. When we tried using only 3, the results were the same. Thus, we decided to modify all the new adapter cards so that only 3 lines are switched. This worked well on the test stand so we modified all the new adapter cards on the detector during a 1-week shutdown in October 2008. The results were striking. All the zeros and split pedestal problems disappeared. Fig. 27 shows a fairly typical before and after adapter card modification.

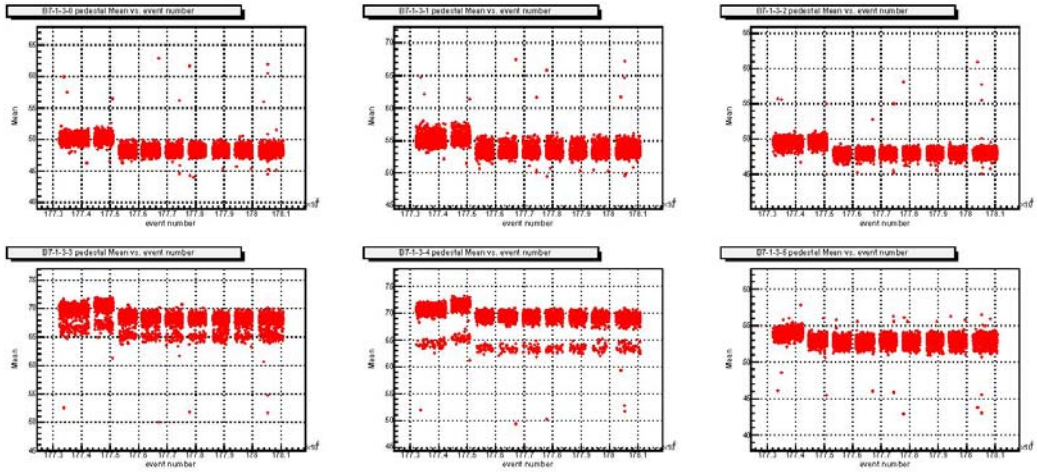


**Fig. 26. This is the same as fig. 23 but with the addition of the 20 pF capacitors on the adapter card. The 500 µF capacitors are on the filter card.**

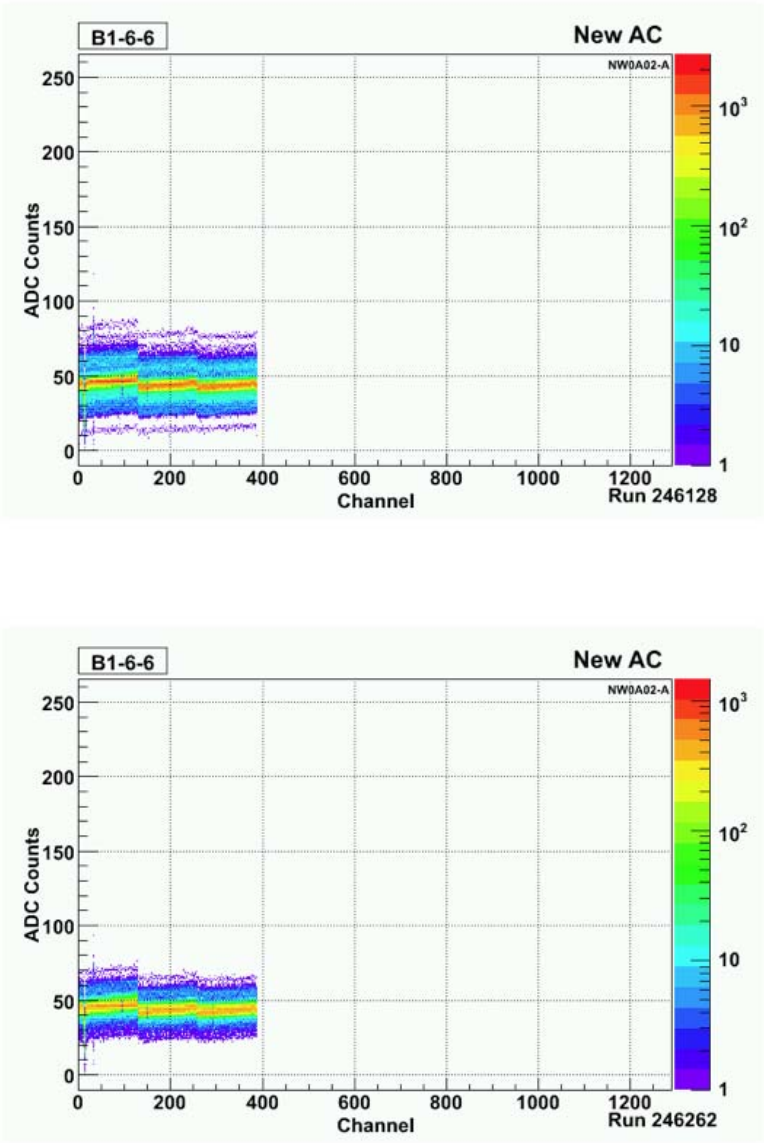



Fig. 27. Before (top) and after (bottom) modifying the new adapter cards. The noise in the pedestals is substantially reduced.

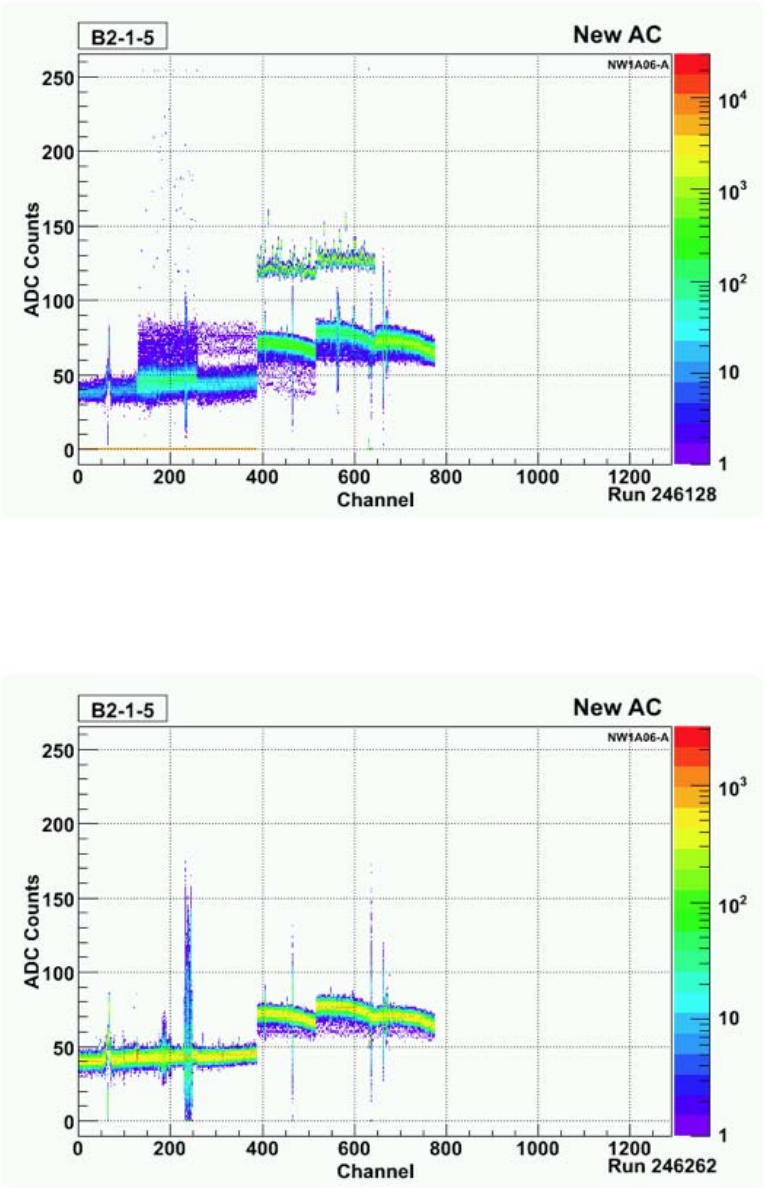



Fig. 28. A second example of the improvement with the new adapter card. Here we see substantial improvement in the split pedestals in the second half of the plot.

# V. Results

The primary failure mechanism appears to be a broken DVDD power bond caused by excessive current draw. The new adapter card only fixes a broken power bond and a new card was left in the detector only if it improved the HDI operation. We replaced 69

adapter cards out of a total of 111 broken HDI's (62%). Note that an adapter card services two HDI's and there are a few cases where both HDI's on an adapter card were bad. Thus, the recovery percentage for HDI's is a little greater than 62%.

Table I shows the number of HDI's that had a failure in the last chip and also the number that had a failure in some other chip. Based on the ratio of HDI's, the probability of having the last chip fail is 35%. However, if we take the total number of HDI's (63) and divide by the total chips (402) we get a failure probability of only 16%. That is, a uniform chip failure probability is 16% so we should have had only 10 HDI's with a last chip failure. The fact that we got 22 indicates that there is something unique about the last chip.

Table II shows the same data for HDI's involved in the incident. Both the uniform probability and the last chip failure probability are nearly the same as in table I. Table III shows the same data but excluding the incident HDI's. Here both the uniform probability and the probability of the last chip failing are lower. This indicates that there are other failures in the total sample.

Finally, Table IV shows the data where only one chip failed. Here 46% of the HDI's had a failure in the last chip. The uniform failure probability (16%) is the same as in the first two tables.

Table IV probably over estimates the last chip failure rate because a failure in the middle of a readout chain may cause an error in the next chip readout. The cause of this error is a delay in transmitting priority to the next chip which causes an interchange of data and channel ID. Nevertheless, there is a strikingly high failure rate in the last chip. The only difference that we can see is that the last chip drives one additional line (Priority Out) to the interface board.

| Entire Data Set | Number of HDI's | Number Of Chips | Last chip Failure probability based on HDI ratio | Last chip failure probability based on total chips and HDI's |
|---|---|---|---|---|
| Number of HDI's with last chip bad | 22 | 126 | 35% | |
| Number of HDI's with other bad chips | 41 | 276 | | |
| Sum | 63 | 402 | | 16% |

**Table I. This shows the number of HDI's with at least one failed chip where the chip failure was the last chip. It also shows the probability of a last chip failing based on the number of failed HDI's (35%) and based on the number of chips (16%).**

| Incident HDI's Only | Number of HDI's | Number Of Chips | Last chip Failure probability based on HDI ratio | Last chip failure probability based on total chips and HDI's |
|---|---|---|---|---|
| Number of HDI's with last chip bad | 11 | 63 | 35% | |
| Number of 's with other bad chips | 20 | 117 | | |
| Sum | 31 | 180 | | 17% |

**Table II. This is the same as table I but for incident HDI's only**

| Non incident HDI's | Number of HDI's | Number Of Chips | Last chip Failure probability based on HDI ratio | Last chip failure probability based on total chips and HDI's |
|---|---|---|---|---|
| Number of HDI's with last chip bad | 7 | 42 | 22% | |
| Number of 's with other bad chips | 19 | 147 | | |
| Sum | 26 | 189 | | 14% |

**Table II. This is the same as table I but for non incident HDI's**

| HDI's with only one chip failure | Number of HDI's | Number Of Chips | Last chip Failure probability based on HDI ratio | Last chip failure probability based on total chips and HDI's |
|---|---|---|---|---|
| Number of HDI's with last chip bad | 17 | 99 | 46% | |
| Number of 's with other bad chips | 20 | 123 | | |
| Sum | 26 | 189 | | 17% |

**Table IV. This is the same as table I but for HDI's with only 1 chip failure.**

The current draw by this driver is small so it is difficult to see how this can cause the wire bonds to fail.

In an effort to try to duplicate the failure mode of the incident, we stopped the 53MHz clock going to the SVXs during readout mode, when SVX current draw is the greatest. We set up a test in the test stand and halted the readout with 7 of the 8 output bits high but the wire bond did not open. We did see some unusual behavior in that the output lines dropped by themselves after about 750 mS. This time was not constant but differed from run to run by 20 or so mS. Priority Out stayed high and no clocks were issued to the chip. This does not follow from the logic of the chip. Perhaps there are other states in the chip that can cause momentary high current draws that open the wire bonds. In all of our tests at the test stand, we have never broken a wire bond.

We also checked the current limit on the interface board. It is set at 700 mA with a 100 mS time constant. Thus, the excessive current draw must occur in less than 100 mS or else the fusing point must be less than 700 mA. The wire itself most likely does not fuse below 100 mA but it may be possible that a defective wire bond might fuse. That could explain why we do not see any failures on the test stand.

Even though we have recovered a large number of HDI's, we have not recovered all of the chips on an HDI. First of all, we always lose the chip with the broken wire bond. Also, there appear to be other problems that cause readout failures. Overall, we have recovered 60% of all of the chips in the 111 HDI's that were listed as failed (552 out of 914 chips). This is the result of all repairs including clock lines, interface boards and sequencers. The largest fraction came from the new adapter cards. If we look only at those involved in the Aug. 30 incident, we recovered 58% (133 out of 914) chips. Not all of the HDI's were disabled because they did not down load so the above numbers overstate the amount of the recovery. Without the new adapter card the readout would have stopped at the chip with the broken wire bond. Thus the new adapter card usually increased the number of chips read out as well as providing a reliable download. The number of chips in this category is not readily available so we have only listed the number of chips recovered and the total number in all the failed HDI's.

# Appendix I

The following 4 tables contain a list of the failed HDI's for each of the quadrants of the detector.

Southeast Quadrant

| | New AC ? | Red=incident 0=dis 1=dwld ign Status | HDI | Adapter card | Clock Res | # chips recover | # of Chips | Comments |
|---|---|---|---|---|---|---|---|---|
| 1 | Y | 0 | B6-5-2 | 04A1 | ok | 1 | 3 | clock reterminated |
| 2 | No | 0 | B5-3-2 | 05A2 | ok | 0 | 9 | clock reterminated; bad dnld and LV trip on cal inject, but r/o all chips |
| 3 | Y | 0 | B6-7-12 | 06A2 | ok | 8 | 9 | |
| 4 | No | 1 | F10-2-2 | 06B1 | | 4 | 8 | no action taken; spontaneous recovery, but no chip 0x80 |
| 5 | No | 0 | F7-1-1 | 07A2 | | 8 | 8 | dnld and r/o ok (reseating low mass?); neighbor ok, but 0 pulse height r/o |
| 6 | yes | 1 | B6-7-3 | 10A2 | ok | 9 | 9 | read out all chips, dnld ok |
| 7 | yes | 0 | B5-6-1 | 11A1 | ok | 2 | 6 | dnld ok, multi-chip failures? |
| 8 | yes | 1 | B4-6-1 | 11A2 | ok | 3 | 6 | dnld ok, multi-chip failures? |
| 9 | yes | 0 | B4-8-1 | 12X1 | ok | 7 | 9 | dnld ok; 0x84 bad and maybe one more? 7-8 on scope; 7/9 on cal inj |
| 10 | No | 1 | B5-5-3 | 13B1 | ok | 0 | 6 | walking hdi ok; r/o 0x80-0x82 |
| 11 | yes | 0 | B6-5-4 | 17A1 | ok | 0 | 3 | dnld ok; one or two chips r/o chip 0x80 needs high thresh, chip 0x82 questionable |
| 12 | No | 1 | F12-2-4 | 19C1 | ok | 6 | 6 | clock reterminated; r/o all chips |
| 13 | No | 0 | F7-1-4 | 20A1 | ok | 8 | 8 | dnld ok, but cal-inject bad; tried 6 chip walking hdi |
| 14 | No | 1 | F8-2-3 | 21A1 | ok | 0 | 6 | dnld fails; no r/o; walking hdi is fine |
| 15 | yes | 0 | B5-8-3 | 25A1 | ok | 0 | 9 | fails dnld; LV trips; Walking HDI ok |
| 16 | yes | 1 | B5-8-4 | 25A2 | ok | 7 | 9 | dnld ok; r/o 0x80-0x86 |
| 17 | yes | 1 | B4-3-6 | 59A1 | ok | 8 | 9 | cal inject strange: timing problem (maybe seq firmware will fix) |
| 18 | yes | 0 | B5-3-6 | 59A2 | ok | 0 | 9 | 8/9 chips r/o ok |
| 19 | yes | 1 | B4-7-10 | 64X2 | | 8 | 9 | 8/9 chips r/o ok |
| 20 | yes | 1 | B4-5-11 | 67A1 | | 2 | 6 | 2/6 chips r/o ok 3rd chip has some problem; missing 4 chips |
| 21 | No | 1 | B5-6-10 | 67B2 | | 3 | 6 | 3/6 chips r/o; AC does not help |
| 22 | No | 0 | B6-3-6 | 68C2 | | 3 | 9 | r/o zero's after chip 0x82; timing problem at sequencer or VRB? |
| 23 | yes | 1 | B5-2-6 | 69A2 | ok | 5 | 6 | new AC improves dnld; befroe and after 5/6 chips r/o |
| 24 | No | 1 | B6-4-1 | 72B1 | ok | 6 | 9 | dnld ok; see 5 chips in scope and examine |
| 25 | yes | 0 | B5-6-11 | 78A1 | | 1 | 6 | chip 0xB1 looks bad on scope; later chips have chan id and data switched |
| 26 | No | 0 | B6-6-11 | 78B1 | ok | 3 | 3 | new AC does not fix dnld; possible outside issue |
| 27 | No | 1 | B4-6-12 | 80A2 | ok | 3 | 6 | new AC does not fix dnld; but walking hdi is fine; inside issue |
| 28 | yes | 0 | B5-5-1 | 80B1 | ok | 4 | 6 | new AC helps dnld; r/o funny (see elog); maybe IB issue? |
| | Total | | | | | 109 | 198 | |

Southwest Quadrant

| | New AC ? | Red=incident 0=dis 1=dwld ign Status | HDI | Adapter card | Clock Res | # recover | # of Chips | Comments |
|---|---|---|---|---|---|---|---|---|
| 1 | No | 0 | B5-1-3 | 03A2 | | 6 | 6 | dnld ok, so clock ok; new AC does not help |
| 2 | yes | 0 | B4-1-4 | 16A1 | ok | 5 | 6 | 5/6 chips in cal inj and on scope |
| 3 | yes | 1 | B5-1-4 | 16A2 | ok | 3 | 6 | 3/6 chips on cal inj; 5/6 on scope |
| 4 | yes | 1 | B5-3-3 | 18A2 | ok | 4 | 9 | new ac fixes dnld; does not readout; walking hdi is fine; outside issue? |
| 5 | yes | 1 | B4-6-4 | 26A2 | ok | 5 | 6 | dnld ok, read out 0x80 – 0x84 |
| 6 | yes | 0 | B5-5-5 | 26B1 | ok | 5 | 6 | dnld ok; scope fingers 0x81; cal inj fingers 0x80 and 0x82 |
| 7 | yes | 1 | B5-6-4 | 26B2 | ok | 5 | 6 | dnld and r/o all but 0x85 |
| 8 | yes | 0 | B6-4-3 | 27C1 | ok | 6 | 9 | readout 6/9 chips; also neighbor on AC; try setting high thresh on 0x86 |
| 9 | yes | 0 | B4-2-3 | 28A1 | ok | 5 | 6 | dnld ok; 5/6 chips readout |
| 10 | yes | 0 | B5-2-3 | 28A2 | ok | 5 | 6 | dnld ok; 5/6 chips readout |
| 11 | yes | 0 | B5-1-5 | 29A2 | ok | 5 | 6 | dnld ok; other chain on AC r/o only 0x8-0x82; scope sees 5 chips |
| 12 | yes | 0 | B6-6-5 | 36A1 | ok | 1 | 3 | only 1 chip reads out; dnld ok; sometimes 0x82 r/o |
| 13 | No | 0 | B5-8-5 | 38A1 | ok | 9 | 9 | all chips readout; dnld ok; no action taken |
| 14 | yes | 0 | B4-8-5 | 38X1 | ok | 8 | 9 | 8/9 chips readout; dnld ok |
| 15 | yes | 0 | B4-8-6 | 38X2 | ok | 8 | 9 | 8/9 chips readout; dnld ok |
| 16 | No | 1 | B4-4-4 | 42A1 | | 5 | 9 | strange cal-inject, possibly an IB issue |
| 17 | y | 0 | B6-4-4 | 42B1 | | 5 | 9 | r/o "full 5/6 chips" but 9 chips listed in db |
| 18 | y | 0 | B6-3-4 | 42B2 | | 1 | 9 | apparent bit failure in r/o; appears to be in detector |
| 19 | y | 1 | B5-2-4 | 43A2 | | 3 | 6 | r/o 3/6 chips; logbook did not specify which |
| 20 | y | 1 | B5-5-8 | 45X2 | | 3 | 6 | r/o 3/6 chips; logbook did not specify which |
| 21 | y | 0 | B5-6-7 | 52A1 | | 1 | 6 | only 0x80 and 0x81 r/o |
| 22 | y | 0 | B4-6-7 | 52A2 | | 1 | 6 | 0x80 r/o fine; 0x81 and 0x82 stuck bits; no other chips read out |
| 23 | yes | 1 | B4-8-7 | 53X1 | | 1 | 9 | no download, little data on cal inject. Replace AC, downloads ok. Cannot see data in error examine, but on cal inject r/o ~8.5 chips. |
| 24 | No | 0 | B4-5-9 | 54A1 | ok | 6 | 6 | clock reterminated; download and r/o all chips |
| 25 | yes | 1 | B5-5-9 | 54B1 | ok | 1 | 6 | B5-6-9 clock line damaged during ops, fixed, and all chips r/o |
| 26 | yes | 1 | B5-6-8 | 54B2 | ok | 4 | 6 | B5-6-8 may have shorted clock at IB end; replaced AC; replaced damaged clock board; |
| 27 | yes | 1 | B6-3-5 | 55B2 | | 1 | 9 | Replaced AC, downloads ok, readout is flaky, but works well if A and B channels are swapped at the AC. |
| 28 | yes | 1 | B5-2-5 | 56A2 | | 5 | 6 | replace AC, downloads ok, 5 chips r/o |
| 29 | yes | 0 | B6-7-9 | 60A1 | | 7 | 9 | replace AC, both download and readout ok. One and two chips bad, respectively |
| 30 | yes | 0 | B6-7-8 | 60A2 | | 7 | 9 | replace AC, both download and readout ok. One and two chips bad, respectively |
| 31 | No | 0 | F7-1-10 | 61A1 | ok | 8 | 8 | clock reterminated, no other changes; cal inject ok |
| 32 | yes | 1 | B5-6-9 | 65A1 | ok | 3 | 6 | clock lines were reversed; AC replaced; 3/6 chips r/o ok |
| 33 | yes | 0 | B6-8-10 | 66B2 | | 1 | 9 | chip 83 (maybe 80 also) need hight thresholds |
| | Total | | | | | 143 | 236 | |

Northeast Quadrant

| | New AC ? | Red=incident 0=dis 1=dwld ign Status | HDI | Adapter card | # chips recovered | # of Chips | Comments |
|---|---|---|---|---|---|---|---|
| 1 | Y | 1 | B3-1-2 | 03A1 | 3 | 6 | |
| 2 | Y | 0 | B3-3-2 | 05A1 | 0 | 9 | LV power trip. |
| 3 | Y | 0 | B2-3-2 | 05A2 | 6 | 9 | |
| 4 | Y | 1 | B3-2-2 | 15A1 | 6 | 6 | |
| 5 | Y | 1 | B2-2-2 | 15A2 | 4 | 6 | |
| 6 | N | 1 | B1-2-2 | 15B1 | 3 | 3 | Reconnected the clock cables and downloads fine. |
| 7 | Y | 0 | B1-3-2 | 19A2 | 0 | 9 | |
| 8 | Y | 0 | B1-5-3 | 24B2 | 1 | 3 | Chip 0x81 has strange readout in Cal Inject, Chip 0x82 nothing. |
| 9 | N | 1 | F2-2-4 | 25C2 | 0 | 6 | Need to reterminate non-marked clock cable. Fixed clock connector on 8/23/07. Dnld okay. Readout okay. |
| 10 | Y | 0 | B1-6-3 | 26C2 | 0 | 3 | |
| 11 | Y | 1 | B3-4-2 | 27A1 | 5 | 9 | |
| 12 | Y | 0 | B2-4-2 | 27A2 | 6 | 9 | |
| 13 | N | 0 | B3-7-2 | 32A1 | 9 | 9 | Dnld ok. Readout 9 chips. OPS database says it has increasing DVDD problems. |
| 14 | N | 0 | B2-7-2 | 32A2 | 9 | 9 | Dnld ok. Readout 9 chips. |
| 15 | N | 0 | F4-1-2 | 33C1 | 8 | 8 | Dnld ok. Readout 8 chips. |
| 16 | N | 1 | F4-2-3 | 34B1 | 6 | 6 | Dnld ok. Readout 6 chips. |
| 17 | Y | 0 | B3-8-2 | 36X1 | 9 | 9 | |
| 18 | Y | 1 | B3-6-2 | 37A1 | 5 | 6 | |
| 19 | Y | 1 | B3-5-12 | 39A1 | 5 | 6 | |
| 20 | Y | 1 | B2-5-12 | 39B1 | 5 | 6 | |
| 21 | Y | 0 | B1-5-12 | 39C1 | 1 | 3 | Channel id errors in third chip. |
| 22 | Y | 0 | B1-6-1 | 39C2 | 3 | 3 | Look at with scope when scaffold is high. |
| 23 | Y | 1 | B3-2-6 | 43A1 | 3 | 6 | |
| 24 | Y | 1 | B2-2-6 | 43A2 | 4 | 6 | |
| 25 | N | 0 | F5-1-12 | 48B1 | 8 | 8 | Dnld ok. Readout 8 chips. |
| 26 | N | 0 | F4-1-12 | 48C1 | 8 | 8 | Has HV problems. |
| 27 | Y | 0 | B3-6-12 | 52A1 | 3 | 6 | |
| 28 | N | 0 | B3-7-11 | 53X1 | 5 | 6 | Skipped. DVDD trip described as a problem in OPS database. |
| 29 | Y | 1 | B3-5-10 | 54A1 | 4 | 6 | |
| 30 | Y | 0 | B3-6-11 | 54A2 | 1 | 6 | Dnld fails with walking HDI. Dnld okay with new AC and detector HDI. CLKBAR okay. 84ns reflection on CLK. |
| 31 | Y | 1 | B2-5-10 | 54B1 | 1 | 6 | |
| 32 | Y | 1 | B2-6-11 | 54B2 | 5 | 6 | |
| 33 | N | 0 | F2-1-11 | 58B2 | 8 | 8 | |
| 34 | N | 0 | F5-2-12 | 62A2 | 6 | 6 | |
| 35 | N | 0 | F4-2-12 | 62B2 | 6 | 6 | |
| | Total | | | | 156 | 227 | |

Southwest Quadrant

| | New AC ? | Red=incident 0=dis 1=dwld ign Status | HDI | Adapter card | Clock Res | # recover | # of Chips | Comments |
|---|---|---|---|---|---|---|---|---|
| 1 | No | 0 | B5-1-3 | 03A2 | | 6 | 6 | dnld ok, so clock ok; new AC does not help |
| 2 | yes | 0 | B4-1-4 | 16A1 | ok | 5 | 6 | 5/6 chips in cal inj and on scope |
| 3 | yes | 1 | B5-1-4 | 16A2 | ok | 3 | 6 | 3/6 chips on cal inj; 5/6 on scope |
| 4 | yes | 1 | B5-3-3 | 18A2 | ok | 4 | 9 | new ac fixes dnld; does not readout; walking hdi is fine; outside issue? |
| 5 | yes | 1 | B4-6-4 | 26A2 | ok | 5 | 6 | dnld ok, read out 0x80 – 0x84 |
| 6 | yes | 0 | B5-5-5 | 26B1 | ok | 5 | 6 | dnld ok; scope fingers 0x81; cal inj fingers 0x80 and 0x82 |
| 7 | yes | 1 | B5-6-4 | 26B2 | ok | 5 | 6 | dnld and r/o all but 0x85 |
| 8 | yes | 0 | B6-4-3 | 27C1 | ok | 6 | 9 | readout 6/9 chips; also neighbor on AC; try setting high thresh on 0x86 |
| 9 | yes | 0 | B4-2-3 | 28A1 | ok | 5 | 6 | dnld ok; 5/6 chips readout |
| 10 | yes | 0 | B5-2-3 | 28A2 | ok | 5 | 6 | dnld ok; 5/6 chips readout |
| 11 | yes | 0 | B5-1-5 | 29A2 | ok | 5 | 6 | dnld ok; other chain on AC r/o only 0x8-0x82; scope sees 5 chips |
| 12 | yes | 0 | B6-6-5 | 36A1 | ok | 1 | 3 | only 1 chip reads out; dnld ok; sometimes 0x82 r/o |
| 13 | No | 0 | B5-8-5 | 38A1 | ok | 9 | 9 | all chips readout; dnld ok; no action taken |
| 14 | yes | 0 | B4-8-5 | 38X1 | ok | 8 | 9 | 8/9 chips readout; dnld ok |
| 15 | yes | 0 | B4-8-6 | 38X2 | ok | 8 | 9 | 8/9 chips readout; dnld ok |
| 16 | No | 1 | B4-4-4 | 42A1 | | 5 | 9 | strange cal-inject, possibly an IB issue |
| 17 | y | 0 | B6-4-4 | 42B1 | | 5 | 9 | r/o "full 5/6 chips" but 9 chips listed in db |
| 18 | y | 0 | B6-3-4 | 42B2 | | 1 | 9 | apparent bit failure in r/o; appears to be in detector |
| 19 | y | 1 | B5-2-4 | 43A2 | | 3 | 6 | r/o 3/6 chips; logbook did not specify which |
| 20 | y | 1 | B5-5-8 | 45X2 | | 3 | 6 | r/o 3/6 chips; logbook did not specify which |
| 21 | y | 0 | B5-6-7 | 52A1 | | 1 | 6 | only 0x80 and 0x81 r/o |
| 22 | y | 0 | B4-6-7 | 52A2 | | 1 | 6 | 0x80 r/o fine; 0x81 and 0x82 stuck bits; no other chips read out |
| 23 | yes | 1 | B4-8-7 | 53X1 | | 1 | 9 | no download, little data on cal inject. Replace AC, downloads ok. Cannot see data in error examine, but on cal inject r/o ~8.5 chips. |
| 24 | No | 0 | B4-5-9 | 54A1 | ok | 6 | 6 | clock reterminated; download and r/o all chips |
| 25 | yes | 1 | B5-5-9 | 54B1 | ok | 1 | 6 | B5-6-9 clock line damaged during ops, fixed, and all chips r/o |
| 26 | yes | 1 | B5-6-8 | 54B2 | ok | 4 | 6 | B5-6-8 may have shorted clock at IB end; replaced AC; replaced damaged clock board; |
| 27 | yes | 1 | B6-3-5 | 55B2 | | 1 | 9 | Replaced AC, downloads ok, readout is flaky, but works well if A and B channels are swapped at the AC. |
| 28 | yes | 1 | B5-2-5 | 56A2 | | 5 | 6 | replace AC, downloads ok, 5 chips r/o |
| 29 | yes | 0 | B6-7-9 | 60A1 | | 7 | 9 | replace AC, both download and readout ok. One and two chips bad, respectively |
| 30 | yes | 0 | B6-7-8 | 60A2 | | 7 | 9 | replace AC, both download and readout ok. One and two chips bad, respectively |
| 31 | No | 0 | F7-1-10 | 61A1 | ok | 8 | 8 | clock reterminated, no other changes; cal inject ok |
| 32 | yes | 1 | B5-6-9 | 65A1 | ok | 3 | 6 | clock lines were reversed; AC replaced; 3/6 chips r/o ok |
| 33 | yes | 0 | B6-8-10 | 66B2 | | 1 | 9 | chip 83 (maybe 80 also) need hight thresholds |
| | Total | | | | | 143 | 236 | |

# Appendix II New Adapter Card Schematic

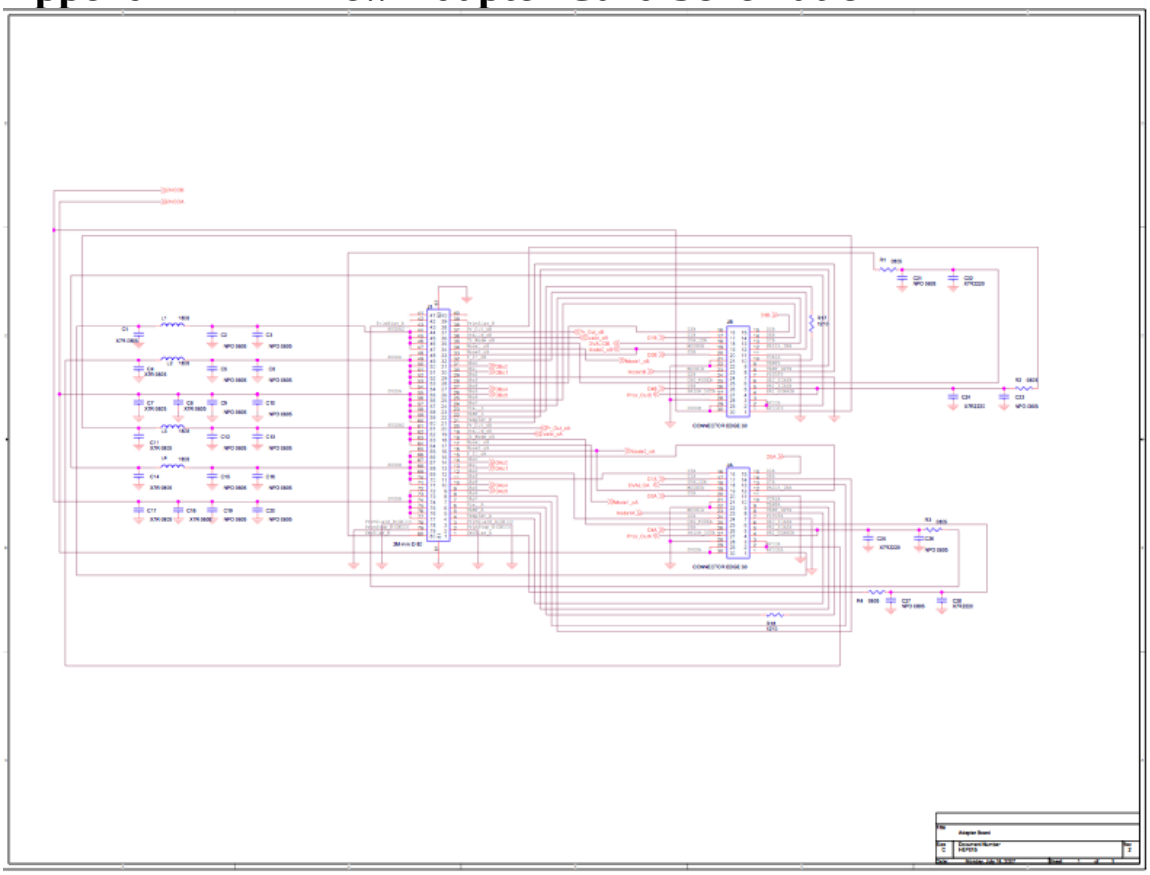


Fig. 1. The schematic is essentially identical to the old Adapter Card. For more detailed information see http://d0server1.fnal.gov/users/utes/webpage/svxfiles/AdapCardRev2_p1.pdf

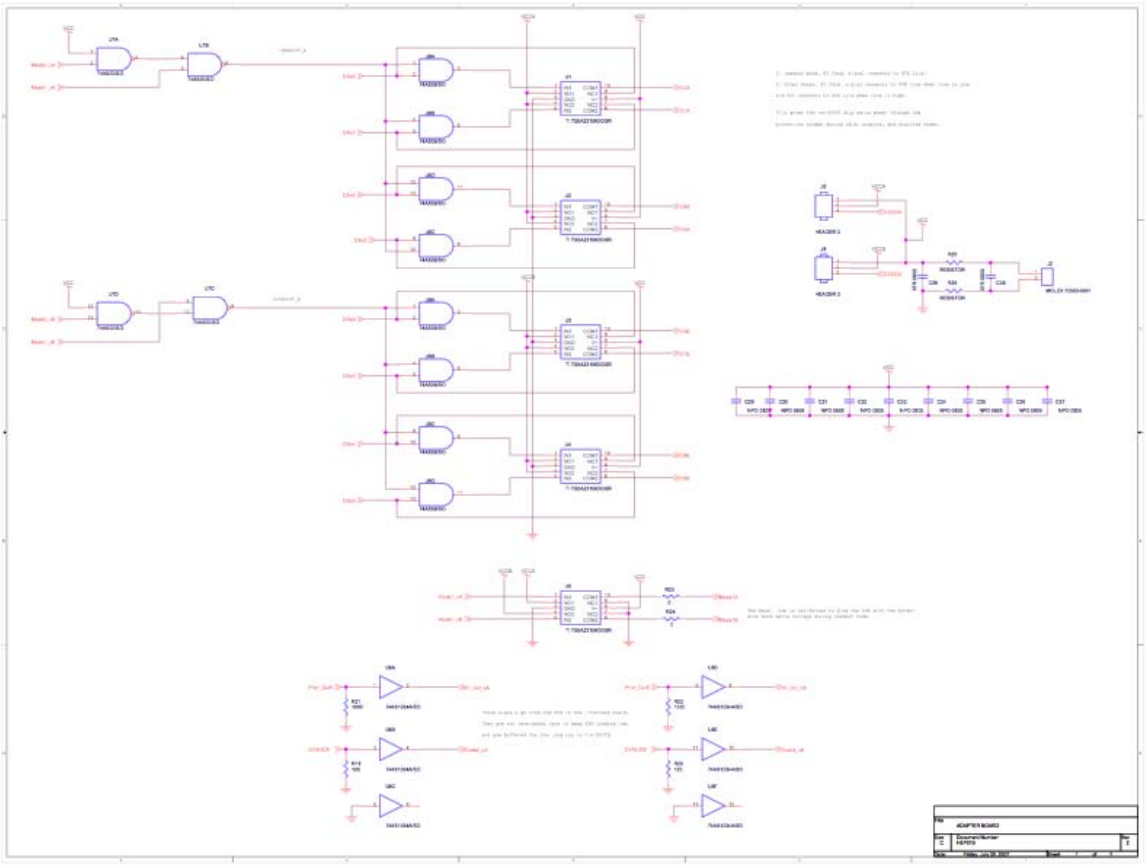


Fig. 2. New circuitry described in text that recovers broken HDI's. For more detailed information see http://d0server1.fnal.gov/users/utes/webpage/svxfiles/AdapCardRev2_p2.pdf