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1 OVERVIEW

The IHEP Test Beam system consists of five layers of silicon detectors arranged to form a small beam telescope. Each layer (Figure 1) employs three 640-channel silicon strip detectors left over from the DZero experiment at Fermilab, totaling 1920 silicon strips per layer. The strips are read out via wire-bond connections to VA1’ ASICs, which are 128-channel “sample and hold” chips that simultaneously store all channels’ charge when beam arrives, and hold each channel’s charge for later readout. Readout occurs by applying a 2.5MHz bipolar clock, each clock edge puts the next channel’s differential current on the output pins. There are five VA1’ chips residing on each of three Hybrid boards, which are mounted on a common frame with the detectors. The Hybrids also carry support components for the ASICs, including power supply bypassing, current sourcing for the preamplifiers and shapers, voltage biasing for the preamplifiers and shapers, and a temperature monitoring IC. Three hybrids connect, via 14cm long custom copper-over-kapton cables, to the Adapter Card. The Adapter Card supplies +2V and -2V power to the ASICs, buffers the control signals from LVTTTL to the +1.8V/-1.8V logic levels required by the ASICs, and translates the differential current output of the ASICs’ analog output into the differential voltage needed by the downstream ADC. The downstream ADC resides on another boardset directly connected to the Adapter Card called CAPTAN. CAPTAN is an expandable data acquisition and processing system which simply connects via Ethernet to a desktop computer. This board, when interfaced to software, forms the control signals needed by the ASICs, digitizes and stores the analog data coming from the ASICs, and interfaces to the temperature readout IC on the Hybrid. All boards are designed by Fermilab for low noise and simplicity of connection.

Figure 1. Block diagram of one layer of the IHEP test beam data acquisition system
2 SENSOR

2.1 Mechanical
The Sensors used for the IHEP project are silicon strip detectors left over from Dzero’s Run2B project at Fermilab. The active length is 98.33 mm, the active width is 38.372 mm, and the thickness is 320um. Strip pitch is 30um, readout pitch is 60um, and there are 639 channels.

2.2 Electrical Properties
These sensors are AC-coupled, single-sided single-metal p+ on n-bulk silicon devices with integrated polysilicon resistors. The depletion region is achieved with a nominal 120 Volts of bias. When a minimum-ionizing particle strikes the detector, the sensor produces electron-hole pairs and liberates about 3.5fC of charge per MIP. Leakage current is specified as <100nA/cm², junction breakdown >350V, 12pF/cm coupling capacitance, coupling capacitor breakdown >100V, and interstrip capacitance <1.2pF/cm.

2.3 Further Information
A link to Sensor testing results can be found at this link:
http://d0server1/users/utes/webpage/svxfiles/Talk_Aug21_final.pdf

3 HYBRID

3.1 Dimensions and Layer Consideration
The Hybrid’s nominal dimensions are 40.34mm by 55.5mm and the thickness is specified to be .062” +/- .005” (1.5748mm +/- 0.127mm). Signal trace width is 0.004” (.1016mm) and clearances are 0.0035” (.0889mm). Center-to-center ASIC distance is 7.6mm. The board is made of FR-4 and copper. There is no specification for controlled impedances due to the low frequencies involved; the main concern here is electric and magnetic field immunity and other noise reduction techniques. There are 347 holes and six conductive layers. Copper thickness per layer is 0.5 oz. copper, which is about 0.018mm thick. Layer assignment is as follows:

<table>
<thead>
<tr>
<th>CONDUCTOR LAYER</th>
<th>FUNCTION</th>
<th>DIELECTRIC LAYER SEPARATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>COMPONENT &amp; SIGNAL</td>
<td>0.012”</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>0.008”</td>
</tr>
<tr>
<td>3</td>
<td>VDD &amp; SIGNAL</td>
<td>0.012”</td>
</tr>
<tr>
<td>4</td>
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</tr>
<tr>
<td>5</td>
<td>GND</td>
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</tr>
<tr>
<td>6</td>
<td>GND &amp; SIGNAL</td>
<td>0.012”</td>
</tr>
</tbody>
</table>
3.2 VA1’ ASICs and Associated Circuitry

The detector signal is fed into the VA1’ ASIC made by Ideas ASA in Norway. It is a 128 channel low-power charge sensitive preamp/shaper circuit. Sampling of the detector signal occurs on all channels at the falling edge of a Hold signal, which should occur after a “peaking time” of 0.5 to 1 microsecond following beam arrival time. Readout of the 128 channels occurs serially during application of a readout clock. Nominal power levels are +2V and -2V +/- 10% although we have found that the chips seem to work at voltages as low as +/- 1.4V. Input logic levels are approximately +1.8V and -1.8V low. The analog output is a differential current with a specified gain of about 10uA/fC. Dynamic range is about 70fC in single polarity mode.

To see the complete documentation for this ASIC please refer to the link here:

www.ideas.no/products/ASICs/pdf/VA1prime_v0_92.pdf

3.3 Temperature Monitoring

Temperature is monitored by a Dallas Semiconductor IC called the DS28EA00 which measures from -40C to +85C, uses a 1-wire interface, and draws only 1.5uA standby current from the +3V supply supplied by the Adapter Card. Temperature readings are taken at intervals several seconds apart and are available in the data stream from the detectors. The 1-wire interface is involved and is handled directly by firmware in the FPGA on the CAPTAN board. The datasheet can be found here:

4 CABLE

4.1 Mechanical Aspects

The cable connects the Hybrid to the Adapter Card and is there to separate the Hybrid and Detector so that they can be more easily enclosed in the temperature-controlled box. It consists of two copper trace layers and kapton dielectric. One layer is solid ground plane; all other signals and power are on the other layer. The cable has redundant vias to increase reliability. Center-to-center distance between connectors is 5.0” (12.7cm) and overall length is 5.5” (13.97cm); width is 0.8” (2.03cm).

4.2 Electrical Aspects

Signal traces are approximately 0.006” (.152mm) wide. Voltage traces vary from 0.025” (.635mm) to 0.110” (2.8mm) in width. Copper thickness is 0.5 oz. copper (0.018mm).

4.3 Connectors

Connectors are Kyocera 24-5046-0506-00-829 and 14-5046-0506-30-829. Since pin 1 carries the detector bias, pins 2, 3, 4 and 5 have been removed to eliminate the possibility of arcing.
5 ADAPTER CARD

5.1 Dimensions and Layer Consideration

The IHEP Adapter Board interfaces three Hybrids to a CAPTAN board. This board measures 12.1 mm by 7.1 mm and is nominally 0.062" thick.

There are six layers with identical layer structure as the Hybrids; in fact they were manufactured on the same FR4 blanks. Traces are 0.004" and spacing is 0.0035". There is one adapter board per layer.

5.2 Control Signal Buffering

The Adapter Board translates the control signals' LVTTL logic levels coming from CAPTAN into +1.8V high/ -1.8V low logic levels compatible with the VA1' chip. This is done with simple op-amp circuits that provide clean edges and low noise.

5.3 Differential Analog Readout Signal Circuitry Buffering

Another function is to translate the differential current levels coming from the VA1' analog output into differential voltage acceptable to the ADC on the CAPTAN board. The differential current from the VA1' ranges from -200 μA to +200 μA, and the adapter card translates this into a differential voltage within the limits of the ADC, which is specified as 0 to 1.4 Volts with a midpoint of 0.7V. The gain factor here is about 4.

5.4 Power for the Adapter Card

Power requirements for the Adapter Card/ Hybrid assembly are +3.0V and -3.0V, current draw is approximately 0.69A and 0.96A respectively. The connection is made with a Molex 70553-0003 on the card and 50-57-9404 on the cable. The four connections are +3V, GND, GND, -3V. The wires should be twisted into two pairs and are 22AWG, therefore the DC power supplies connected to these cables should be current-limited to no more than 5.8A to prevent overheating in the event of accidental shorting of the two wires. Fuses on the Adapter Card protect its circuitry and are rated at 2A for each supply.

5.5 Power Regulation for the Hybrid

Clean power is provided to the Hybrid for powering the ASICs via linear regulators (LDOs). For providing +2V, there is one regulator shared by all three hybrids since the current demand is low, about 70mA. For the -2V supply there is one regulator for each Hybrid; the current draw is about 360mA. The components on these regulators were adjusted until the total noise was about 15 counts and the differential noise was about 10 counts. This is only about two counts higher than if separate +2V/-2V supplies are used. Using separate supplies is still an option. Ground posts are next to the power posts, separated by 0.1”. The posts are 0.025” square (.365mm), and twisted-pair wires should carry the current if these connections are used.

Note: The -2V regulator is referenced to the +3V supply on the Adapter Card. Please adjust the +3V supply voltage until the -2V on the Hybrid is the correct voltage.
6 CAPTAN

6.1 Overview

The CAPTAN system is a flexible and expandable DAQ system which interfaced to PC based systems through Ethernet.

For IHEP, CAPTAN consists of two octagon-shaped cards stacked together for each layer. From the PC, an Ethernet cable connects to the Node Processing and Control Board. Here, an FPGA handles communication and VA1’ control functions. Control signals are passed down to the Data Conversion Board, on which a 70-pin connector mates to the Adapter Card and supplies control signals to the Adapter Card and receives the differential analog information from the Adapter Card. These differential signals are received by an ADC which then sends digitized values back to the NPCB and this data then flows back to the PC. The power supply requirement for CAPTAN is 3.5V, 1A.

6.2 Link to Documentation

Some links to information about the CAPTAN system can be found here:

http://www-ese.fnal.gov/DIG_Test_Stand/docs/CAPTAN_SYSTEM_V1_0.pdf


APPENDIX

Links to Schematic Diagrams

A schematic diagram of the Hybrid can be viewed at this link:

http://d0server1/users/utes/webpage/svxfiles/IHEP_Hybrid_Sch.pdf

A schematic diagram of the Adapter Card can be viewed at these links:

http://d0server1/users/utes/webpage/svxfiles/IHEP_Adapter_Sch_p1.pdf

http://d0server1/users/utes/webpage/svxfiles/IHEP_Adapter_Sch_p2.pdf