



# Fermi National Accelerator Laboratory

## **Engineering Note**

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**Project: Detector Hybrids**

**Doc. No: U030408A**

**Subject: Considerations for making Ceramic Circuit Boards**

### **Introduction**

This note is intended to be used as a gathering point of information that is helpful for building ceramic circuit boards (hybrids) using thick film. These circuits are typically used for high frequency (to 100GHz), small detail, high accuracy, rigidity, high thermal conductivity, and low atomic cross section. Blind and buried vias are inherent in the process. Some drawbacks are that they are relatively expensive, can be brittle, and can have safety implications if Beryllia is used as a substrate.

The circuit boards we're familiar with are made starting with FR4 fiberglass clad on both sides with copper. The copper is coated with a photochemical, exposed to light through a Mylar sheet with the pattern of our desired traces, and etched. Holes are drilled and plated-through, and several such sheets can be sandwiched together to make a multi-layer circuit board. The thick-film process is different in that the dielectric and metal layers are applied one at a time as a paste and "fired" each step like typical ceramics to harden each layer.

### **Description of the Manufacturing Process**

The circuit starts out with a pre-purchased thin piece of either Alumina or Beryllia called a substrate. This acts as a flat working surface upon which the subsequent layers are built. Each subsequent layer is applied according to the customer's layout layers. In our case the first layer of metal paste is applied to act as a ground plane. It is then fired slowly in an oven with a precise temperature profile along the length of the conveyor, where the volatiles are driven off and only metal remains.

The next layer, a dielectric paste, is applied. These applications are squeegeed through a very fine stainless steel screen which has a polymer in the places where dielectric should not be present and can later be filled with metal. The pattern is usually just the via pattern. This process is inherently conductive

to blind and buried vias. Vias should be greater than 8 mils for reliability and typically have no annular ring.

Each metal layer and dielectric layer has its own such reusable screen. Pre-made screens are coated with a photo chemically-reactive polymer which is then hardened. Then the Mylar artwork layer from the customer is placed against the polymer and light is applied. A chemical is then applied to remove the polymer and only the polymer that was exposed to the light is removed. The result is a stainless screen with raised portions in the pattern of the artwork, again, usually just vias. This screen may be used to make all boards.

In the case of the dielectric layers, the screen is placed on the substrate or previous layer, and the machine applies the dielectric paste and at the same time squeegees the paste through the screen onto the board. The paste pattern remaining on the board is then fired and is ready for the next metal layer.

Another type of dielectric process is available using a photo chemically reactive dielectric paste from Dupont called Fodel. This process can make finer dielectric features but requires more steps. Here they spread the paste on the layer and fire it, then apply the customer's Mylar, expose it and etch the unwanted dielectric away. The paste is 7 times more expensive and the labor is 3 times more expensive. There may be slightly more warping using this technique.

For metal layers with feature sizes under 8 mils, a photosensitive paste containing gold or silver is applied and fired. The customer's Mylar layer is then applied and exposed to light and etched, leaving the desired traces. The next layer of dielectric may then be applied as described above, but this time the dielectric layer is also filling voids in the metal layer below.

For metal layers with larger feature sizes, they use a screen similar to the screen used for the dielectric, except it is "negative" in that the paste is allowed to penetrate only where traces are desired. The paste is squeegeed in and then fired to harden it.

In both cases, the metal paste will fill the via void in the dielectric layer below.

With respect to artwork necessary to accommodate their process, the main differences are:

- 1) They prefer Autocad .dwg files so they can tweak things prior to manufacture. We are fairly confident that a set of .dxf files generated by schematic-to-layout programs will be acceptable. Doing the job solely in Autocad seems crazy. CPT seems resistant to using our gerbers.
- 2) In addition to the typical metal artwork layers generated, their process also needs dielectric artwork layers, which typically consist of nothing more than vias.
- 3) Square vias are preferred so the surface tension of the paste achieved the correct shape and size.

This process may be repeated any number of times to create multilayer boards. When finished, the substrate is laser-trimmed to define the edge of the board. This trimming has a 2 mil tolerance.

## **Design Considerations**

Metal layers should be set back from the edges by at least 3 mils.

Dielectrics are applied at a minimum thickness of 30 $\mu$ m, and can go up to 60 $\mu$ m. Metal thickness can be 4-6 $\mu$ m for ground planes, but 7-9 $\mu$ m is typical as for traces.

Vias can be stacked but yield will be better when via stackup is minimized.

Ultrasonic cleaning is not recommended since it will peel up the metal.

Capacitors and resistors may be printed onto the circuit boards using their pastes.

Platinum/palladium silver is used for soldering applications; silver or gold are good for aluminum-wire bonding.

These manufacturers like to talk in mils, not microns. The only time they mention microns is sometimes in layer thickness.

Resistors may be printed with values between 1 $\Omega$  and 10 M $\Omega$ . Capacitance values are available from 5pF to over 200pF.

Thru holes are 0.007" diameter  $\pm$  0.001".

## **Manufacturers**

Amitron Inc. North Andover, Ma. <http://www.anaren.com/products/substrates/>

CPT, Inc. Oceanside, Ca. <http://www.cptcircuitry.com/web/cptcircuitry.nsf>

Halcyon Microelectronics, Inc. Irwindale, Ca. [http://www.halcyonmicro.com/contact\\_us/index.html](http://www.halcyonmicro.com/contact_us/index.html)

Scrantom, Inc Costa Mesa, Ca. <http://www.scrantom.com/about/>

## **Cost Factors**

The easiest way to drive the cost up is to blindly build what the physicists want. The other easiest way to drive cost up is to make the feature size required of the dielectric layers too small. Keeping the vias at least 8 mils square and their separation 10 mils will allow the manufacturer to use standard screen-printing of dielectric layers, avoiding the use of Fodel, which is an expensive dielectric that is etched once the layer is applied.

Using larger feature sizes in the metal layers can also save money by eliminating the etching of each metal layer. 5 mil traces and 6 mil spaces can generally allow the manufacturer to screen-print the metal layers.

Another way to drive the cost up is to set specifications that reduce yield. These circuits are brittle and specifying a very thin package can lead to breakage during manufacture and result in lower yield.

Strict warping requirements will affect cost. A warp requirement of 70 microns over a board length of 5 cm seems to be reasonably achievable.

Beryllia is sometimes used as a substrate because of its low Z, high thermal conductivity, and resistance to warping, but it is made only by Brush-Wellman and is expensive. It is also hazardous and special handling, cleaning and testing must be done if it is used.

Drilled holes will increase the cost.