

# Considerations for proper operation of HP G-Link Transmitter

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- Low jitter clock
- Isolated power plane under chip with C-L-C filter connecting power to plane
- No foreign traces near the circuit
- The ground plane is common, but ground slits are recommended to prevent stray currents.
- Good layout of destination terminations into chip.
- The G-Link required a 10-ohm resistor *in series with* a 0.1uF to bypass each Vee/Gnd pair of pins. They reduce excessive ringing caused by current spikes generated by the parasitic inductance in the ECL Gnd leads.

See figure 20 of page 38 of the G-Link datasheet. Note the position of Gnd and Vee.