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Engineering Note

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Project: SMT Operations

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Subject: Sequencer and Controller modifications to prevent SVX damage due to loss of heartbeat

Introduction

In August of 2006 several HDIs in the SMT system were rendered useless because part of the Trigger Framework system tripped off, causing a halt of the heartbeat signal. The heartbeat is an occasional signal provided to the SMT Sequencers if actual Level 1 triggers stop. Either a trigger or a heartbeat is needed by the SVX chips to keep the DVDD current from getting high enough to possibly cause failure of the wire bond carrying power to the chip. The most likely mechanism for this behavior is described in DZero note 5697, which also describes how we used a modified Adapter Card to restore operation of the damaged HDIs.

Prevention of a recurrence

The modifications to the Sequencer and Sequencer Controller are summarized as follows:

In the Sequencer Controller, we glued a watchdog timer IC to the board with two wires connecting it to the NRZGenB EPLD. The first wire coming from the EPLD carries the logical OR of Level 1 Accept and the heartbeat. Either one of these signals will reset the countdown timer of the watchdog; if there is no reset for approximately 90 seconds, a pulse will emerge from the watchdog and go to the EPLD via the second wire. If this occurs, a “trip” code (hex code C) will be sent to the Sequencers via the NRZ link on the backplane. The HDI Control EPLD receives this code and sends a signal to the 1553 FPGA, which controls the HDI on/off bits going to the Interface Board. The 1553 FPGA runs a state machine that runs a brief sequence controlling the chip enable, clk, and data lines of U33 and U505 to lower the HDI_ENx bits to the Interface Board. Since this is a retrofit, a previously unidirectional line “Shadow” was made bidirectional in

order to avoid having to solder a wire onto each of the 120 Sequencers. The new logic is designed so that the bidirectional line is tri-stated normally and floats low.

After downloading an HDI the shadow registers in the SVXs must be pulsed, so now this bidirectional line is pulled high by the 1553 FPGA and shadow register bits are written just as they were before the modification. If a trip situation ever occurs, the Control EPLD will pull the bidirectional line high and that is a signal to the state machine in the 1553 FPGA to drop the HDI_EN lines to the Interface Board.

Since the pins are very closely spaced on the EPLDs, we wanted to avoid soldering a pull-down resistor to the bidirectional line. As a result, the line drifts to a low level relatively slowly, about 30 ms. This decay time can interfere with downloading by corrupting reads done during the decay time. It will also cause the power to trip during downloading because we must pulse the shadow register by pulsing this bidirectional line.

To avoid this situation I added logic that disables the power trip function; one does this by writing a high to bit D00 of Subaddress 21 of the Sequencer. Downloading can then proceed without corruption of SVX readback or tripping power. Once downloading is finished, one can then enable the power trip capability by writing this bit low. These modifications require us to replace the 1553 FPGA programming PROM for each Sequencer. The firmware changes require downloading the NRZGEN PLD in the Controller and the Prtrcd PLD in the Sequencer via the JTAG connectors.

Bit for detecting trips

Bit D3 in the Sequencer Controller's Control/Status register (subaddress 1 for left half of crate and 16 for right half of crate) will go high if a trip is generated. This is latched high until reset by writing bit D3 low via 1553.

Some notes on operation

The watchdog chip is the Maxim MAX6372, which has a timeout from 90 – 120 seconds. Any trigger, including Level 1 Accepts, software-generated triggers, or front panel triggers will reset the timeout. A logic low level out of the chip indicates a trip and typically lasts for about 1.7ms. The Sequencer system must be in Acquire mode to recognize this trip. HDI power will be shut off approximately 3us after the watchdog timeout pulse. Note, we are also considering having a no-sync condition on the NRZ link to cause a trip of the HDI power.

Firmware on Server

The firmware used for this upgrade changes three EPLDs. All files can be found at D0Server6\Projects\Electronics\Run2B_Firmware in the following directories:

	Original file	Modified file
Sequencer Controller NRZGen	NRZGenB_011508	NRZGenB_020209
Sequencer HDI Control	Control_042706	Control_041008
Sequencer 1553	1553_11_27_02	1553_041008

Conclusion

Added system protection has been achieved by adding a feature to power off the HDIs in the event of a heartbeat failure. This had been achieved by a minor physical modification to the Sequencer Controllers and reprogramming three PLDs. These mods should prevent future occurrences similar to what happened in August of 2006.