D0 Engineering Note #U960913A

SVX2E ASIC Testing Results

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Introduction

The SVX2E Chip testing was begun immediately after arrival from the manufacturer beginning on August 18, 1996. Testing was done at full speed, i.e., 132ns interaction interval, 53MHz digitization clock, 26Mhz readout clock, using the version 1 prototype data acquisition electronics designed for the Silicon and Fiber Tracker systems. Three chips were initially tested. Each was mounted on custom test boards designed at LBL which allow for any necessary capacitors and resistors, and a header for connecting to a 28' cable that runs to the DAQ system. This is close to the length of cable needed between the chips and DAQ system in the final detector installation. The DAQ system consisted of the Port Card, SAR, SAR Controller, VBD, and BIT 3 PC Interface all housed in a VME crate interfaced to a PC running a Microsoft Excel spreadsheet. See figure 1. The spreadsheet uses a Visual Basic routine to control the various boards in the crate. The chip is thus cycled through the initialize, acquire, digitize, and readout modes, and the computer records and plots the chip's data.

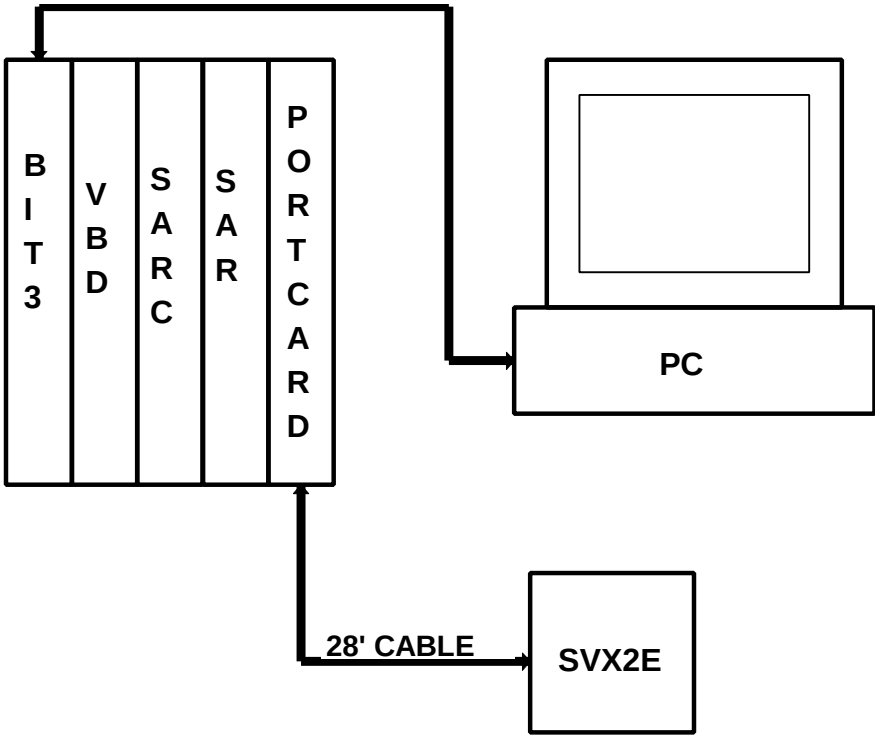

Figure 1. Setup for testing the SVX2E Chip

Test Results

1) Initialization The chip initializes correctly and the Bottom Neighbor pin successfully drives the initialize bit stream back to the Port Card.

2) Chip ID The first byte of information during the readout mode is Chip ID, and was correct for all values loaded into the chip.

3) Calibration bit mask Any or all channels can be selected during initialize to receive the Calibration pulse. This feature is functional.

4) Polarity Four bits, namely calibration polarity, pipeline polarity, comparator polarity, and ramp polarity all behaved properly.

5) Preamp Bandwidth There are six bits for this in the initialization bit stream giving 64 possible settings. Recommended settings are as follows:
132ns interaction interval with 10pf input capacitance: Use a setting of 12
132ns interaction interval with 30pf input capacitance: Use a setting of 0
396ns interaction interval with 10pf input capacitance: Use a setting of 24
396ns interaction interval with 30pf input capacitance: Use a setting of 8

6) Pipeline Depth There are five bits for this in the initialization bit stream giving 32 possible settings. Each setting represents a different pipeline storage capacitor; The setting chosen will determine the capacitor from which to digitize charge, and since a different capacitor is used for each subsequent beam crossing, this setting represents the number of crossings elapsed between an interaction and when the trigger is received at the chip. All settings are functional.

7) Chip Current or Master Bias Current Multiplier is used to account for process variations from chip to chip. There are three bits for this in the initialization bit stream giving eight possible settings. An external pulse was injected into one channel and the number of counts was recorded as Chip Current was varied. Each incremental setting gave about a 6% change in the pulse height. See Figure 1.

8) Cal Voltage There are three bits for this in the initialization bit stream giving 7 possible settings. By using this feature, a calibration pulse may be injected into any or all channels without the use of external pulser equipment. When the chip was set up to give 250 counts for 90fC of charge, the Cal Voltage feature gave seven useful points in either positive or negative mode. See figure 2. The minimum pulse was about 10 counts over pedestal, the max was just full scale at 255 counts. Note that a setting of zero here allows the use of an external voltage for the Calibration pulse.

9) ADC Pedestal This feature allows the adjustment in the number of counts given during data readout for channels that have no hit. This parameter affects all 128 channels equally, and there are sixteen possible settings. It was designed so that the eight middle values would be a vernier. This vernier was measured to be about 0.3 counts per setting, while the non-vernier range gave wide swings of about 20 counts per setting (Figure 3).

10) Read All One bit for either forcing the chip to read all channels or just those over threshold. This feature was functional.

11) Read Neighbor One bit for having the chip read out the channels on either side of a channel whose value was over the preset threshold. This feature was functional.

12) Last Chip This feature forces the last chip in a string to read out channel 127, signalling to the VRB module that the readout for that string is complete. This feature was functional.

13) Ramp Trim Adjusts the gain of the ADC by providing a settable capacitance on the circuit that determines the ramp rate for the Wilkenson A/D converter. There are eleven bits for this in the initialization

bit stream giving 2048 possible settings. There was ample range in the settings available, and some suggested settings are:

Charge to get 255 counts	Ramp Trin in hex	Ramp Trim in decimal
24	790	1936
90	250	592
270	180	384

14) Threshold is a gray-encoded eight bit number that is used by the chip to determine the channels to read out in sparsify mode. A few values were chosen to test this feature and operation was correct.

15) Counter Modulo is a gray-encoded eight bit number that determines the maximum value to which the chip will count. Maximum value (255 counts) is 80 in gray hex. Counter modulo is functional.

16) Maximun Speed of Operation The master clock used by the data acquisition system will be about 53.105 Mhz. The chip will receive this clock during digitize mode, and since both edges of the clock are used, the digitization rate will be 106.2 Mhz. The clock during readout is half the master clock frequency, but again, both edges of the clock are used. Alternating bytes of chip ID and data therefore appear on the bus every 18.8ns. Our system including the SVX2E chip operated error-free at master clock frequencies up to 63.2 Mhz. The system continued working with some errors up to almost 77 Mhz, but the logic analyzer showed the chip itself was still operating correctly. See Figure 4. At 80 Mhz, the system could no longer stimulate the chip properly, so the maximum operating frequency of the chip was not determined.

17) Dynamic Range of the Preamp This was measured to be 270fC for both positive and negative pulses. The measurement was done by using two separate pulses occurring in consecutive pipelines, much the same as the chip will operate in the collider. Figure 5 shows the Preamp response to increasing single pulses. The limitation seen in positive mode is due to the slower response time of the preamp to positive pulses.

18) Dynamic Range of the Pipeline The pipeline is linear to approximately 110 fC for both positive and negative pulses. See Figure 6.

19) Gain at the output of the pipeline is 12.9 mV per fC.

20) Pedestal uniformity Intrinsic to the chip, the pedestals are all the same to within one count for 100 samples (Figure 7). With two detectors bonded and biased to 30 volts, the channels' pedestals are the same to within about two counts. Noise is about three counts. See Figures 8 & 9.

21) Linearity was measured for both positive and negative modes and at various full-scale settings of the ADC. Results are shown in figures . Results show that the linearity is very good up to about 170fC. Figure 10 shows a typical linearity plot with fit superimposed.

22) Crosstalk was measured to be 0.2% in both positive and negative modes at the output of the pipeline. Figure 11 shows the effect at the output of the ADC.

23) Black Hole Effect When a silicon strip fails in such a way that it becomes shorted to the detector bias, thirty volts could be applied, through one or two megohms, to the input pin of a channel. Steps were taken to make sure that this relatively large current does not affect the operation of nearby channels. One was to stagger the placement of the input-overvoltage protection diodes at the input side of the chip. Another was to provide a small diode on each channel, the anode of which is connected to the channel's input, and the cathode connected to a common voltage of 4.3 volts provided by a resistor divider. This diode would shunt away any small DC current travelling through the overvoltage protection diodes from a nearby channel shorted to the bias. The diode, however, turned out to be a transistor and the resulting current was large enough to overpower the resistor divider, and the effect was that the black hole effect was not diminished adequately. See figure .The solution was to tie the middle of the voltage divider, which is available as a bondable pad, to AVDD2. Implementing this fix, the black hole effect does not occur for input currents of at least 50uA. See figure 12.

24) Chip recovery at high trigger rates The chips show no noticeable change in performance when retriggered within 13.5us of a previous trigger. This is the fastest rate we can achieve with our system to date. The minimum time from a trigger to the end of readout is about 10 us.

Further Testing will be done when HDIs designed for SVX2E chips arrive. Pedestal uniformity, noise, and speed margin will be more meaningful with this arrangement, as well as determining the drive capability of the DAQ system and the SVXs when more that two chips are on the bus.