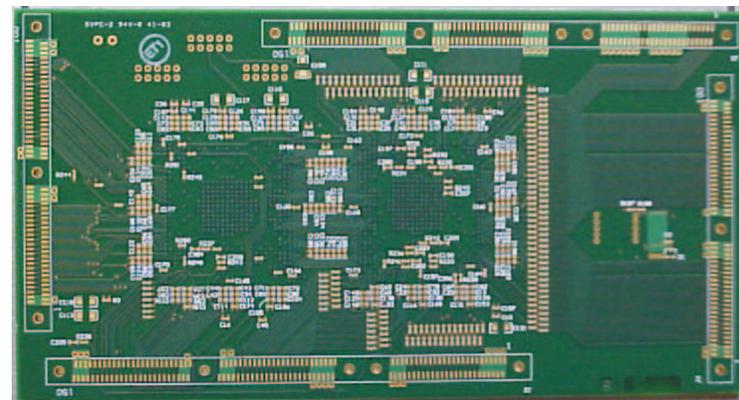
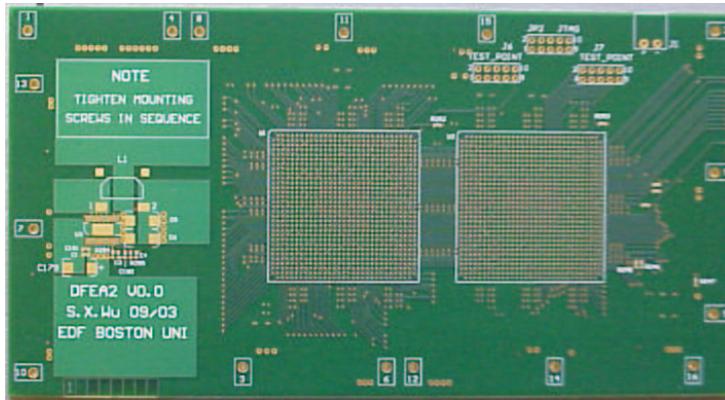




L1 Central Track Trigger

(from Vivian's plenary talk)

- Digital Front End Axial (DFEA) daughter cards redesigned with larger FPGA's (Xilinx Virtex-II XC2V6000)
 - Allows more complicated equations for using narrower (singlet) roads
- Implemented prototype firmware (Boston U)
 - Includes equation files from all 4 momentum bins
 - DFEA logic is implemented in two FPGAs
 - Prototype board functionality tested
- Hardware, Firmware and software components progressing on schedule





L1 CTT Rescope

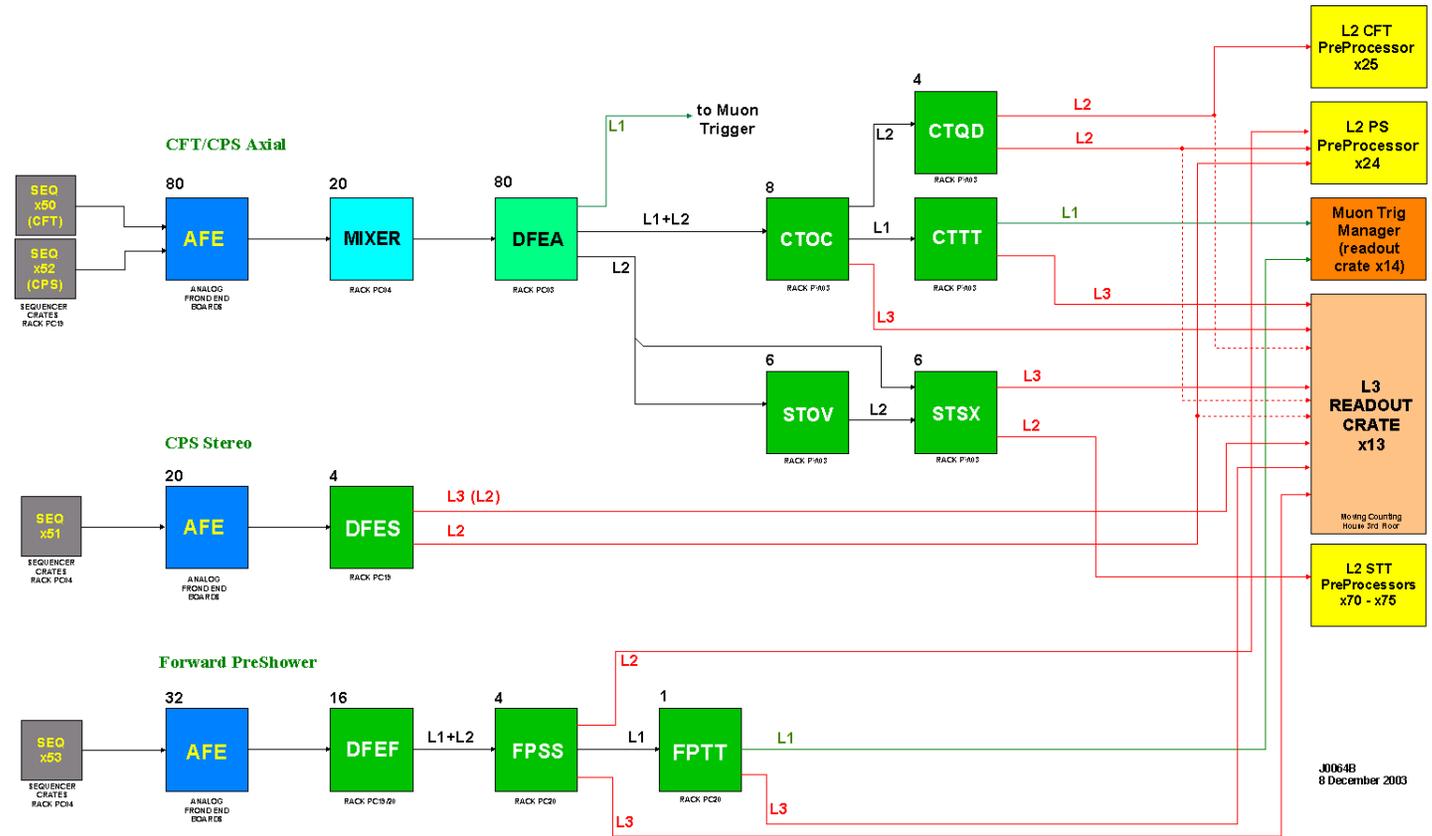
(from Vivian's plenary talk)

- In order to add testability to the system:
 - A new motherboard (daughterboard – to a less extent) design.
 - Improved diagnostics: input and output buffers, and L3 capability.
- To alleviate colossal download times:
 - A new DFE crate controller with a faster connection to the D0 online computers.
 - A new DFE backplane design
 - Utilize this chance to put the cables to the back.
 - No transition boards.
- Plan to run on a partial crate of the new system on the platform in parallel with the existing DFEA using LVDS splitters
 - Key to successful commissioning of the new system
- Advantages:
 - Can assemble the whole crate outside of the collision hall
 - Extensive testing of the entire chain possible before putting in collision hall
 - Take out the old crates (2 of them) and replace them with new ones
 - Use the existing Run2a tools used for commissioning
 - Low level changes will be transparent at user level
- Proposal reviewed April 5, approved by directorate end of April



CTT Upgrade: Overview

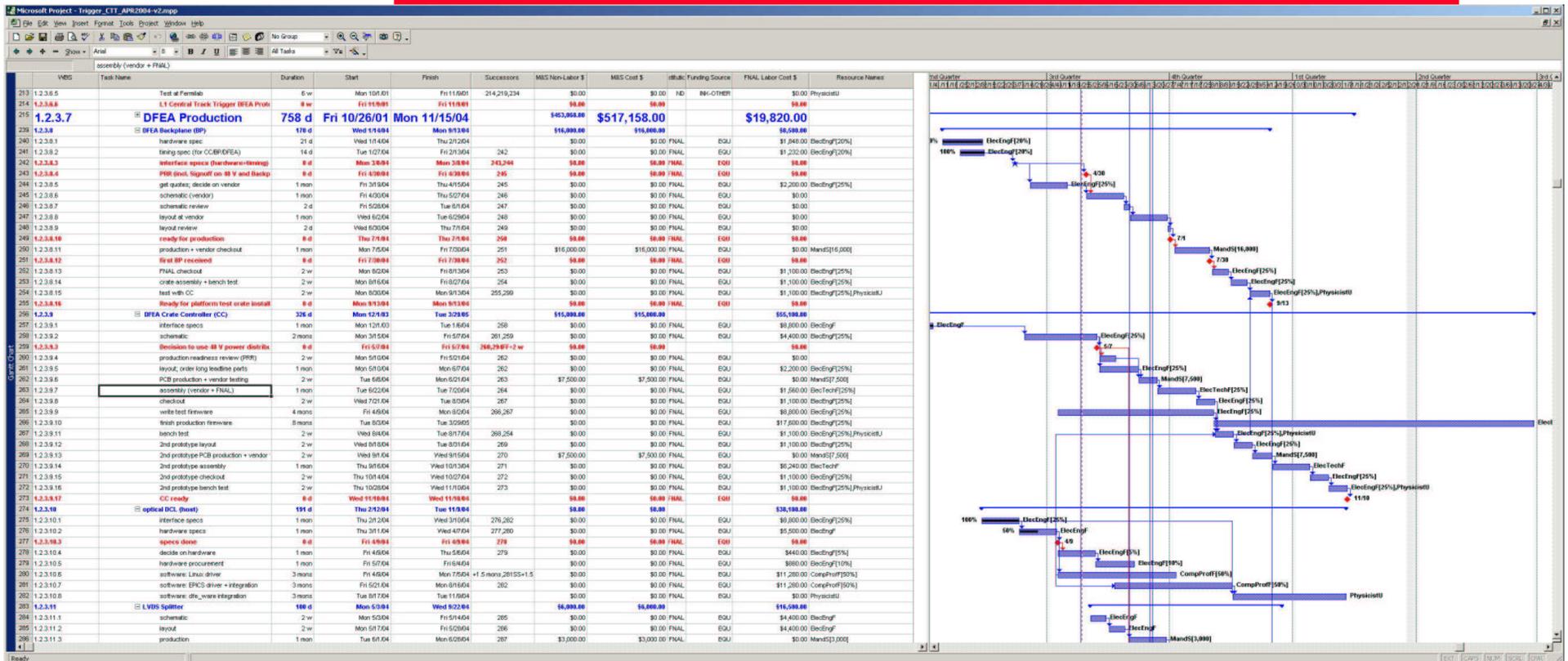
- New DFEAs (DFEB ?)
- Sequence:
 - Standalone tests (enhanced by new I/O buffers on board)
 - Test stand (chain with few AFE/Mixer/CTOC)
 - Partial parallel chain on platform



Parallel chain: (AFE-MIXER)-Splitter-DFEB-CTOC-(VRB in x13) and -CTTT-(VRB in x13)



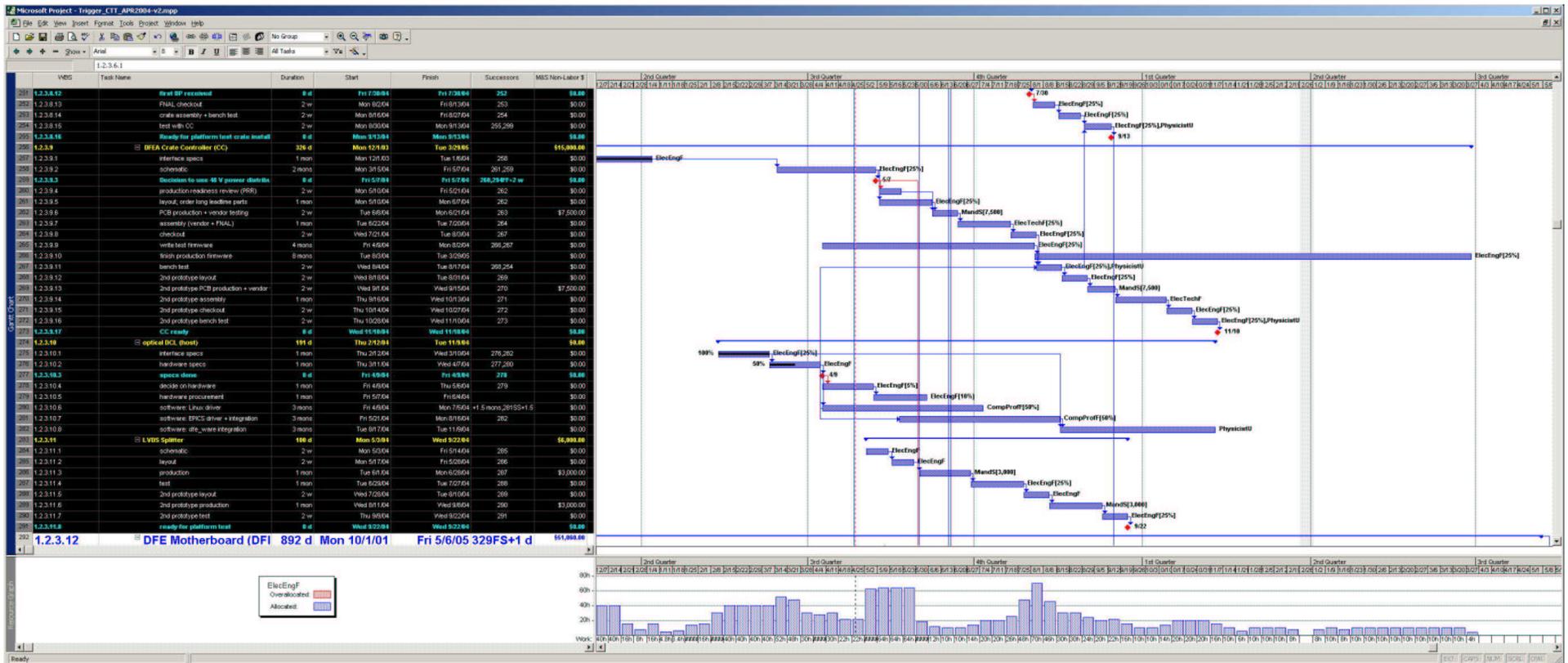
CTT Upgrade: Schedule I



- Not shown: sequence of DFEA prototypes (3) and DFEA production and testing. Progressing on (long established) schedule. Prototype 2 will be used on the platform in the Fall.



CTT Upgrade: Schedule II



- Backplane (new crate) and Splitter are the critical projects for installation in the Fall 2004 shutdown. Other boards (Crate Controller, DFEAs) can follow later.



CTT Upgrade: 'Commission/Install/Commission'

- Try to offload as much as possible from commissioning after installation
- With partial chain and real data from the real frontend:
 - Test system level hardware issues
 - Verify ('certify') that current algorithms produce identical results on new hardware (part of this can be done offline by using I/O capture buffers on DFEBs)
 - Test and optimize (efficiency vs. rate) new singlet algorithms (again, can use capture buffers to get real data for offline tests)
- Populate two full crates, check in test stand
- Install (summer 2005); verify cabling
- If parallel chain tests were done right, there should be no issues left at this point. We either continue running doublet (old) algorithms until everybody (TB, physics groups) is happy with the 'operating point' of the new ones, or switch right away.



CTT Upgrade: Manpower needed

- Hardware (Boston+FNAL), Firmware (Boston) and equations (Kansas) **covered**
- Trigsim needs to be updated (Mike Hildreth, Carsten Hensel)
- AFE 'personality' (output mapping) (Makoto -> AFE II group ?)
- Mixer support (Makoto -> ?)
- dfe_ware (download + FW bookkeeping) (Yurii M. -> Oana) **covered**
- ctt_examine (Mike Cooke) **covered**
- CTT_analyze (offline verification) (Yurii M., Makoto -> ?)
- CTT daily operation: current postdocs have to be (and are) moving on

Some of the infrastructure adaptations are needed for this Fall, and thus will have to be done by current experts, but we need new people to start 'learning the CTT' asap.