

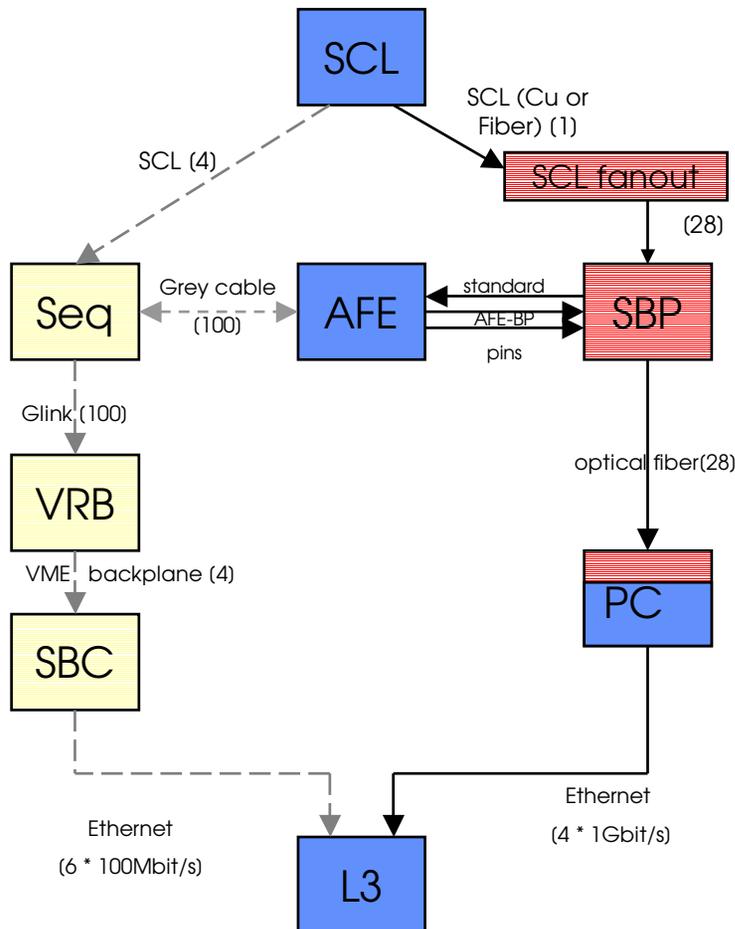


AFE Readout Replacement

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(http://d0server1.fnal.gov/users/stefan/www/AFE_II_readout.pdf/txt)

V3 (Mar. 11, 2005): smart backplane + PCI buffer



Motivation:

Replace all problematic readout components, like grey Sequencer cables (cross talk, unbalanced ground) and Sequencer backplane (many known and probably also many unknown bad connectors).

Basic outline:

AFE II ADC output (1kB/event/board) is read via the standard SVX bus into an FPGA on the new backplane.

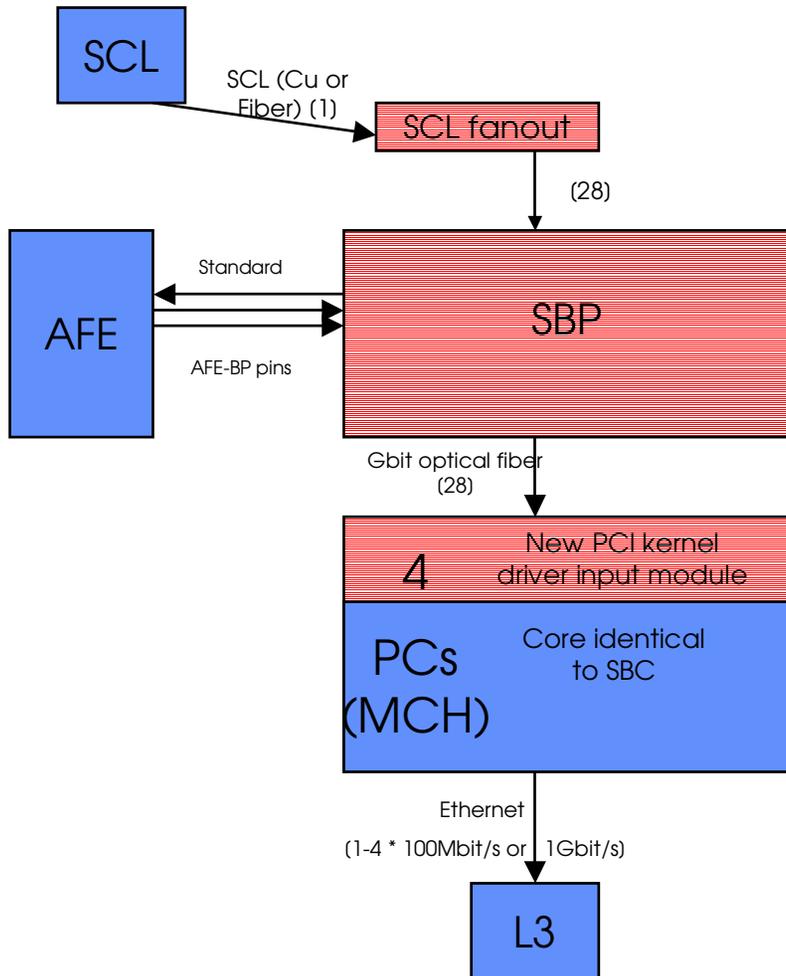
L1 buffering is done in the FPGA. Upon L2 accept data are transferred via optical Gbit link to 4 standard PCs (8 BPs per PC) with one IPM buffer board each.

The PCs run the standard L3 'user code', with a special PCI kernel driver module replacing the VME kernel driver, and feed the L3 system via Gbit ethernet links.

obsolete	exists	new
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smart backplane + PCs



Smart Backplane ('SBP'):

- optical SCL in, one optical Gbit fiber output.
- Buffer depth of 16 events (same as VRB) = $8 * 16 * 1\text{kB} = 128\text{ kByte}$. Easy to have more buffering.
Optional: operate in SDAQ mode; transfer out on each L1 accept
- Output: Gbit optical to 8-input IPM Buffer module

Receiver PCs:

Receives 8 optical Gbit inputs, via 8-input IPM buffer PCI card, and sends one or more ethernet outputs to L3.

Except for the special input driver it runs standard SBC software. (Doug Chapin: replace custom kernel driver module for VME input with new driver;

interface to SBC 'user level' code is 'BIGPHYS' memory array; 'user code' = route manager and L3 interface identical to SBC)

Bandwidth:

- L1 transfer AFE to FPGA exactly the same as now:
 - 1 kB over Byte-wide bus at 53 MHz = 19 microseconds per event
- L2 transfer 1: concentrator to IPM: 8kB at 1 Gbit/s = 70 microseconds
- L2 transfer 2: IPC to PC: $64 * 1\text{kB}$ at 200 MB/s = 0.3 ms
- L2 transfer 3: PC to L3:
 - $64 * 1\text{kB}$ over single Gbit ethernet link = several ms (?)
currently we use 6 (of 8 possible) 100 Mbit ethernet links in parallel (4 readout crates with up to two ethernet links each).



AFE 2 output format

no timing: 16 bit = 9 bit address + 1 bit discriminator + 6 bit ADC

with timing: 22 bit = 9 bit address + 1 bit discriminator + 6 bit TDC + 6 bit ADC

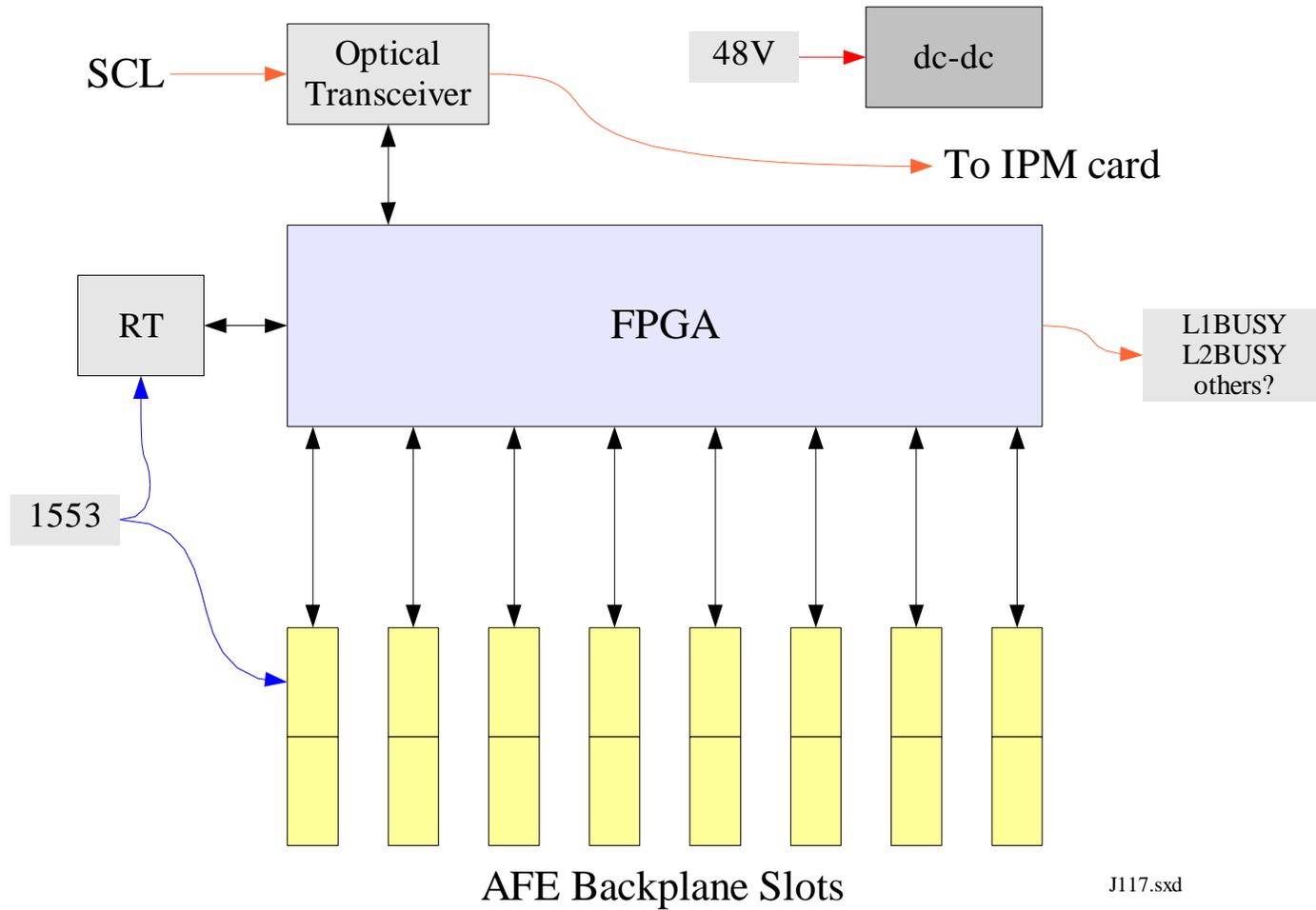
Drop address if running above 50% occupancy.

Data size:

$0.5 * 512 \text{ channels} * 3 \text{ byte} = 0.75 \text{ kB/board/event}$



SBP Block Diagram





SBP Details

- Replaces Sequencers (& grey cables), Sequencer Controller, VRBs, and the VRBC.
- Looks just like sequencers to AFEs
- Same AFE pinout & backwards compatible with existing AFEs
- Possibility of using 48V power distribution
- Communicate with the FPGA via 1553
- Ability to buffer many events in the FPGA
- Sends SCL status signal (busy, etc.) to the TFW



IPM Card

- 8 optical inputs
- PCI 32/64
- Designed by Rick Kwarciany
- Huge buffer memory
- PCI throughput is ~100MBps
- Pre-Production boards working now
- We would need to add a BUSY output to interface with the TFW

