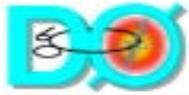


The BROADCASTER and L1 / L2 Trigger

**communication protocols
and
data encoding**

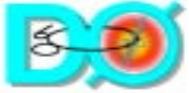
Version 5.0

Manuel I. Martin Feb/09/1999

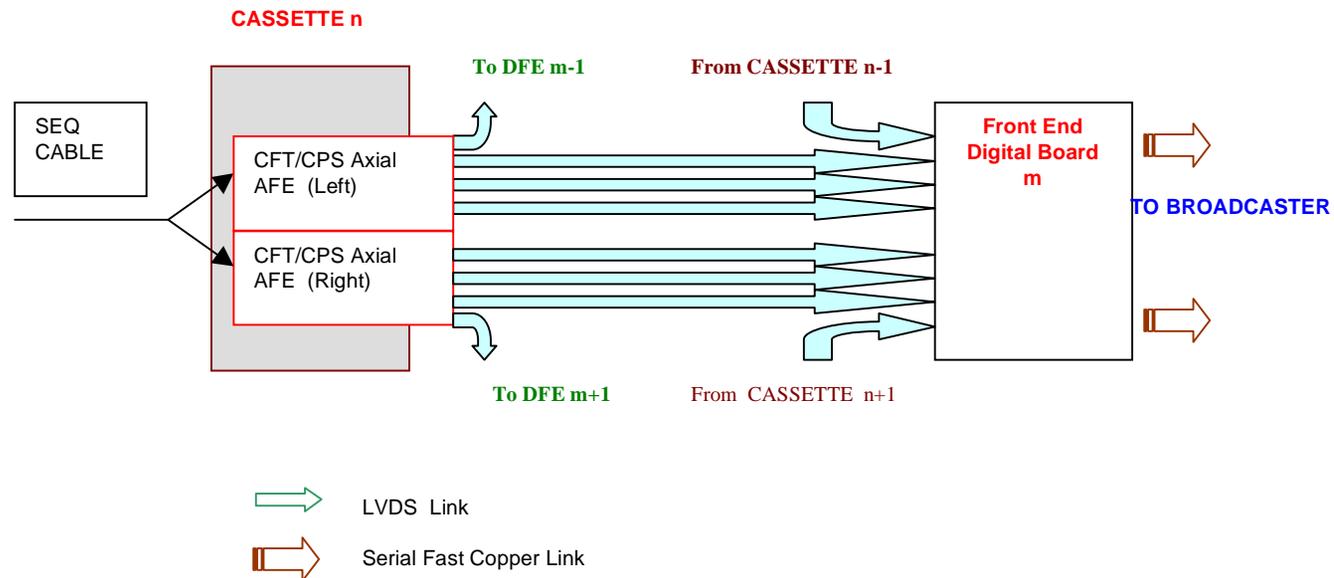


Some Useful Definitions

Track	an object defined by hits in the eight CFT layers such that they fulfill one of the $\cong 16K$ predefined Boolean Equation for trajectories
Isolated Track	a Track that is the only Track in a 13.5° wedge
Cluster	an object formed by one or more consecutive PS strips with #e above a threshold
H PS	a cluster with at least one strip above the High Threshold
L Ps	a cluster with all its elements between a Low and a High Threshold
Loose e	a Track matched to a PS Cluster (H and/or L)
Isolated e	when only one Loose e (H or L) is found in a 13.5° wedge this e is an Isolated e
Loose γ	a H PS cluster with no matched Tracks above a given Pt
Tight γ	if a Loose γ is the only object in found in one 4.5° sector and the adjacent sectors are void the γ is consider a Tight γ
Jet	NOT DEFFINED YET (up to 6 bits available)



Conceptual Block Diagram of the Front End Electronics





Fast Serial Cu Link

- One balance pair Cu line
- Clock embedded in the data
- Transmission Rate at one frame at 53 MHz
- a frame consists of
 - 16 data bits
 - 4 control bits (not all accessible)
- Maximum data Bandwidth 96 bits/crossing
- Error rate $\cong 10^{-13}$
- Big foot area
- needs isolating/balance transformers
- Price per Transmitter /Receiver pair > \$100

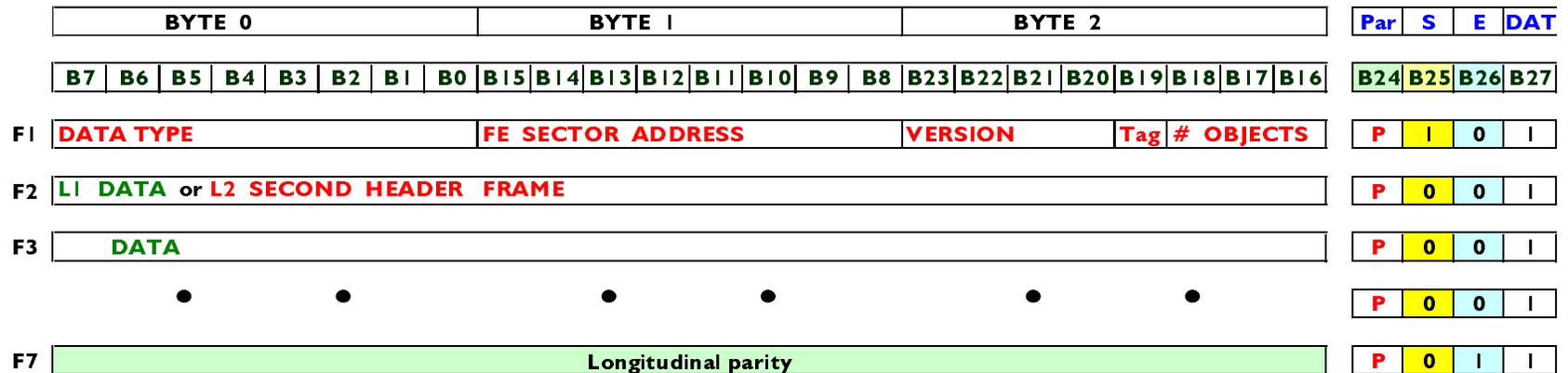
versus

LVDs Link

- Four differential pairs for data
- A separated differential pair for clock
- Transmission Rate at one frame at 53 MHz
- a frame consists of
 - 28 data bits of these we use 4 as control bits (all completely accessible)
- Maximum data Bandwidth 144 bits/crossing
- Error rate $\cong 10^{-12}$ without parity correction much better than 10^{-24} with parity correction
- Very small foot area (surface mounted)
- Price per Transmitter /Receiver pair < \$20



Protocol to Transmit Data via the LVD Link



For L2 Transfers, the Second Frame is part of the Header



A frame is sent every 18.8ns (53MHz) with a transfer rate of 196 bits/crossing

A frame consists of 24 data bits and 4 control bits (user defined)

The usage of Longitudinal and Transversal Parity a permits:

correct any single error in a record

correct any single error in any

column/frame combination

This assures a data transfer practically error free (one in more than 10^{24} bit transfers)



Data Type Code

used by the

Digital Front End Board

- **1 0 x x x x x x** **L1 data**
- **0 1 x x x x x x** **L2 data**
- **x x 1 0 0 0 0 x** **CFT /CPS axial data (only L1)**
- **x x 0 1 0 0 0 x** **CPS axial data**
- **x x 0 0 1 0 0 x** **CPS stereo data**
- **x x 0 0 0 1 0 x** **FPS data**
- **x x 0 0 0 0 1 x** **Forward Proton data**
- **x x x x x x x 1** **Normal Data**
- **x x x x x x x 0** **Debug Data**



System Architecture (no STT)

CFT/CPS Axial:

- Each Broadcaster receives data from 10 Digital Front End boards, serving one full Octant
- Each Broadcaster sends data to one Digital Trigger Card via an LVDs Link
- Each Broadcaster sends data to the L3 via a G Link
- Each Broadcaster sends identical data to the L2CFTpp and the L2CPS using a G Link (passive optical splitter is used)
- One (two) Digital Trigger Card(s) receive data from eight (four) Broadcasters
- The Digital Trigger Cards send data via a Fast Serial Copper Link to a L1CFT/CPS Trigger Manager

CPS Stereo:

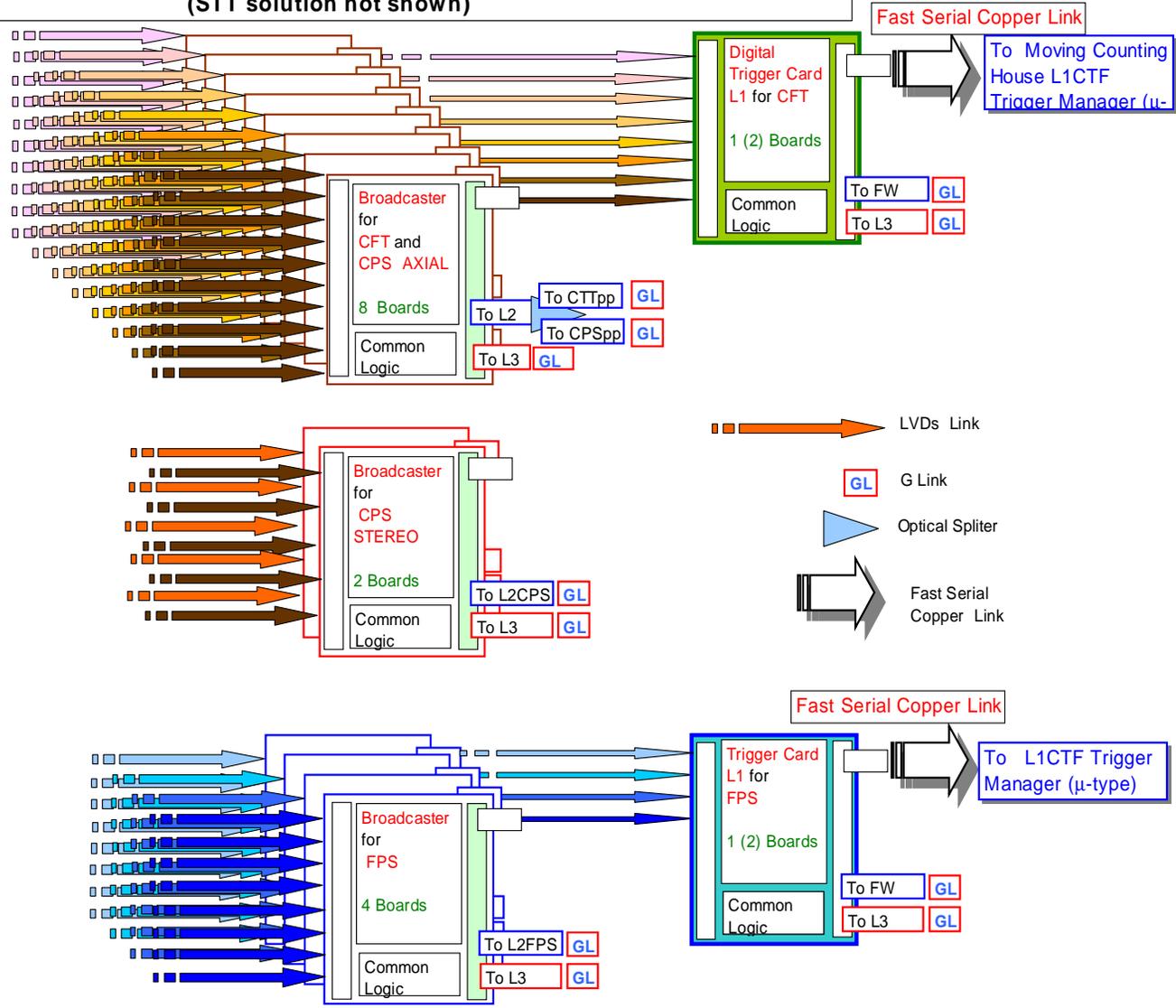
- No L1 Trigger
- Each Broadcaster receives data from 5 Digital Front End boards, serving the North or South
- Each Broadcaster sends data to the L3 via a G Link
- Each Broadcaster sends data to the L2CFTpp

FPS

- Each Broadcaster receives data from 8 Digital Front End boards, serving one full North or South Quadrant
- Each Broadcaster sends data to one Digital Trigger Card via an LVDs Link
- Each Broadcaster sends data to the L3 via a G Link
- Each Broadcaster sends identical data to the L2CFTpp and the L2CPS using a G Link
- One (two) Digital Trigger Card(s) receive data from four (two) Broadcasters
- The Digital Trigger Cards send data via a Fast Serial Copper Link to a L1FPS Trigger Manager



Figure. 17 Broadcaster and L1 Trigger Architecture (STT solution not shown)





Data Transfer from Broadcaster to Digital Trigger Manager (with LVD Link)

	BYTE 0								BYTE 1								BYTE 2								Par	S	E	DAT						
	B7	B6	B5	B4	B3	B2	B1	B0	B15	B14	B13	B12	B11	B10	B9	B8	B23	B22	B21	B20	B19	B18	B17	B16	B24	B25	B26	B27						
F1	#T +Pt 1, No PS				#T- Pt 1, No PS				#T + Pt 1, L PS				#T - Pt 1, L PS				#T + Pt 1, H PS				#T - Pt 1, H PS				P	1	0	1						
F2	#T +Pt 2, No PS				#T- Pt 2, No PS				#T + Pt 2, L PS				#T - Pt 2, L PS				#T + Pt 2, H PS				#T - Pt 2, H PS				P	0	0	1						
F3	#T +Pt 3, No PS				#T- Pt 3, No PS				#T + Pt 3, L PS				#T - Pt 3, L PS				#T + Pt 3, H PS				#T - Pt 3, H PS				P	0	0	1						
F4	#T +Pt 4, No PS				#T- Pt 4, No PS				#T + Pt 4, L PS				#T - Pt 4, L PS				#T + Pt 4, H PS				#T - Pt 4, H PS				P	0	0	1						
F5	V		H		L		S		Pt BIN		V		H		L		S		Pt BIN		V		H		L		S		Pt BIN		P	0	0	1
F6	V		H		L		S		Pt BIN		L. Oc.		# of γ		Φ First Tight γ		Σ Pt		Φ of Jet Axis		Jets ??		P	0	1	1								
F7	Longitudinal parity																												P	0	1	1		

Number of Links

One LVD Link

Total number of bits transferred

196

Total number of data bits transferred

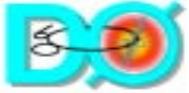
144

Transfer Efficiency

73.5%

Expected error rate

$< 10^{-24}$

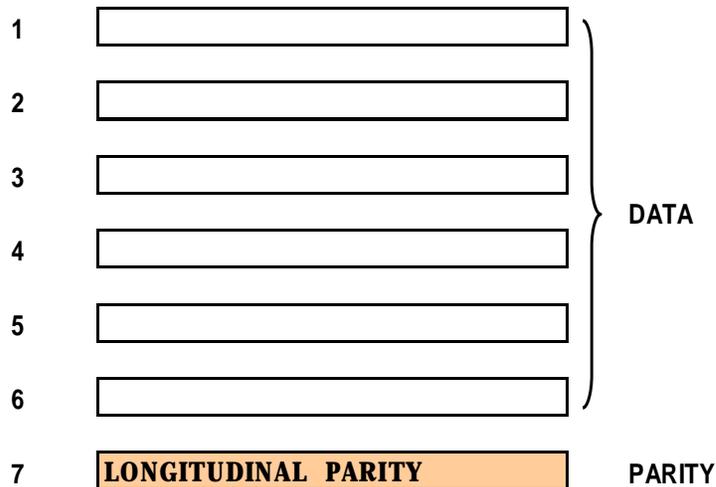


L1

PROTOCOLS for the Fast Cu Serial Link

Digital Trigger Manager to L1CFT/CPS Axial Trigger Manager

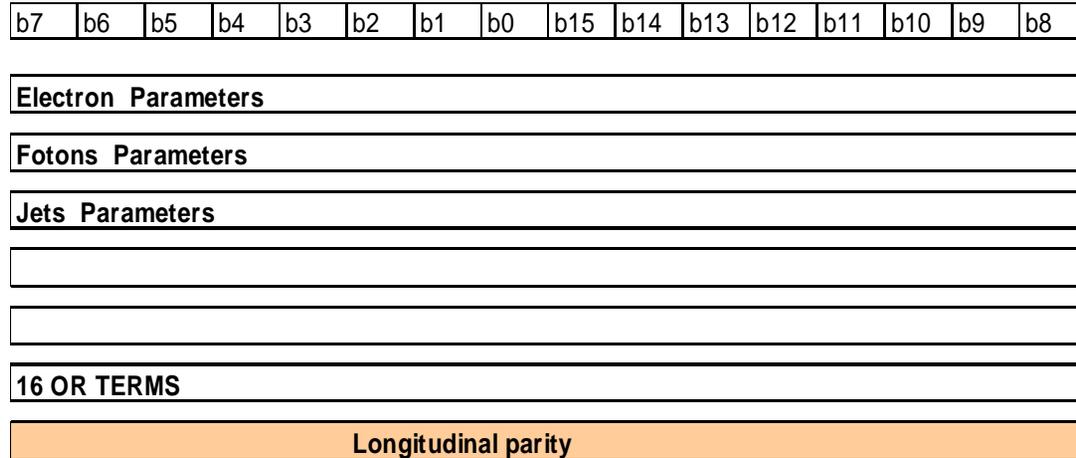
FRAME



- ◆ 96 bits of data per record
- ◆ Longitudinal Parity
- ◆ No Transversal Parity
- ◆ No Sync. Code
- ◆ Fast Serial Copper Link using balance transformed coupled lines



Data Transfer from Digital Trigger Manager to μ -type Trigger Manager



The information generated by the DIGITAL TRIGGER Manager could have more Physics contents that the information provided to it.

The information reaching the LICFT Trigger Manager could include 16 first level AND*OR terms.

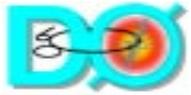
Total Number of bits Transferred	140		
Total Number of Data Bits	96	Efficiency of transfer	58.6%
Expected error rate	$>10^{-13}$		



Data used by the L1FPS Trigger Manager

Number of Matched U and V,
Low and High Threshold Clusters 64 bits for a maximum of 63 clusters
of each type

	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
F1	# of M atch H igh Threshold U Clusters								# of U nmatch H igh Threshold U Clusters							
F2	# of M atch L ow Threshold U Clusters								# of U nmatch L ow Threshold U Clusters							
F3	# of M atch H igh Threshold V Clusters								# of U nmatch H igh Threshold V Clusters							
F4	# of M atch L ow Threshold V Clusters								# of U nmatch L ow Threshold V Clusters							



System Architecture to L2 Central

including a solution for the STT mapping

The Problem

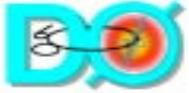
The Silicon Tracker has a six fold symmetry whether the SF tracker has an eight fold symmetry

The Si Sextants boundaries are at 0° , 60° , 120° , 180° , 240° , 300° , 360°

To assure full track coverage each Sextant needs to be mapped into overlapping wedges of the SF Tracker with boundaries defined as follows:

$351^{\circ} > \text{Min},$	$\text{Max} > 69^{\circ}$
$41^{\circ} > \text{Min},$	$\text{Max} > 129^{\circ}$
$111^{\circ} > \text{Min},$	$\text{Max} > 189^{\circ}$
$171^{\circ} > \text{Min},$	$\text{Max} > 249^{\circ}$
$231^{\circ} > \text{Min},$	$\text{Max} > 309^{\circ}$
$291^{\circ} > \text{Min},$	$\text{Max} > 369^{\circ} (9^{\circ})$

The Octants of the SF boundaries are defined for the CFT Trigger at 0° , 45° , 90° , 135° , 180° , 225° , 270° , 315° , 360°



System Architecture to L2 Central

including a solution for the STT mapping

The Solution

Create by electronic means suitable partitions into non overlapping wedges such that they cover the 360° and map each Sextant into three wedges. Each wedge is “created” by one Broadcaster board.

The best partition is as follows:

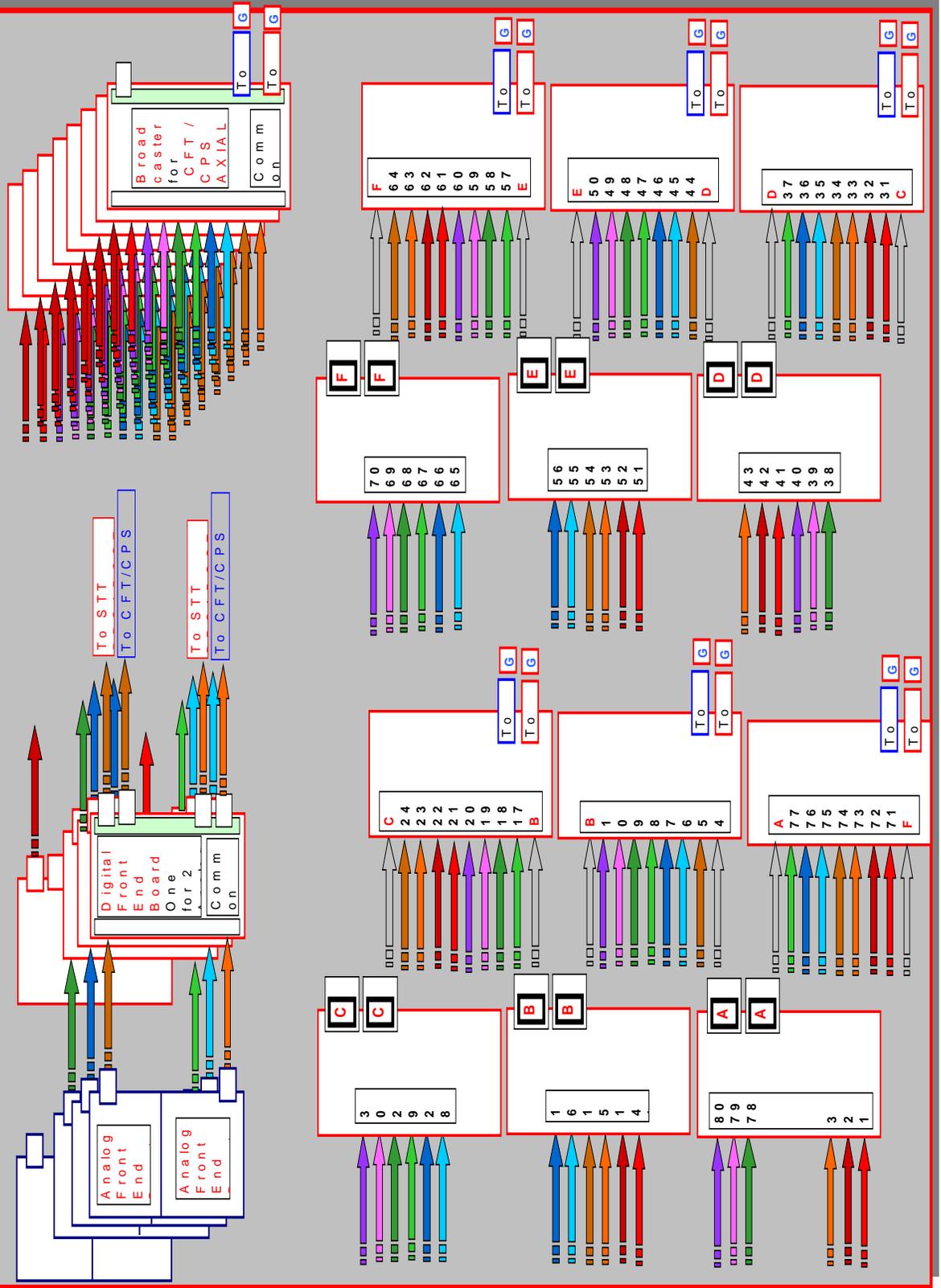
$\{346.5^{\circ}, 13.5^{\circ}\}$, $\{13.5^{\circ}, 45^{\circ}\}$, $\{45^{\circ}, 72^{\circ}\}$, $\{72^{\circ}, 108^{\circ}\}$, $\{108^{\circ}, 135^{\circ}\}$, $\{135^{\circ}, 166.5^{\circ}\}$,
 $\{166.5^{\circ}, 199.5^{\circ}\}$, $\{199.5^{\circ}, 225^{\circ}\}$, $\{225^{\circ}, 252^{\circ}\}$, $\{252^{\circ}, 288^{\circ}\}$, $\{288^{\circ}, 315^{\circ}\}$, $\{315^{\circ}, 346.5^{\circ}\}$,

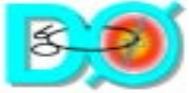
The mapping of Sextants into wedges is as follows:

Sextant	$\{0^{\circ}, 60^{\circ}\}$	⇒	$\{346.5^{\circ}, 13.5^{\circ}\}$, $\{13.5^{\circ}, 45^{\circ}\}$, $\{45^{\circ}, 72^{\circ}\}$
Sextant	$\{60^{\circ}, 120^{\circ}\}$	⇒	$\{45^{\circ}, 72^{\circ}\}$, $\{72^{\circ}, 108^{\circ}\}$, $\{108^{\circ}, 135^{\circ}\}$
Sextant	$\{120^{\circ}, 180^{\circ}\}$	⇒	$\{108^{\circ}, 135^{\circ}\}$, $\{135^{\circ}, 166.5^{\circ}\}$, $\{166.5^{\circ}, 199.5^{\circ}\}$
Sextant	$\{180^{\circ}, 240^{\circ}\}$	⇒	$\{166.5^{\circ}, 199.5^{\circ}\}$, $\{199.5^{\circ}, 225^{\circ}\}$, $\{225^{\circ}, 252^{\circ}\}$
Sextant	$\{240^{\circ}, 300^{\circ}\}$	⇒	$\{225^{\circ}, 252^{\circ}\}$, $\{252^{\circ}, 288^{\circ}\}$, $\{288^{\circ}, 315^{\circ}\}$
Sextant	$\{300^{\circ}, 360^{\circ}\}$	⇒	$\{288^{\circ}, 315^{\circ}\}$, $\{315^{\circ}, 346.5^{\circ}\}$, $\{346.5^{\circ}, 13.5^{\circ}\}$

This is shown in the next picture

Figure. 18 Digital Front End, Broadcaster and L2 Trigger Architecture





Notes about the STT L2 Architecture

The solution presented is the most flexible and the one which requires minimum hardware.

Although the block diagram shows two G Links from the six Broadcaster boards going to the L2STT in reality only one is needed.

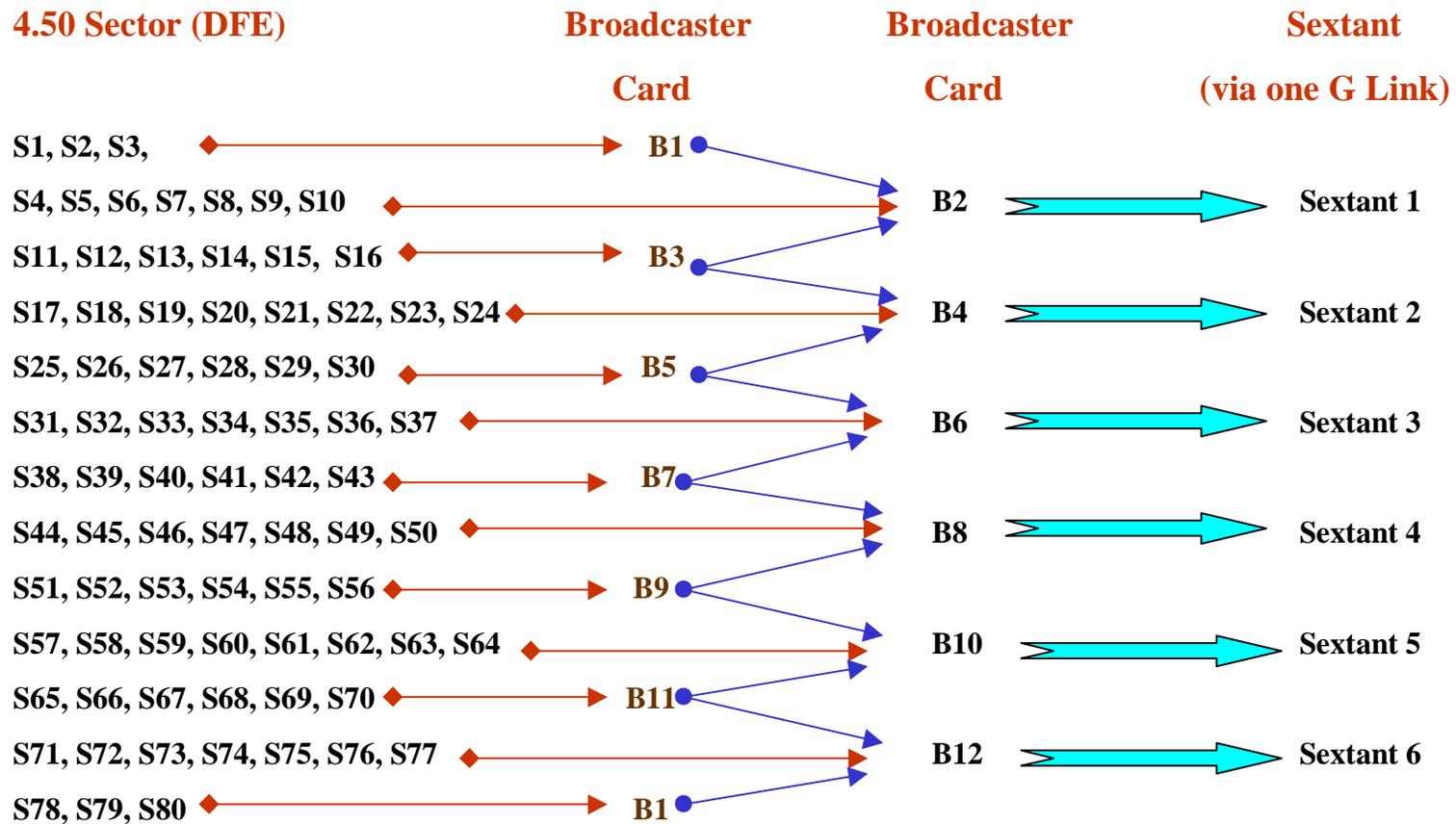
Each G Link serves a single Sextant of the STT minimizing the hardware/software requirements for the L2STTpp

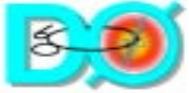
12 Broadcaster cards are required to do the proper mapping of the 80 4.50 sectors into the “expanded” sextants of the Si tracker. Of these only six required G Link outputs.



Notes about the STT L2 Architecture

Naming of the 4.5° sectors is as follows: S1 covers 0° to 4.5° , S80 covers 355.5° to 360° . The mapping these sectors into the Broadcaster cards and Si sextants is shown in the following table:





Protocol for BROADCASTER to L2pp (FIC) Transfers

F#	LW#	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D09	D08
1	1	Number of Objects								Header Length (3)							
2		Object Length (1 or 2)								Hd. Format				Obj. Format			
3	2	Source ID								Bunch Number							
4		Rotation Number															
5	3	Algorithm Major Version								Algorithm Minor Version							
6		Processing ID								Global ERROR Code							
2N-1	N	Bunch Number								Source ID							
2N	N	Longitudinal Parity								Longitudinal Parity							

HEADER

TRAILER

Compromise to have common protocol with other systems



Data used by the L2CFTpp

Number of Tracks per Pt bin	4*8 bits	for a maximum of 46 tracks
List of tracks with tagging and address	n*32 bits	for a maximum of 46 tracks

F #	LW#	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
5	3	# of Tracks in Pt bin 1								# of Tracks in Pt bin 2							
6	3	# of Tracks in Pt bin 3								# of Tracks in Pt bin 4							
7	4	ERROR CODE			HPS	LPS	ISO	eISO	S	Pt BIN		EXTENDED Pt VALUE					
8	4	FE BOARD # (address)									Φ ADDRESS						





Data used by the L2CPSpp (AXIAL)

List of clusters with tagging, width, address and Pt information n*32 bits for a maximum of 47 clusters of track associated

F #	LW#	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
5	3	ERROR CODE				PSH	PSL		T	S	Pt BIN		CLUSTER WIDTH				
6	3	FE BOARD ADDRESS							N/S	CLUSTER ADDRESS							



Data used by the L2CPSpp (STEREO)

List of clusters with tagging,
width and address

n*32 bits for a maximum of 47 clusters

F #	W #	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
7	4	ERROR CODE				PSH	PSL							CLUSTER WIDTH			
8	4	FE BOARD ADDRESS							U/V	CLUSTER ADDRESS							





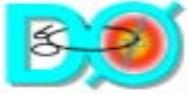
Data used by the L2FPSpp

List of clusters with tagging,
width, address and mip bit
pattern

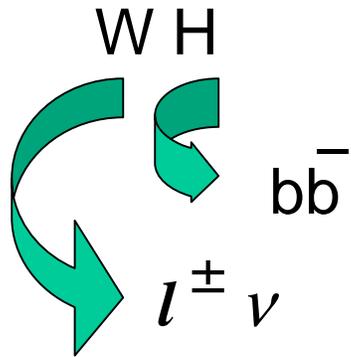
n*34 bits for a maximum of 23 clusters

F #	LW #	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	
7	4	ERROR CODE			PSH	PSL				CLSTR WIDTH								
8	4	FE BOARD ADDRESS						U/V	N/S	CLSTR ADDRESS								
9	5	MIP BIT PATTERN																
10	5																	

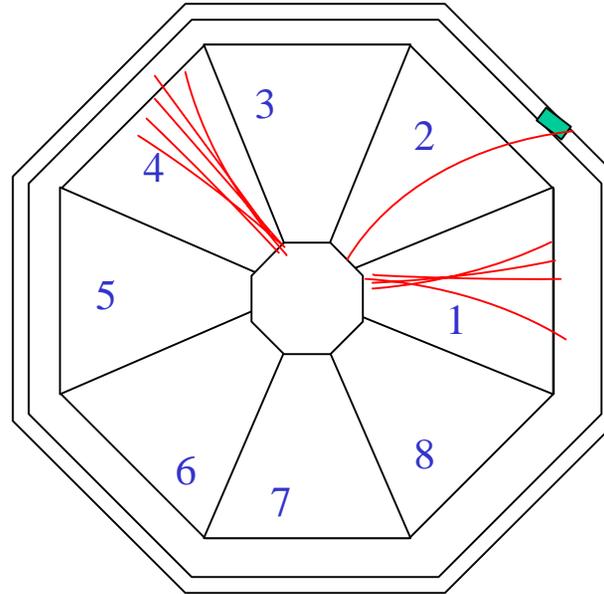


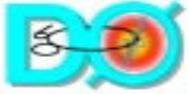


Some Examples of L1CTT Triggers

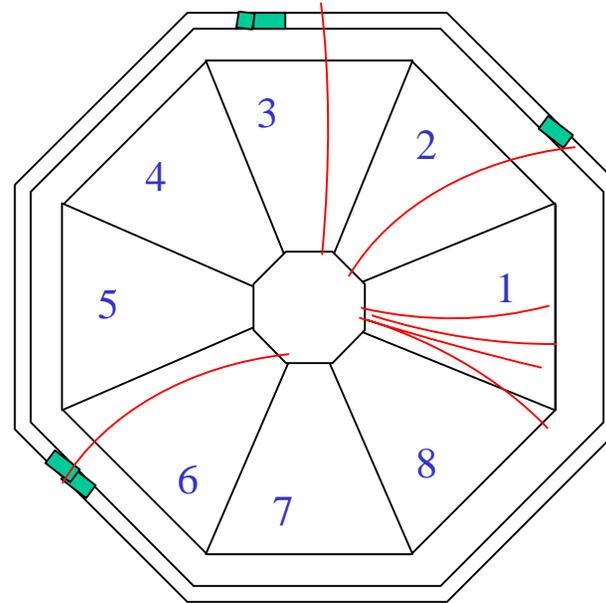
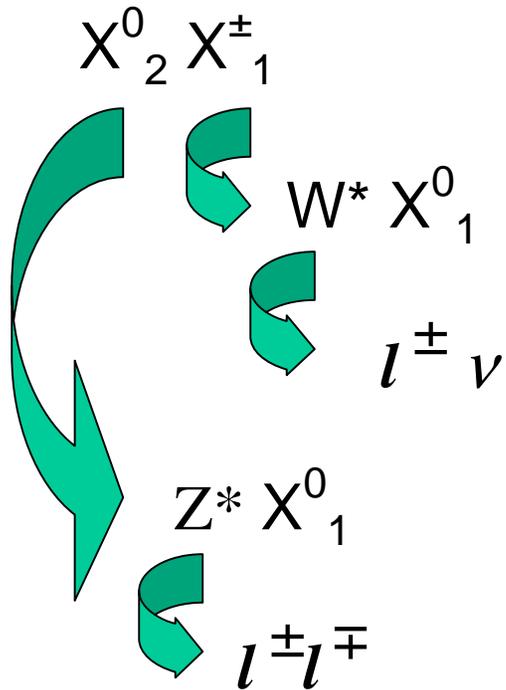


e $P_t > 10$





Some Examples of L1CTT Triggers



τ $P_t > 10$
 e $P_t > 5$
 e $P_t > 3$

