

SF Trigger Progress Report

April, 2, 1998



➤ Reached agreement with the μ Trigger (L1) group to anchor the track-finding algorithm on the A layer. This eliminates a very difficult problem created by the need of anchoring the tracks in A layer for the SVT (L2) and in the H layer for the μ L1 Trigger!



➤ Waiting closure in regard to the proposal to use the FIC, SLIC and MBTC to build the SVTpp and CFTpp. This issue is delaying the progress of the Broadcaster design and the TDR

SF Trigger Progress Report

April, 2, 1998

Hardware

➤ **Trigger Test Board**

Successful download of VHDL programs
into FPLDs

Layout of Data Distribution mezzanine continues

➤ **MCM (Multiple Chip Module) Test Board is designed and layout completed. Ready for PCB manufacturing. (8 layers and includes a version of the MCM).**

➤ **25 new SIFT chips arrived Tuesday.**

➤ **VRB Controller design is being modified to accommodate CFT requirements (add clock and triggers path directly to FE Boards).**