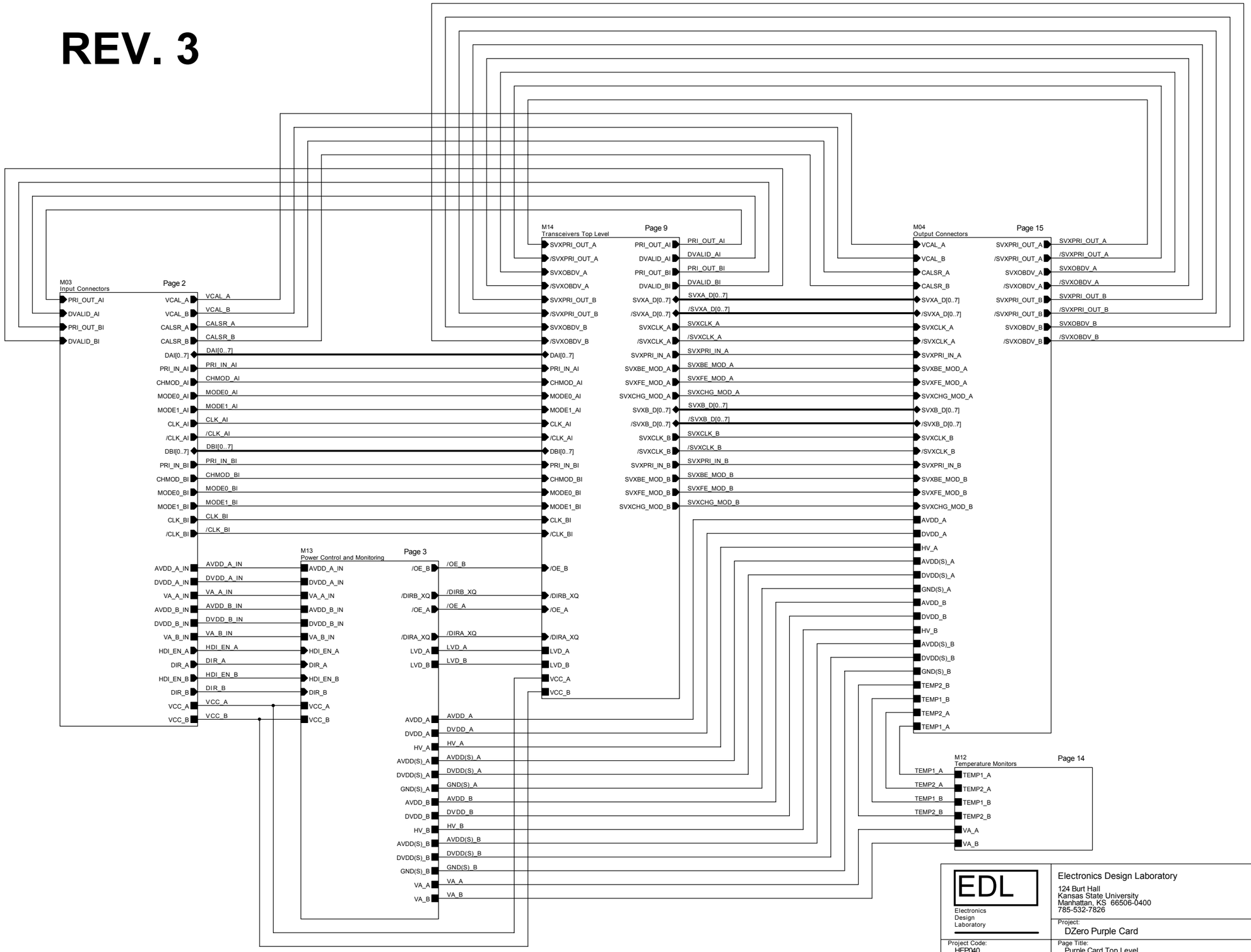
REV. 3



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785-532-7826

Project: DZero Purple Card

Project Code: HEP040

Page Title: Purple Card Top Level

Approvals:

Rev. 3.0

Page Date: Friday, January 24, 2003

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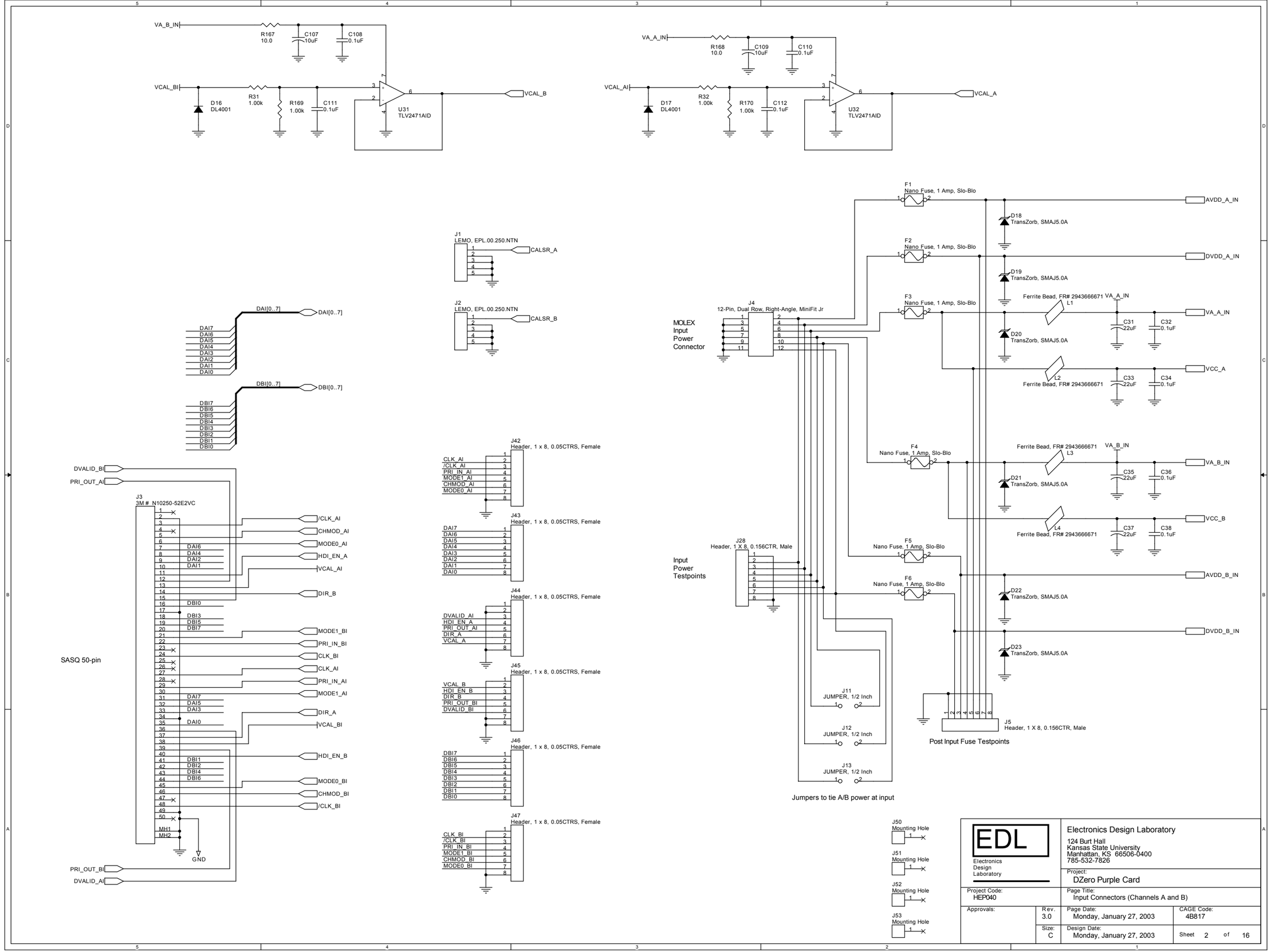
Design Date: Friday, January 24, 2003

Sheet 1 of 16


VA_B_IN
R167 10.0
C107 10uF
C108 0.1uF
VCAL_BI
D16 DL4001
R31 1.00k
R169 1.00k
C111 0.1uF
U31 TLV2471AID
VCAL_B
VA_A_IN
R168 10.0
C109 10uF
C110 0.1uF
VCAL_AI
D17 DL4001
R32 1.00k
R170 1.00k
C112 0.1uF
U32 TLV2471AID
VCAL_A
J1 LEMO, EPL.00.250.NTN
CALSR_A
J2 LEMO, EPL.00.250.NTN
CALSR_B
DAI[0..7]
DAI7 DAI6 DAI5 DAI4 DAI3 DAI2 DAI1 DAI0
DBI[0..7]
DBI7 DBI6 DBI5 DBI4 DBI3 DBI2 DBI1 DBI0
DVALID_BI
PRI_OUT_AI
J3 3M # N10250-52E2VC
SASQ 50-pin
/CLK_AI
CHMOD_AI
MODE0_AI
HDI_EN_A
VCAL_AI
DIR_B
MODE1_BI
PRI_IN_BI
CLK_BI
CLK_AI
PRI_IN_AI
MODE1_AI
DIR_A
VCAL_BI
HDI_EN_B
MODE0_BI
CHMOD_BI
/CLK_BI
MH1
MH2
GND
PRI_OUT_BI
DVALID_AI
J42 Header, 1 x 8, 0.05CTRS, Female
CLK_AI /CLK_AI PRI_IN_AI MODE1_AI CHMOD_AI MODE0_AI
J43 Header, 1 x 8, 0.05CTRS, Female
DAI7 DAI6 DAI5 DAI4 DAI3 DAI2 DAI1 DAI0
J44 Header, 1 x 8, 0.05CTRS, Female
DVALID_AI HDI_EN_A PRI_OUT_AI DIR_A VCAL_A
J45 Header, 1 x 8, 0.05CTRS, Female
VCAL_B HDI_EN_B DIR_B PRI_OUT_BI DVALID_BI
J46 Header, 1 x 8, 0.05CTRS, Female
DBI7 DBI6 DBI5 DBI4 DBI3 DBI2 DBI1 DBI0
J47 Header, 1 x 8, 0.05CTRS, Female
CLK_BI /CLK_BI PRI_IN_BI MODE1_BI CHMOD_BI MODE0_BI
F1 Nano Fuse, 1 Amp, Slo-Blo
F2 Nano Fuse, 1 Amp, Slo-Blo
F3 Nano Fuse, 1 Amp, Slo-Blo
F4 Nano Fuse, 1 Amp, Slo-Blo
F5 Nano Fuse, 1 Amp, Slo-Blo
F6 Nano Fuse, 1 Amp, Slo-Blo
D18 TransZorb, SMAJ5.0A
D19 TransZorb, SMAJ5.0A
D20 TransZorb, SMAJ5.0A
D21 TransZorb, SMAJ5.0A
D22 TransZorb, SMAJ5.0A
D23 TransZorb, SMAJ5.0A
AVDD_A_IN
DVDD_A_IN
VA_A_IN
VCC_A
VA_B_IN
VCC_B
AVDD_B_IN
DVDD_B_IN
Ferrite Bead, FR# 2943666671
L1 L2 L3 L4
C31 22uF
C32 0.1uF
C33 22uF
C34 0.1uF
C35 22uF
C36 0.1uF
C37 22uF
C38 0.1uF
J4 12-Pin, Dual Row, Right-Angle, MiniFit Jr
MOLEX Input Power Connector
J28 Header, 1 X 8, 0.156CTR, Male
Input Power Testpoints
J5 Header, 1 X 8, 0.156CTR, Male
Post Input Fuse Testpoints
J11 JUMPER, 1/2 Inch
J12 JUMPER, 1/2 Inch
J13 JUMPER, 1/2 Inch
Jumpers to tie A/B power at input
J50 Mounting Hole
J51 Mounting Hole
J52 Mounting Hole
J53 Mounting Hole
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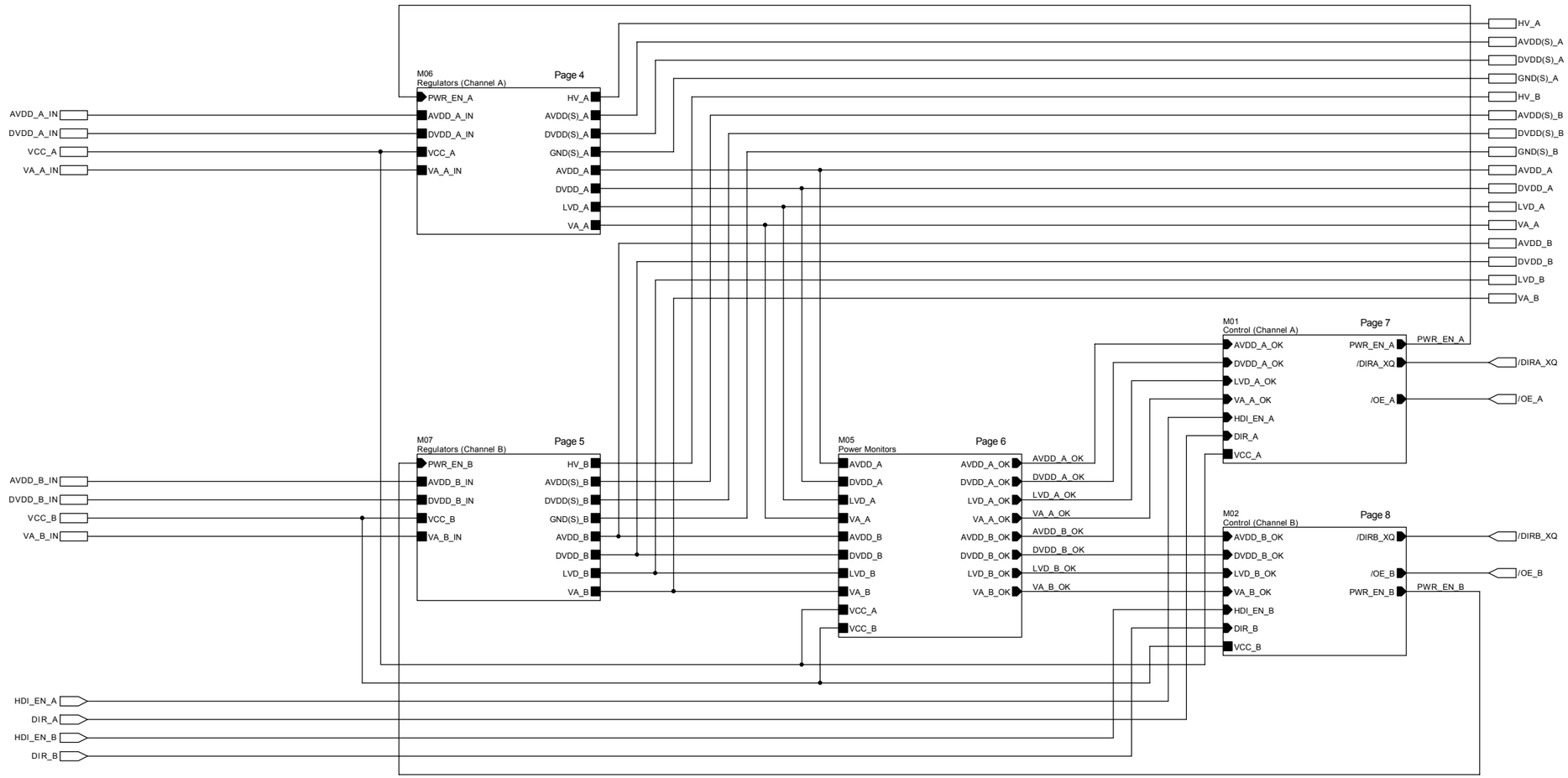
785-532-7826
Project: DZero Purple Card
Project Code: HEP040
Page Title: Input Connectors (Channels A and B)
Approvals:
Rev. 3.0
Page Date: Monday, January 27, 2003
CAGE Code: 4B817
Size: C
Design Date: Monday, January 27, 2003
Sheet 2 of 16



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785-532-7826

Project: DZero Purple Card

Project Code: HEP040

Page Title: Power, Control, and Monitoring Top Level

Approvals:

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CAUTION: Heatsinks are at requlator ourpur voltage. Use caution not to short outputs when handling the board.

J23
Header, 2 x 5, 0.1CTRS, Male
Post Regulator Fuse Testpoints

Use Aavid-Thermalloy Heatsink # 7106D with U18.

AVDD_A_IN
VA_A
U18
Vcontrol
Vout_Tab
Vout
Vsense
Vpower
Adjust
CS5253B-1
R56 243
D6A MV6LED
C56 10uF
C57 100uF
R58 56.2
R178 100 Ohm, Sngl Turn
Bourns 3224W
R57 124
F10 Nano Fuse, 1 Amp, Slo-Blo
C55 33uF
R177 100K
C54 0.1uF
GND(S)_A
AVDD_A
AVDD(S)_A
GND(S)_A

J49 is used when single regulator operation is needed.

J49
Header, 2 x 2, 0.1CTRS, Male

As configured, minimum Vpower input voltage (AVDD_IN and DVDD_IN) is 3.1 V.

Use Aavid-Thermalloy Heatsink # 7106D with U19.

DVDD_A_IN
VA_A
U19
Vcontrol
Vout_Tab
Vout
Vsense
Vpower
Adjust
CS5253B-1
R61 243
D6B MV6LED
C60 10uF
C61 100uF
R63 56.2
R180 100 Ohm, Sngl Turn
Bourns 3224W
R62 124
F11 Nano Fuse, 1 Amp, Slo-Blo
C59 33uF
R179 100K
C58 0.1uF
GND(S)_A
DVDD_A
DVDD(S)_A

U17
VCC
C62 0.1uF
U17D 74HCT14D
U17C 74HCT14D
U17E 74HCT14D
U17B 74HCT14D

Use Aavid-Thermalloy Heatsink # 7106D with U20.

VCC is isolated on this page

VCC_A
VCC
VA_A
U20
Vcontrol
Vout_Tab
Vout
Vsense
Vpower
Adjust
CS5253B-1
R66 357
D7A MV6LED
C64 10uF
C67 100uF
R69 205
R67 124
F12 Nano Fuse, 1 Amp, Slo-Blo
C65 33uF
R181 100K
C63 0.1uF
LVD_A

PWR_EN_A
U17F 74HCT14D
VCC
R71 681
LS10 PVN012
R98 357
D7B MV6LED
VA_A_IN
VA_A
R182 100K
C68 0.1uF
VA_A

Short pins 1 and 2 of jumpers J25 and J26 for operation to 300V. For 1kV operation, open J25 and J26 and tie J25 pin 1 to J26 pin 2 with HV wire

Isolated SHV Connector

J24
SHV, Panel Mount
J24 Guard
R138 0
J25
JUMPER, 0.3 Inch
J26
JUMPER, 0.6 Inch
HV_A
C66 0.1uF, 500V
LS9 PVU414S
VCC
R70 681
U17A 74HCT14D

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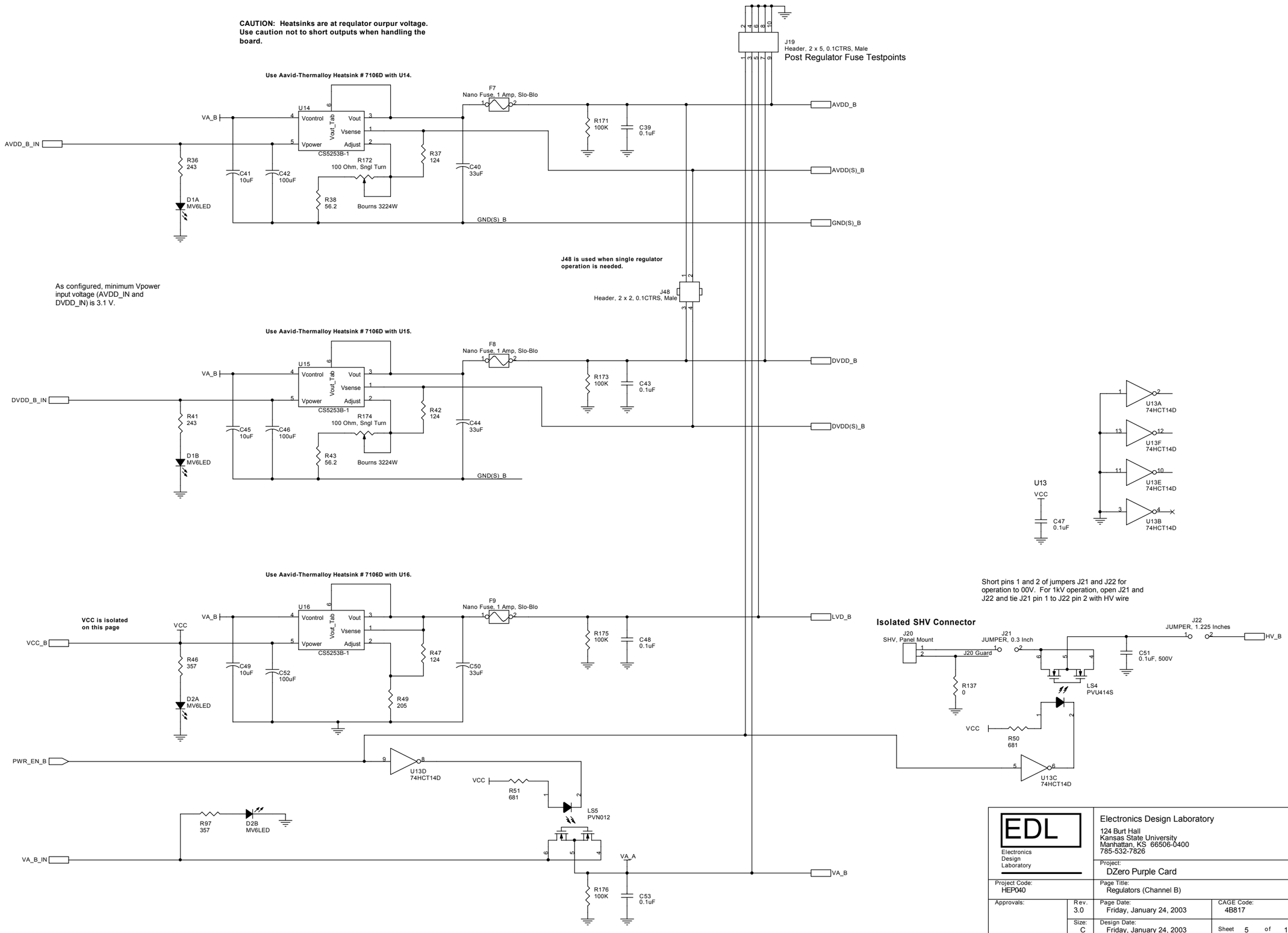
	Project: DZero Purple Card		
Project Code: HEP040	Page Title: Regulators (Channel A)		
Approvals:	Rev. 3.0	Page Date: Friday, January 24, 2003	CAGE Code: 4B817
	Size: C	Design Date: Friday, January 24, 2003	Sheet 4 of 16


CAUTION: Heatsinks are at requlator ourpur voltage. Use caution not to short outputs when handling the board.
J19
Header, 2 x 5, 0.1CTRS, Male
Post Regulator Fuse Testpoints
Use Aavid-Thermalloy Heatsink # 7106D with U14.
U14
Vcontrol
Vout_Tab
Vout
Vsense
Vpower
Adjust
CS5253B-1
VA_B
AVDD_B_IN
R36
243
D1A
MV6LED
C41
10uF
C42
100uF
R172
100 Ohm, Sngl Turn
R38
56.2
Bourns 3224W
R37
124
C40
33uF
F7
Nano Fuse, 1 Amp, Slo-Blo
R171
100K
C39
0.1uF
AVDD_B
AVDD(S)_B
GND(S)_B
J48 is used when single regulator operation is needed.
J48
Header, 2 x 2, 0.1CTRS, Male
As configured, minimum Vpower input voltage (AVDD_IN and DVDD_IN) is 3.1 V.
Use Aavid-Thermalloy Heatsink # 7106D with U15.
U15
DVDD_B_IN
R41
243
D1B
MV6LED
C45
10uF
C46
100uF
R174
100 Ohm, Sngl Turn
R43
56.2
Bourns 3224W
R42
124
C44
33uF
F8
Nano Fuse, 1 Amp, Slo-Blo
R173
100K
C43
0.1uF
DVDD_B
DVDD(S)_B
U13
VCC
C47
0.1uF
U13A
74HCT14D
U13F
74HCT14D
U13E
74HCT14D
U13B
74HCT14D
Use Aavid-Thermalloy Heatsink # 7106D with U16.
VCC is isolated on this page
U16
VCC_B
R46
357
D2A
MV6LED
C49
10uF
C52
100uF
R47
124
R49
205
C50
33uF
F9
Nano Fuse, 1 Amp, Slo-Blo
R175
100K
C48
0.1uF
LVD_B
Short pins 1 and 2 of jumpers J21 and J22 for operation to 00V. For 1kV operation, open J21 and J22 and tie J21 pin 1 to J22 pin 2 with HV wire
Isolated SHV Connector
J20
SHV, Panel Mount
J20 Guard
J21
JUMPER, 0.3 Inch
J22
JUMPER, 1.225 Inches
HV_B
C51
0.1uF, 500V
R137
0
LS4
PVU414S
R50
681
U13C
74HCT14D
PWR_EN_B
U13D
74HCT14D
R51
681
LS5
PVN012
R97
357
D2B
MV6LED
VA_B_IN
VA_A
R176
100K
C53
0.1uF
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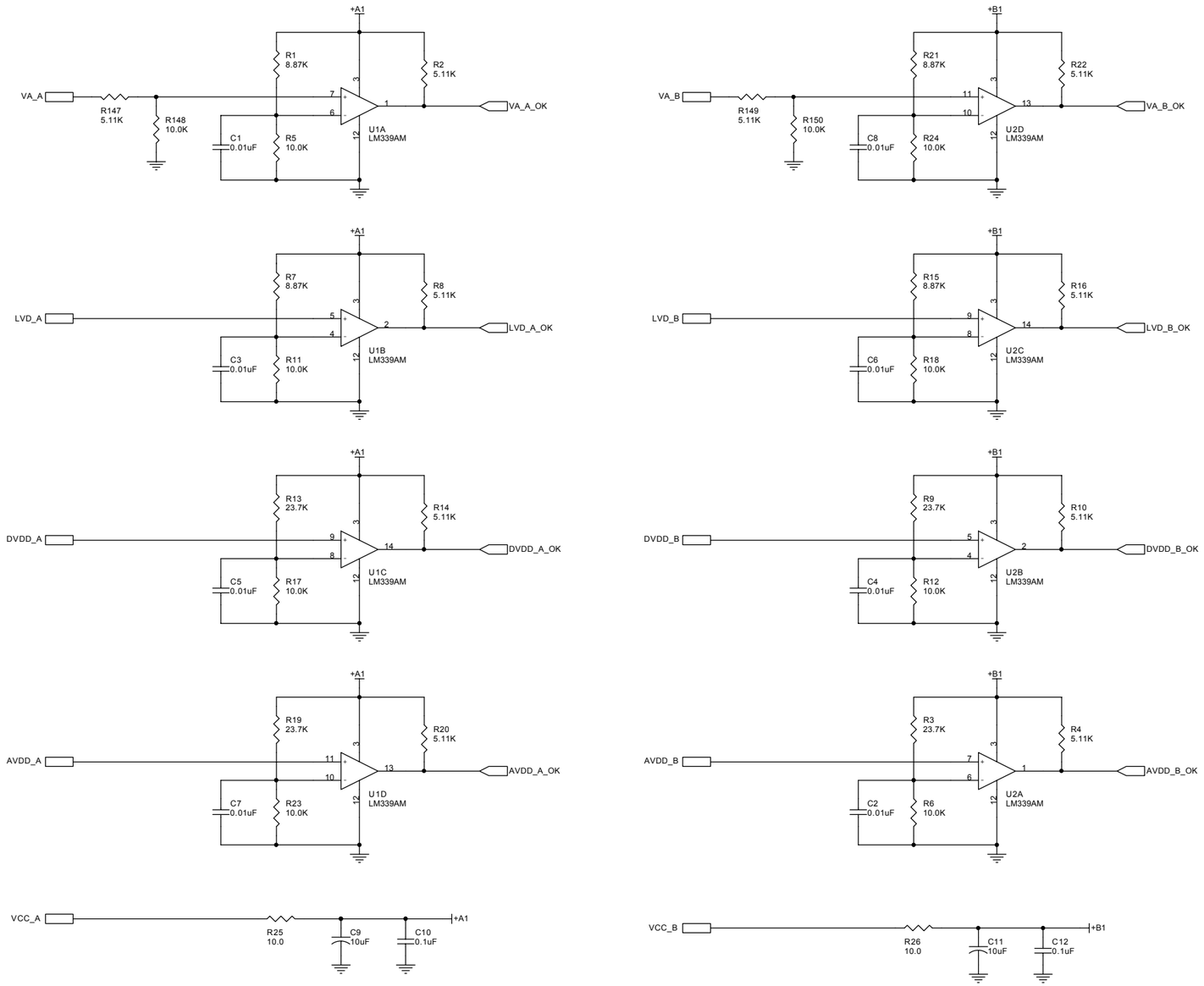
Project:
DZero Purple Card
Project Code:
HEP040
Page Title:
Regulators (Channel B)
Approvals:
Rev.
3.0
Page Date:
Friday, January 24, 2003
CAGE Code:
4B817
Size:
C
Design Date:
Friday, January 24, 2003
Sheet 5 of 16



Circuits only check for nominal voltage 80% of desired

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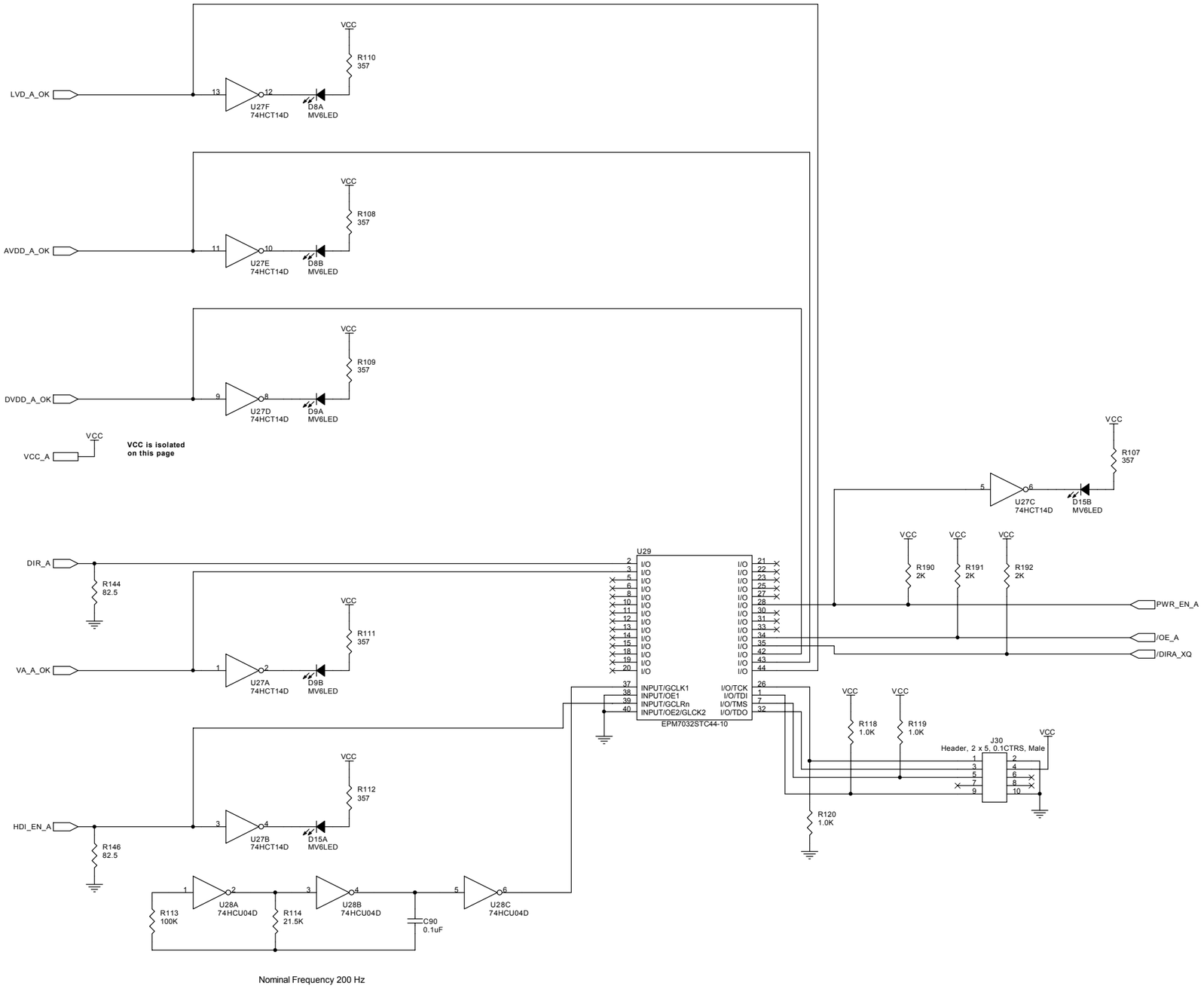
	Project: DZero Purple Card		
Project Code: HEP040	Page Title: Power Monitors (Channels A and B)		
Approvals:	Rev. 3.0	Page Date: Friday, January 24, 2003	CAGE Code: 4B817
	Size: C	Design Date: Friday, January 24, 2003	Sheet 6 of 16



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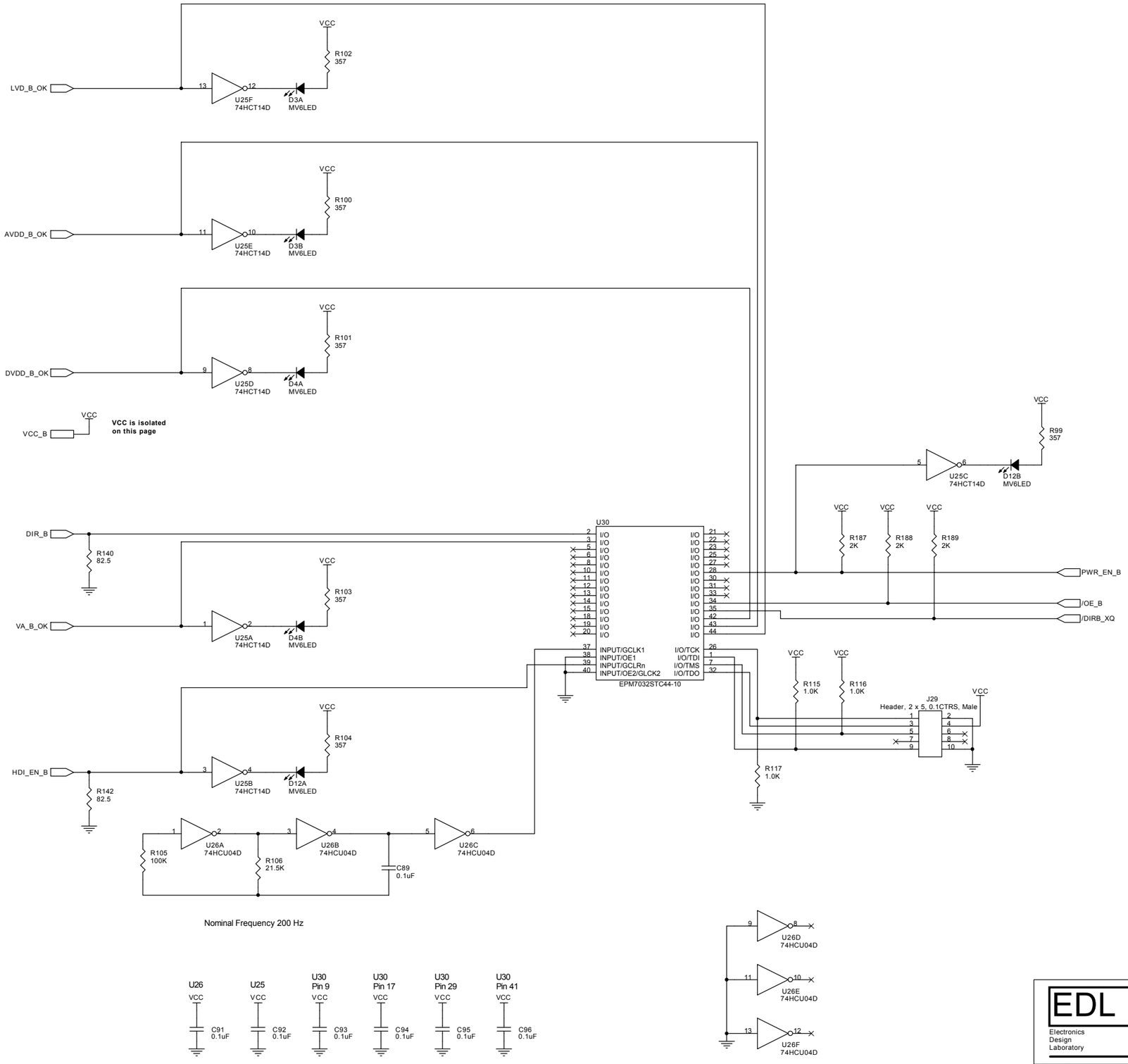
	Project: DZero Purple Card		
Project Code: HEP040	Page Title: Control (Channel A)		
Approvals:	Rev. 3.0	Page Date: Friday, January 24, 2003	CAGE Code: 4B817
	Size: C	Design Date: Friday, January 24, 2003	Sheet 7 of 16



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Project: DZero Purple Card

Project Code: HEP040

Page Title: Control (Channel B)

Approvals:

Rev. 3.0

Page Date: Friday, January 24, 2003

CAGE Code: 4B817

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Design Date: Friday, January 24, 2003

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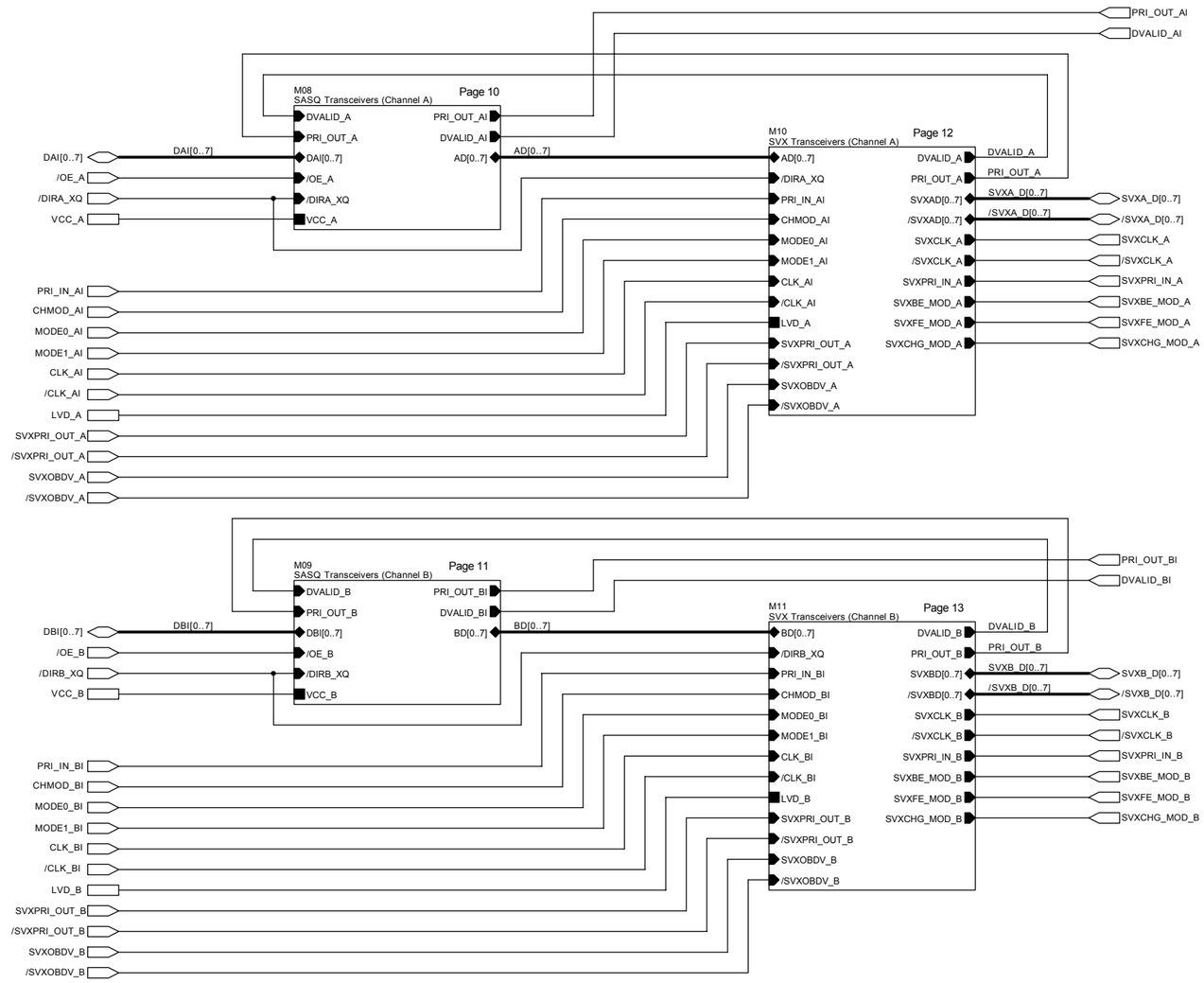

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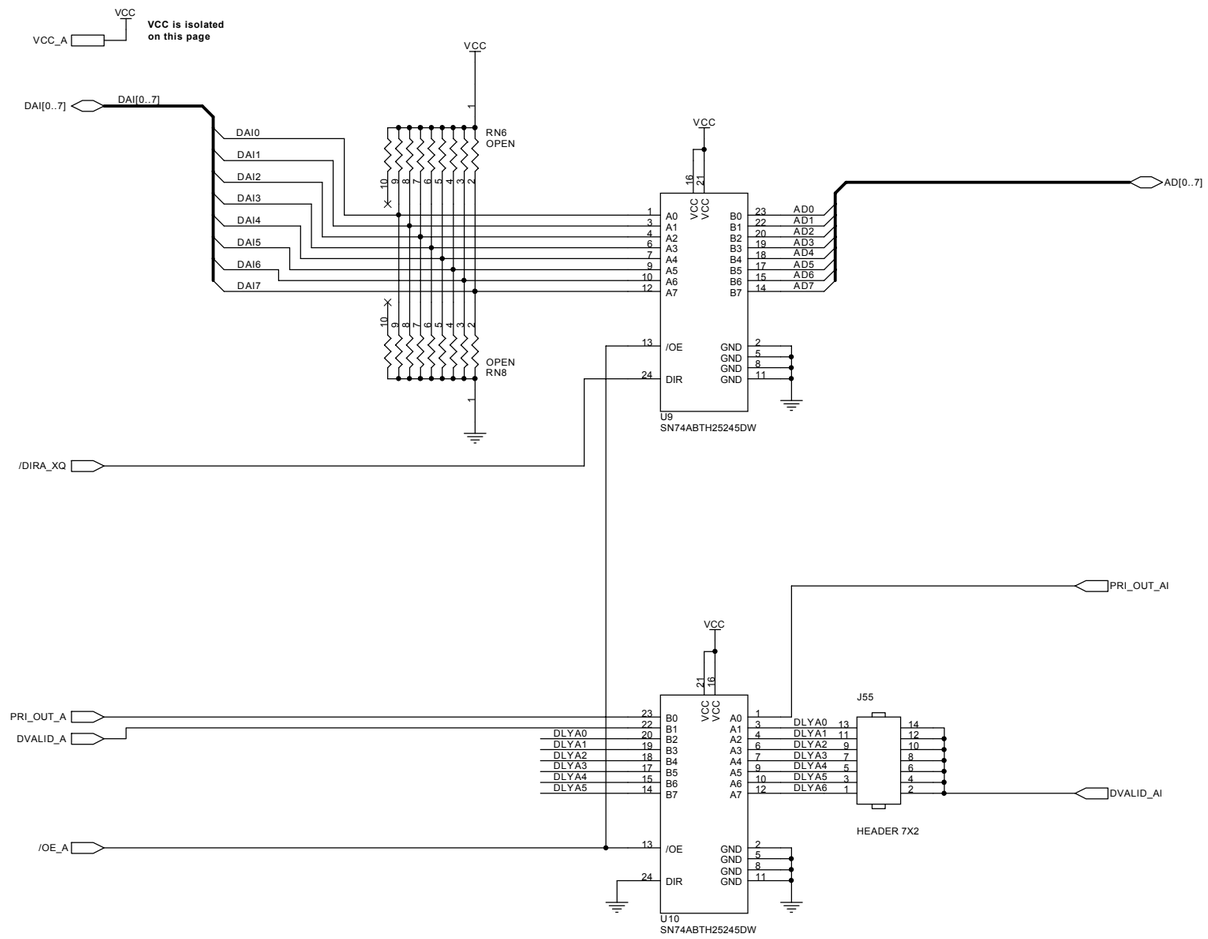
	Project: DZero Purple Card		
Project Code: HEP040	Page Title: Transceivers Top Level		
Approvals:	Rev. 3.0	Page Date: Friday, January 24, 2003	CAGE Code: 4B817
	Size: C	Design Date: Friday, January 24, 2003	Sheet 9 of 16



U10 Pin 16	U9 Pin 21	U10 Pin 21	U9 Pin 16
VCC	VCC	VCC	VCC
C29 0.1uF	C30 0.1uF	C105 0.1uF	C106 0.1uF

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Project: DZero Purple Card

Project Code: HEP040

Page Title: SASQ Transceivers (Channel A)

Approvals:

Rev. 3.0

Page Date: Friday, January 24, 2003

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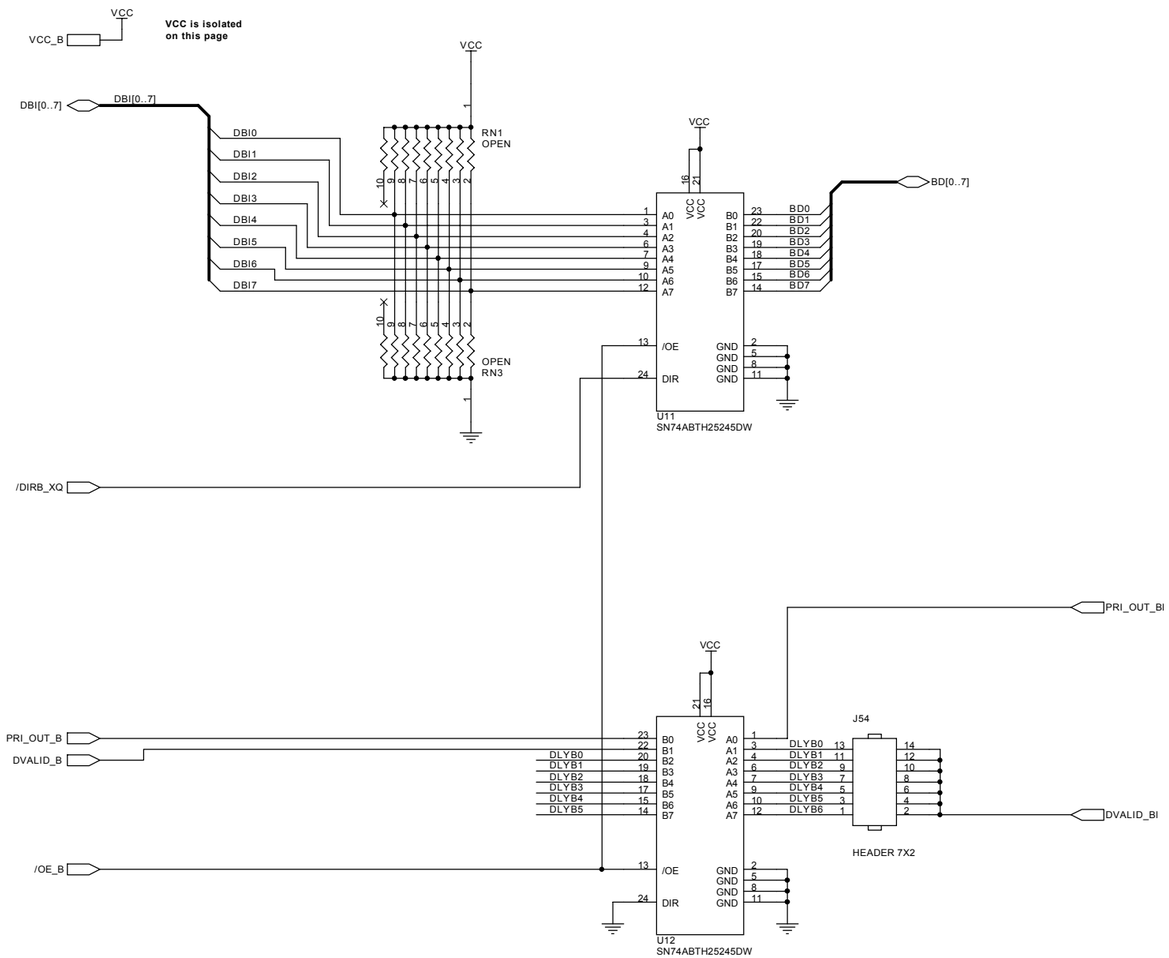
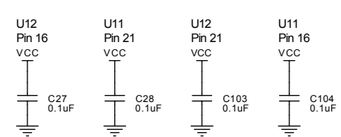
Size: C

Design Date: Friday, January 24, 2003





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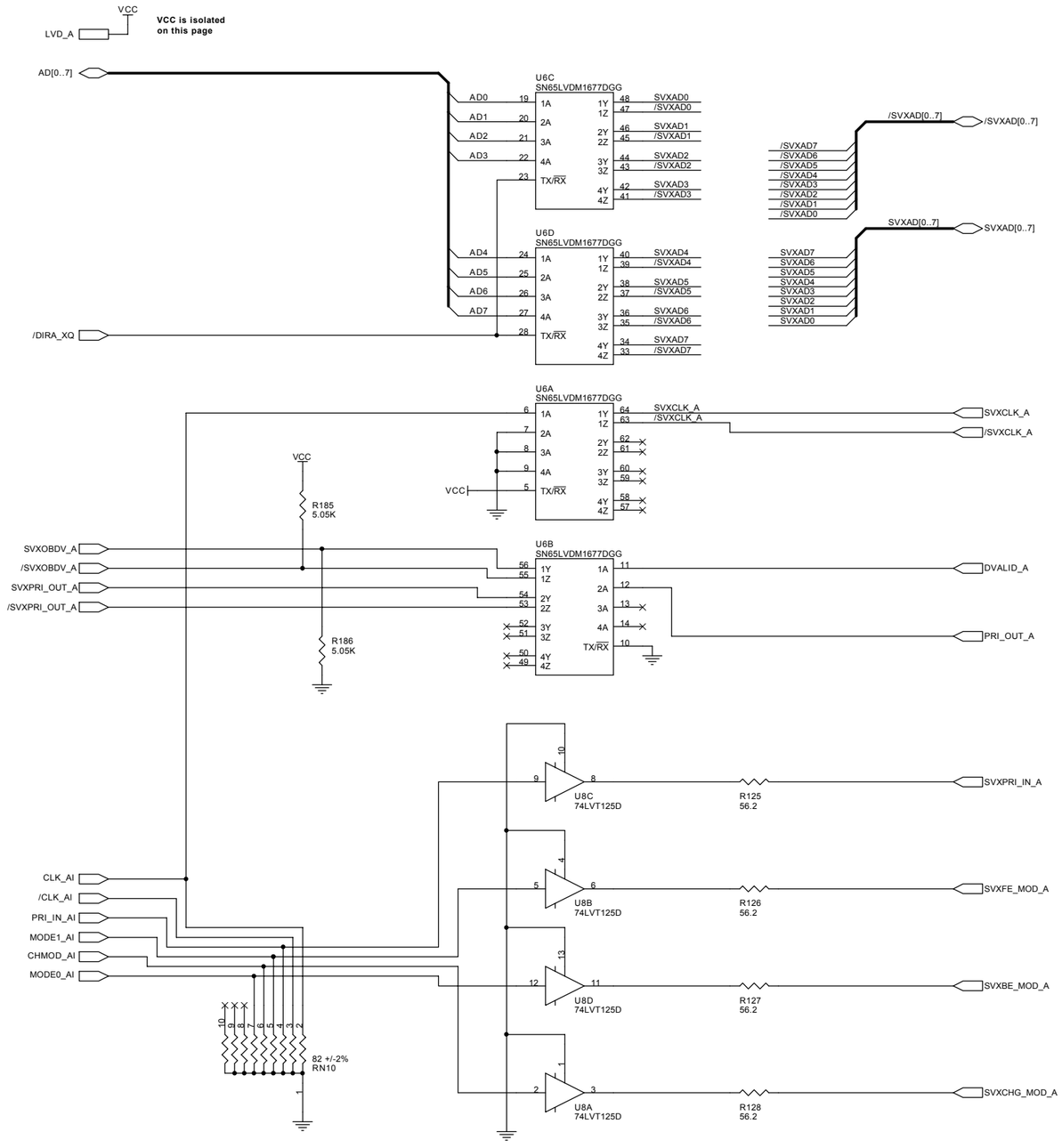
Project: DZero Purple Card			
Project Code: HEP040	Page Title: SASQ Transceivers (Channel B)		
Approvals:	Rev. 3.0	Page Date: Friday, January 24, 2003	CAGE Code: 4B817
	Size: C	Design Date: Friday, January 24, 2003	Sheet 11 of 16



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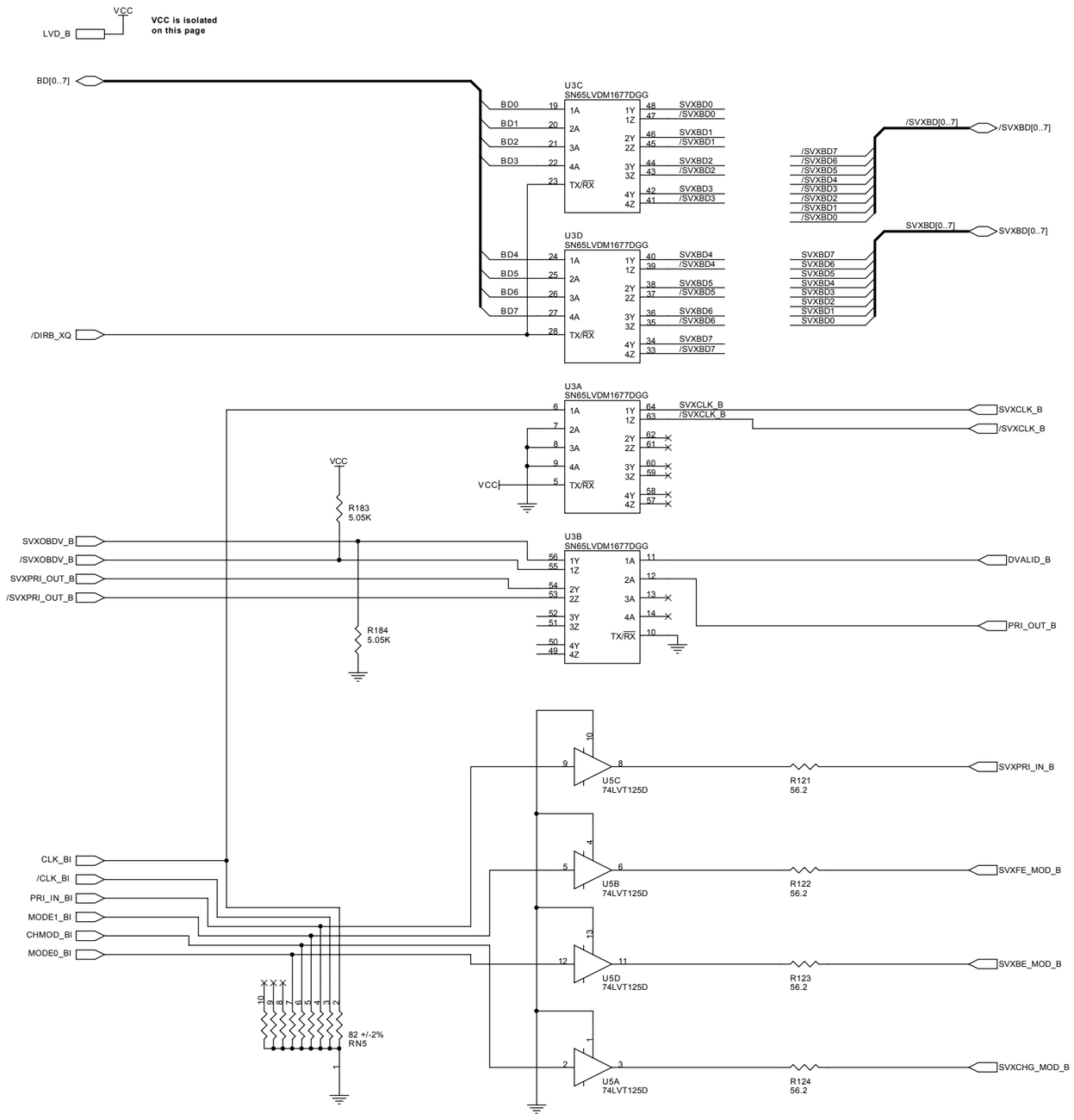
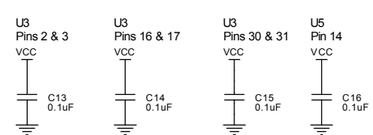
Project: DZero Purple Card			
Project Code: HEP040	Page Title: SVX Transceivers (Channel A)		
Approvals:	Rev. 3.0	Page Date: Friday, January 24, 2003	CAGE Code: 4B817
	Size: C	Design Date: Friday, January 24, 2003	Sheet 12 of 16





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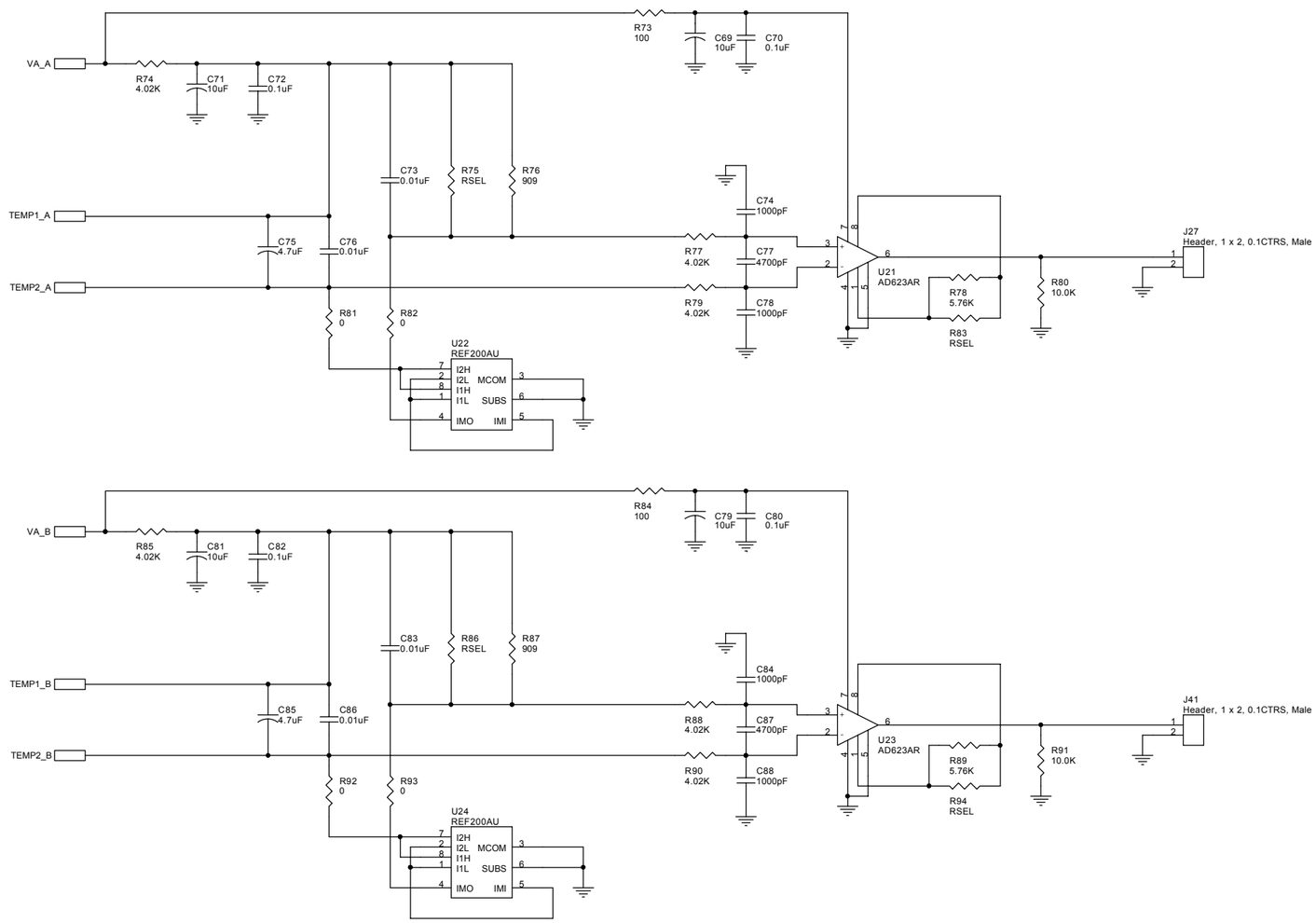
Project: DZero Purple Card			
Project Code: HEP040	Page Title: SVX Transceivers (Channel B)		
Approvals:	Rev. 3.0	Page Date: Friday, January 24, 2003	CAGE Code: 4B817
	Size: C	Design Date: Friday, January 24, 2003	Sheet 13 of 16



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Project: DZero Purple Card

Project Code: HEP040

Page Title: Temperature Monitors (Channels A and B)

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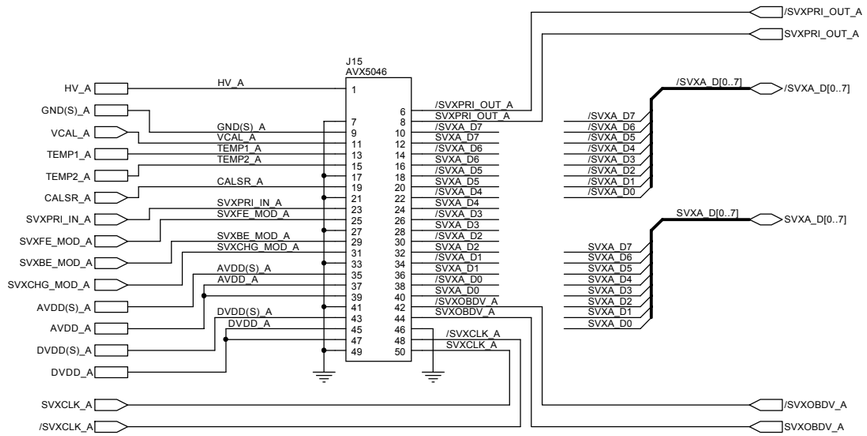
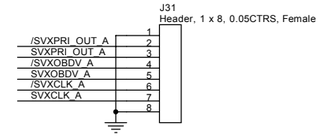
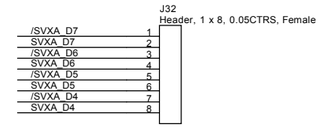
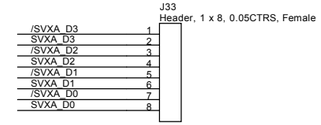
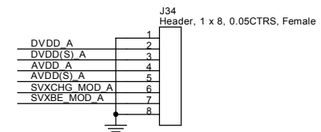
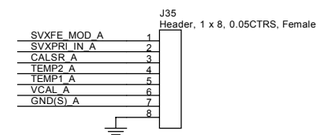




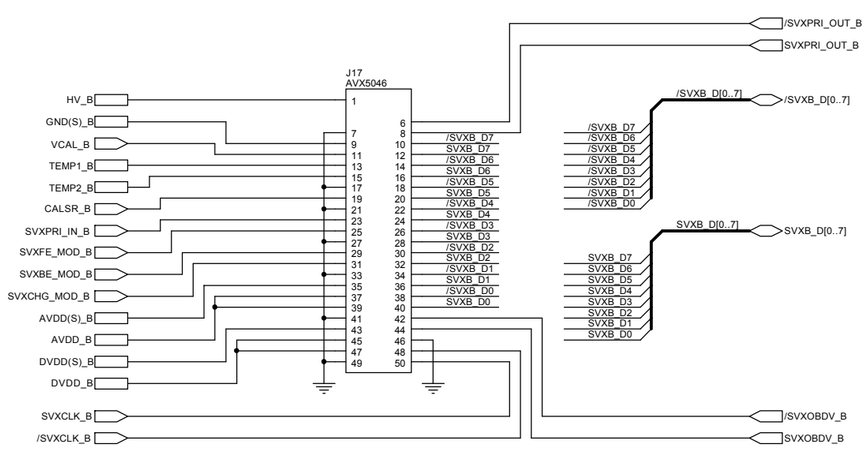


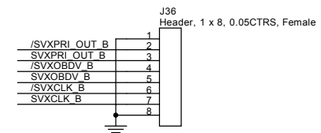


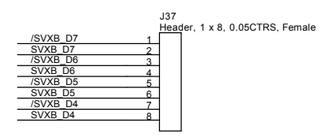


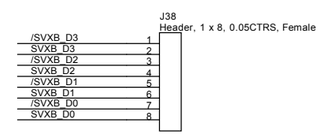


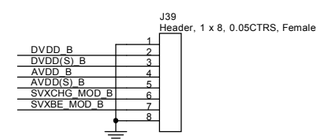
J35 pins 7 and 8 must be connected if testing regulators when SVX is not connected.

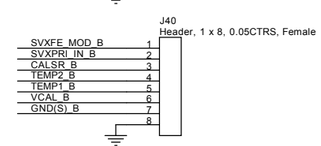












J40 pins 7 and 8 must be connected if testing regulators when SVX is not connected.

EDL
Electronics Design Laboratory

Electronics Design Laboratory
124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400
785-532-7826

Project: DZero Purple Card			
Project Code: HEP040		Page Title: Output Connectors (Channels A and B)	
Approvals:	Rev. 3.0	Page Date: Friday, January 24, 2003	CAGE Code: 4B817
	Size: C	Design Date: Friday, January 24, 2003	Sheet 15 of 16

Rev. 2 Changes

1. Correct wiring on Jumpers J11, J12, and J13.

2. Add 100k pulldowns on the outputs of all solid-state relays.

3. Fix reversed silk on R115 and C96.

4. Rewire AVDD, DVDD, and LVD SSR's to correct adjust pin bias problem. Use VA (switched by HDI_EN) to turn on
regulators via the control input.

5. Correct power monitor reference voltages R1 = R7 = R21 = 8.87k, R13 = R19 = 15.0k.

6. Add 5.11k/10.0k voltage divider to VA input to power monitors to correct comparator common mode voltage problem.

7. Change U17 and U13 from 74ABT04D to 74HCT14D (or 74HCT04D) to yield higher drive voltage to SSR's.

8. Fix soldermask error on regulator heat sink mounting areas.

9. Fix clock polarity. Swap from /CLK to CLK on U3A and U6A. This change takes into account bypassing U10 and U12 -- see #13.

10. Add 5.05K pullups/pulldowns on SVXOBDV and /SVXOBDV (input to U6B and U3B) to prevent oscillation in undriven state.

11. Remove RN2 and RN7. These are now 43 ohms series resistors and are to be completely removed from the design.

12. Add an adjustable resistor in series with R58, R63, R38 and R43 to provide a 2.5+/- .3V adjustment range for AVDD and DVDD.

13. Remove lump delay for dvalid (U4 and U7). Take the
terminated input signals (CLK, PRI_IN, MODE1, CHMOD, and MODE0) directly to the LVDS chips (U8 and U5) with the same terminations, bypassing the ABT25245 (U10 and U12). U10 and U11 would them be used to drive PRI_OUT and DVALID to the SASQ, with DVAILD being daisy chained through multiple gates and a 0.1" jumper being provided to select the desired delay.

14. Change R125 from 90 to 56 ohms.

15. Put op-amps to drive Vcal signals. Drive is 0 to +2.5V into a 4.5k pullup to 2.5V and a 1.5K pulldown to ground (times 10 chips).

16. Replace R137 and R138 (1 MOhm in HV ground line) with a jumper. The capability of placing a resistor in this location will be preserved but it will be stuffed with 0 ohms during assembly.

17. Change to a purple color solder mask if available.

18. Design and build 90 degreee holders for purple card testing.

Rev. 3 Changes:

19. Change VCAL opamp circuit (U31, U32) so that a divide by 2 voltage divider is followed by a unity gain buffer. This will protect the SVX4 from the 5V DAC output of the SASQ.

20. Change resistors R38, R43, R58, R63 from 90.9 to 56.2 to correct adjustment range on the voltage regulators. New
adjustment range is from 1.82V to 2.82V (2.5 +0.32 -0.68).

21. Change R137 and R138 (HV Jumpers) to zero ohm.

22. Change R3, R9, R13, R19 to 23.7k to compensate for regulator adjustment range.

23. Delete R139, R141, R143, R145. These were termination resistors missed in the Rev. 2 changes.

24. Delete R95, R96. These are duplicated with R118 and R188.

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Kansas State University
Manhattan, KS 66506-0400
785-532-7826

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Approvals:	Rev. 3.0	Page Date: Friday, January 24, 2003	CAGE Code: 4B817
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