

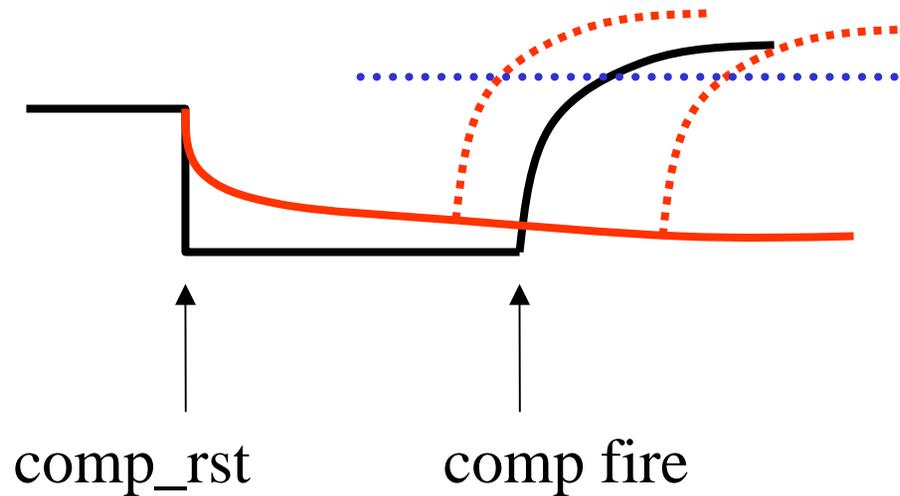
Status of SVX4 testing at DØ

Kazu Hanagaki / Fermilab

- Who is working? Len Christofek, Marvin Johnson, Andrei Nomerotski, Petros Rapidis, Mike Utes, and myself.
 - Major known problems.
 - D0 operation (i.e. needs FE clock for PRD1).
 - Pedestal non-uniformity across the channels;
1) bow or slope, 2) channel to channel variation
 - Pedestal non-uniformity across the pipeline cells.
 - Some observations on the comparator.
 - Readout related stuff (frequency scan, double readout...)
 - Still working on gain and noise measurement.
 - Checklist based on the specification (a few examples) and yield test on hybrid.
 - Summary and plan.
- 

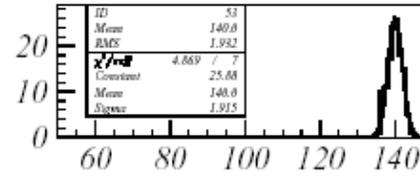
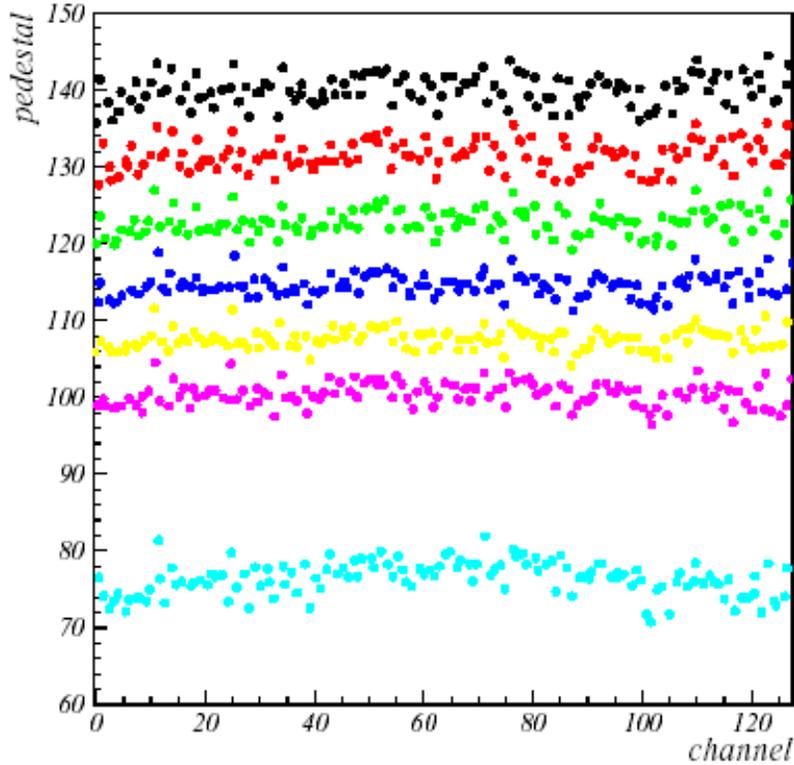
Comparator issue

Signal in the output buffer seems to need some time to be stable.

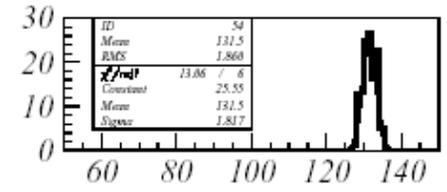


- Internal delay depends on the time interval between `comp_rst` and when the comparator fires.
- Pedestal should depend on this time interval.
- Expect pedestal increase for larger interval.

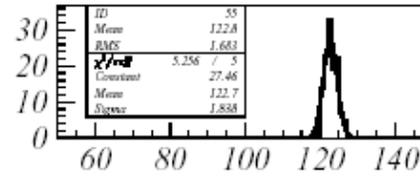
Observation



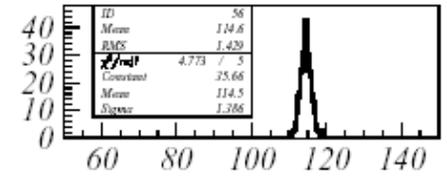
FE 5 Ped 3



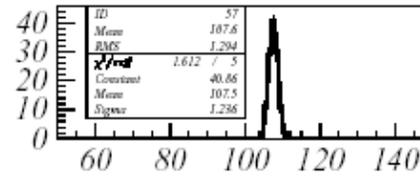
FE 5 Ped 4



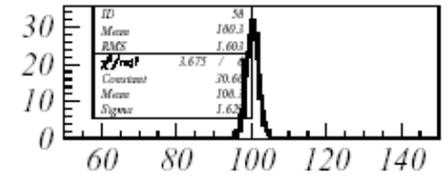
FE 5 Ped 5



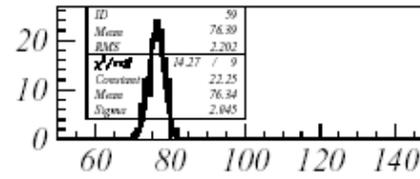
FE 5 Ped 6



FE 5 Ped 7

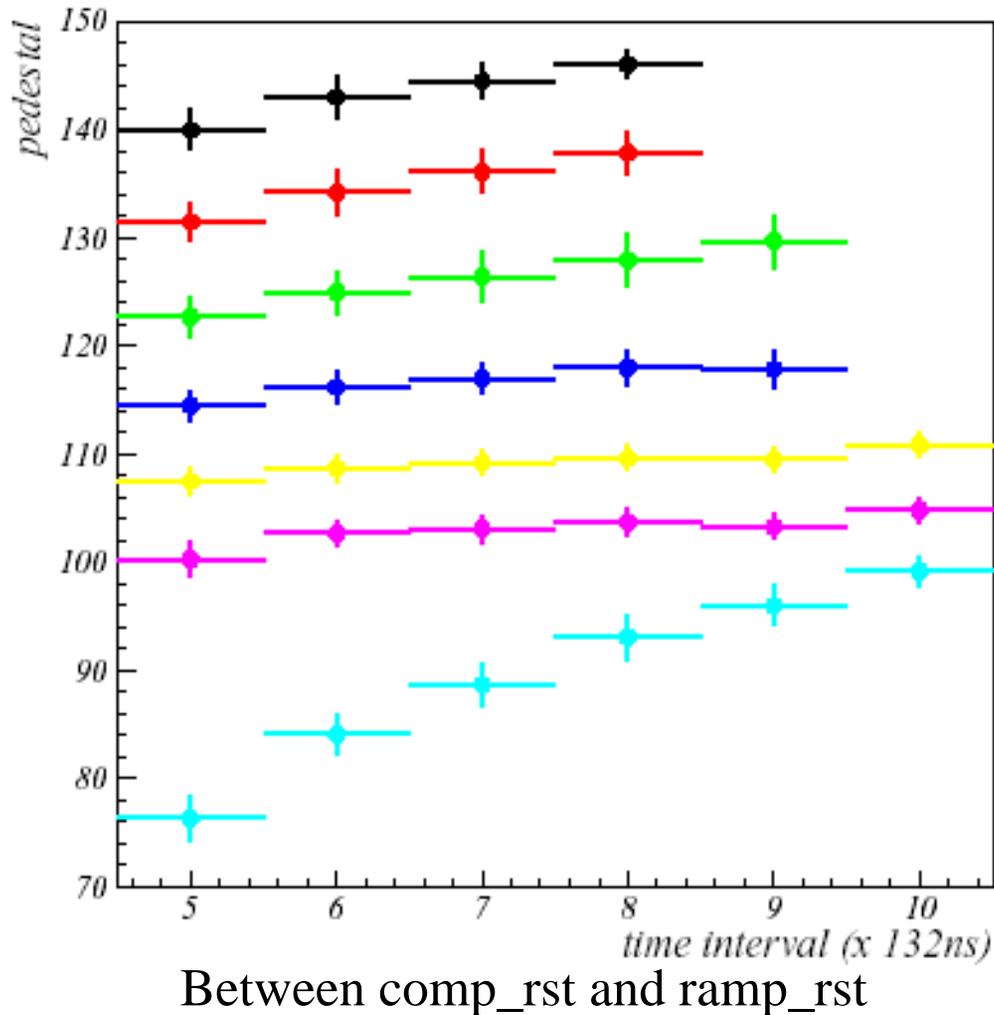


FE 5 Ped 8



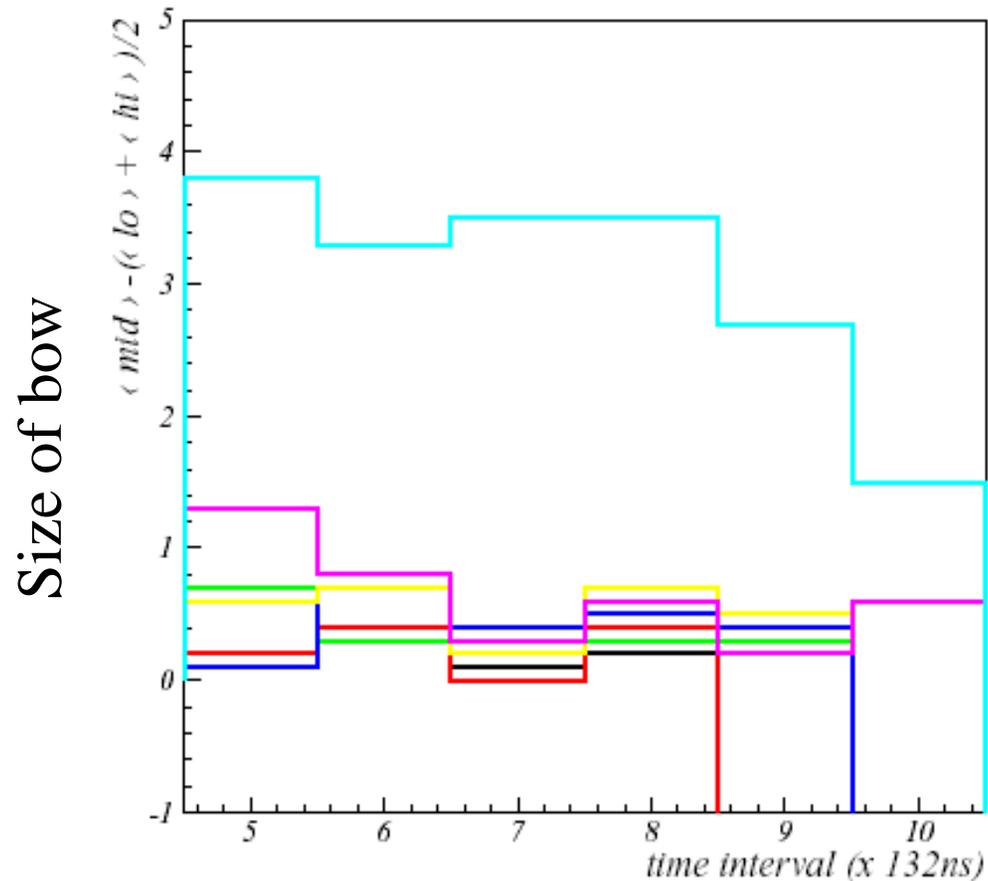
FE 5 Ped 9

Pedestal shift



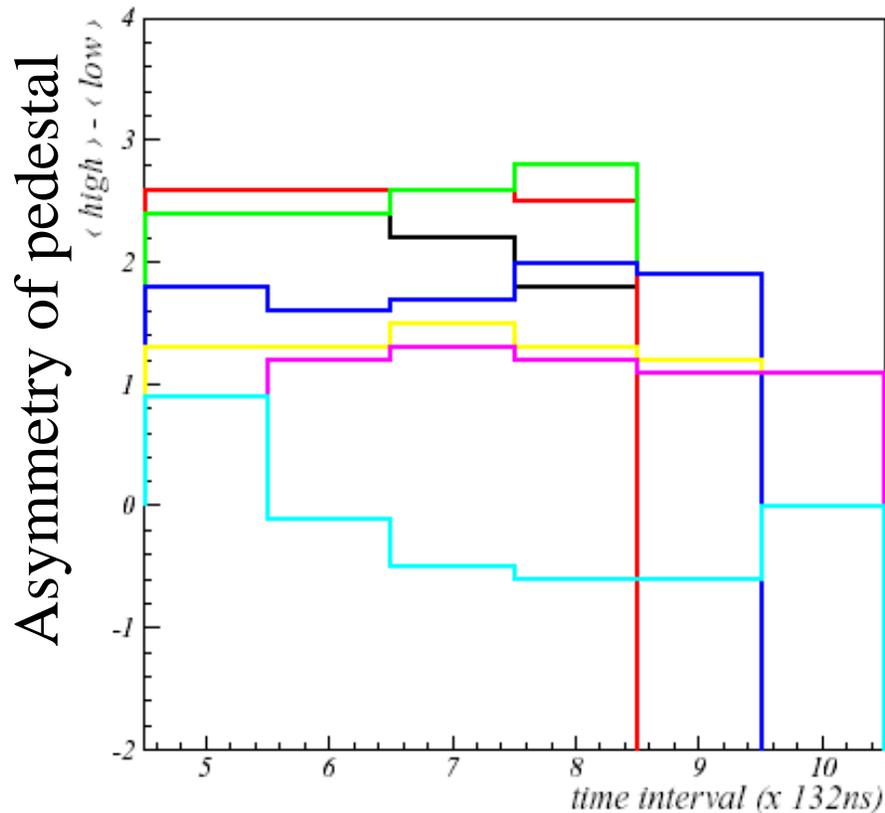
- The behavior is consistent with the expectation.
- **NOTE!!** What relevant here is the time interval between comp_rst and when comparator fires, i.e. longer is more stable.
- A setting with higher pedestal value has longer time interval internally.
← the dependence is less.

Size of bow



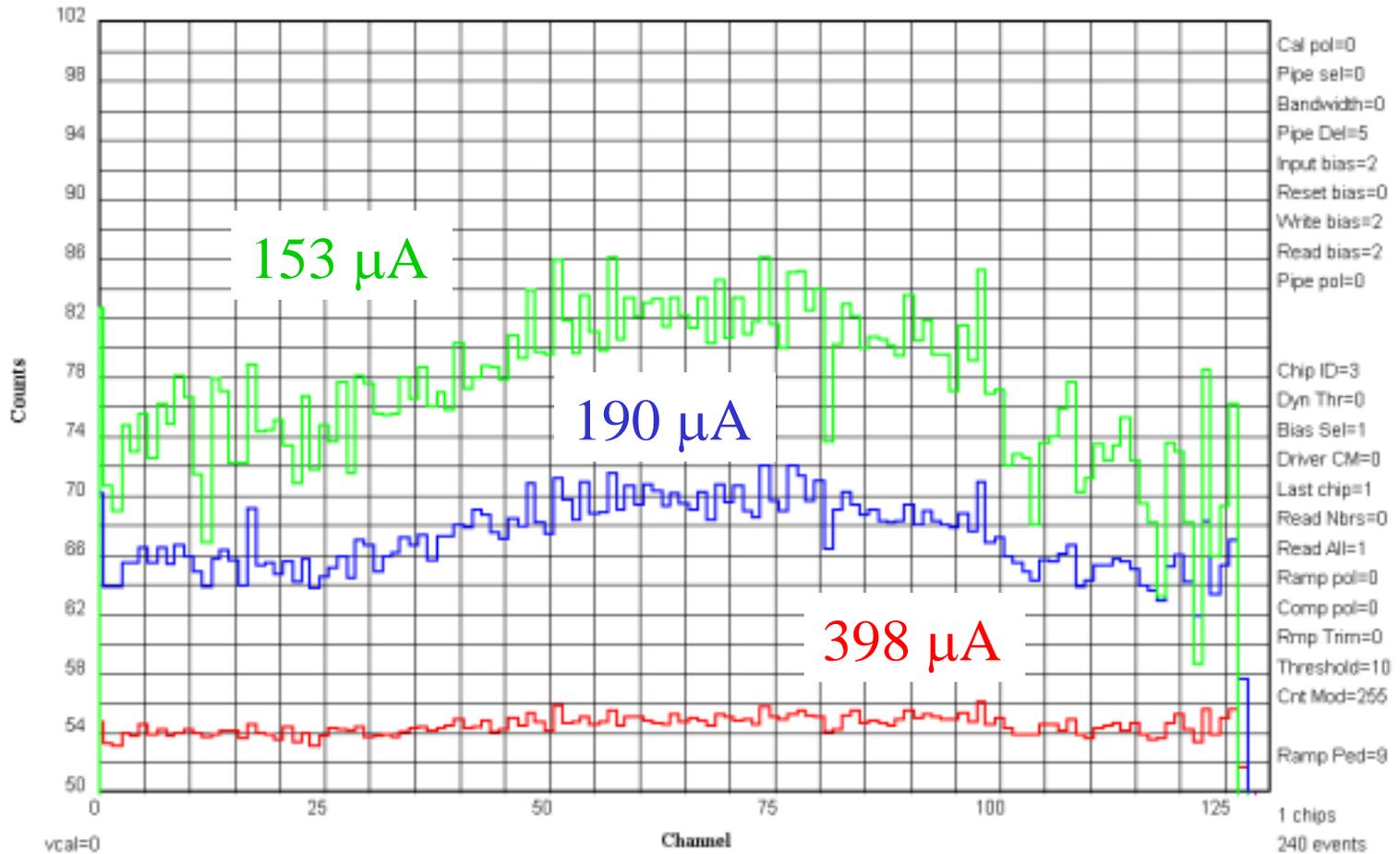
- The bow disappears after the long time interval. (= after the comparator reaches the saturation point, or stabilization.)

Size of slope

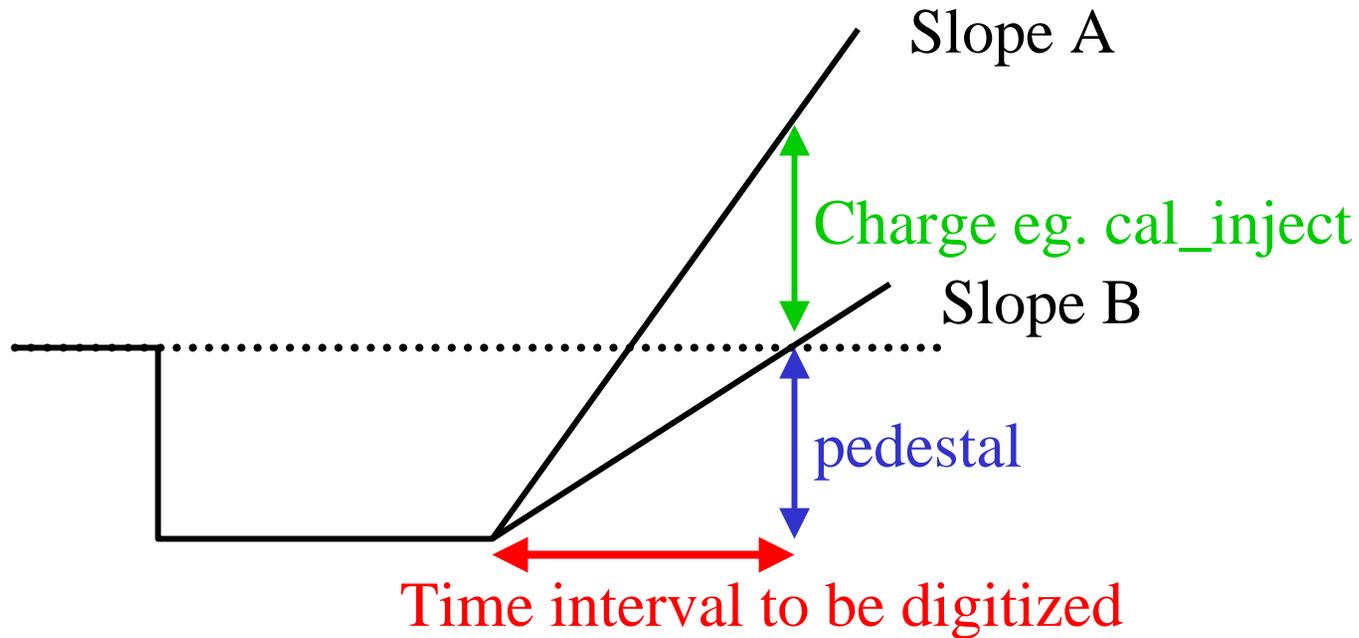


- No bow, but slope exists...
- All we know is that the comparator seems to cause the non-uniformity of pedestal. Tom says the comparator performance is not robust by its design, for example, the geographical effect.
- But we don't understand the geographical effect which really brings the non-uniformity.

Dependence on IQUI (comparator bias current)

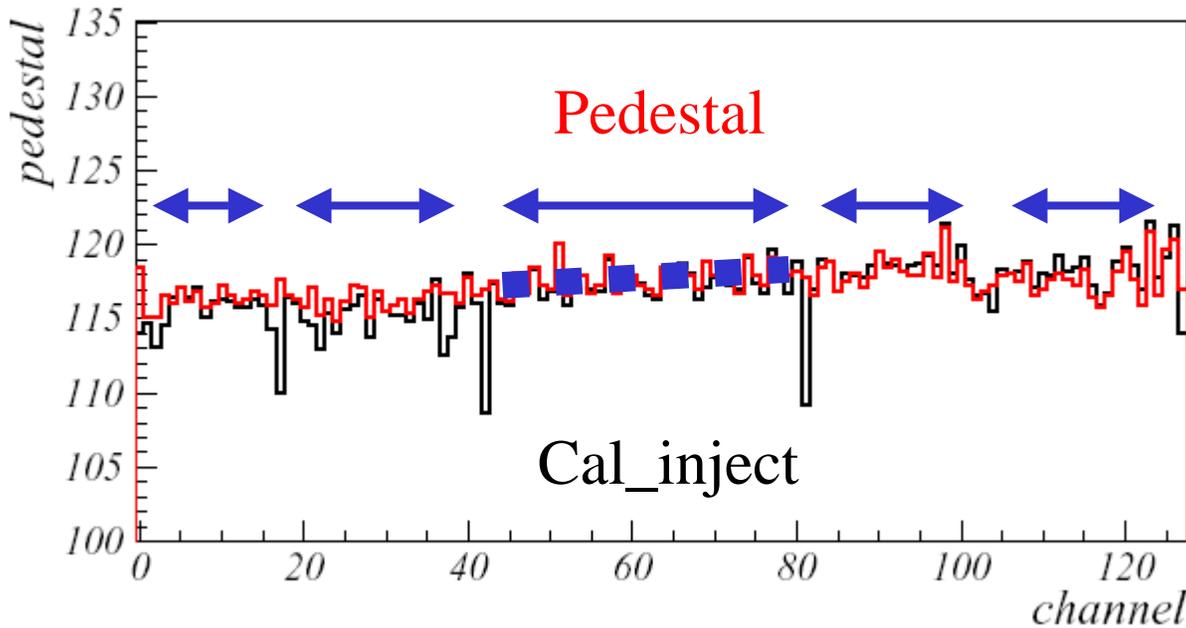


No dependence on the input to ADC?



- Adjust the injection charge so that ADC counts with slope A is the same as the pedestal with slope B.
- When slope $A = 2(\text{slope B})$, for example, the non-uniformity should be as twice as slope B, if the non-uniformity comes from the input to ADC. (assuming the cal_inject is uniform across the channel.)

Channel to channel variation



Slope in
each region

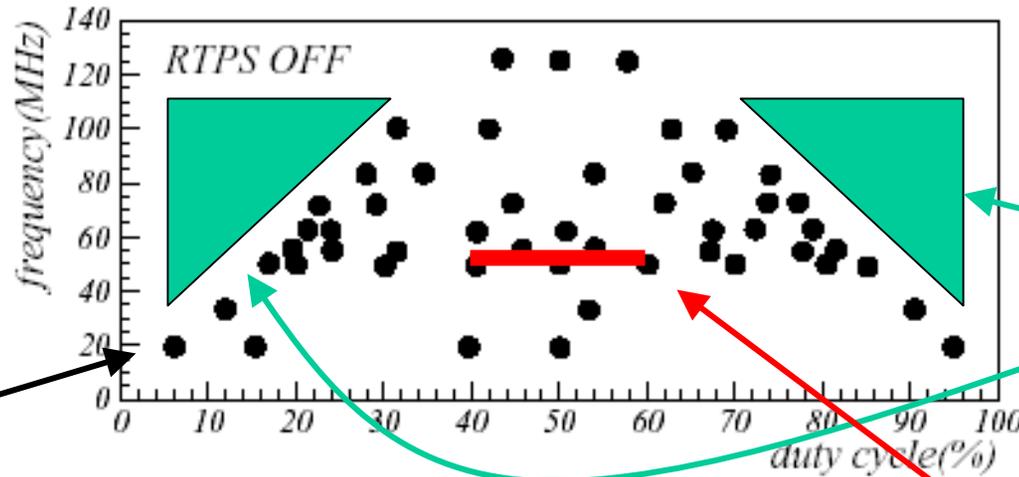
	1st	2nd	3rd	4th	5th
ped	0.046	0.028	0.027	0.039	0.057
cal	0.048	0.027	0.028	0.011	0.066

- The shape is consistent each other both visually and numerically.
- ➔ No effect from the input.

Frequency Scan for digitization

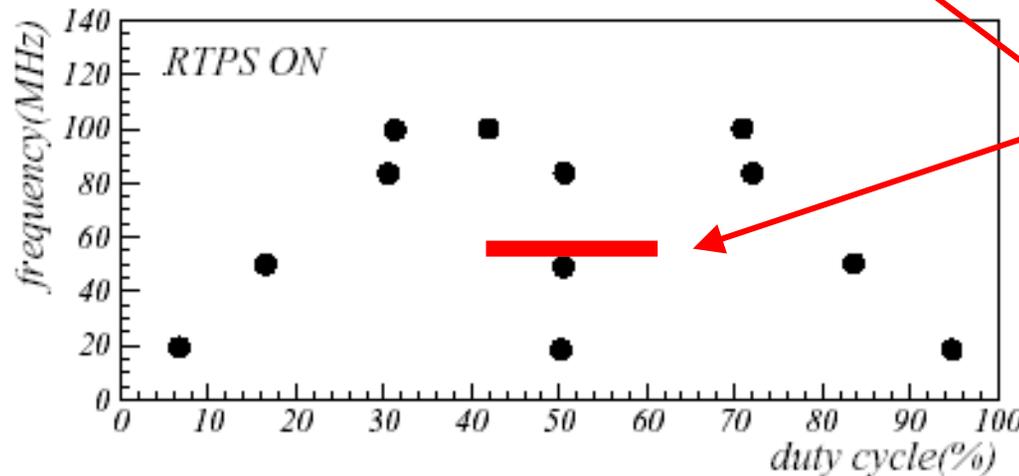
(thanks to Len for fixing the DAQ problem)

Confirmed both pedestal & cal_inject are consistent with expectation.



Did not measure these regions

Operation range

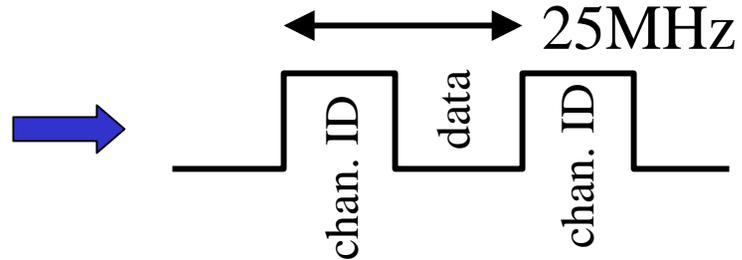


No failure so far → very large frequency margin!

Frequency Scan for readout

- Len and Mike worked on the readout frequency scan.

For example,
BE clock = 50MHz

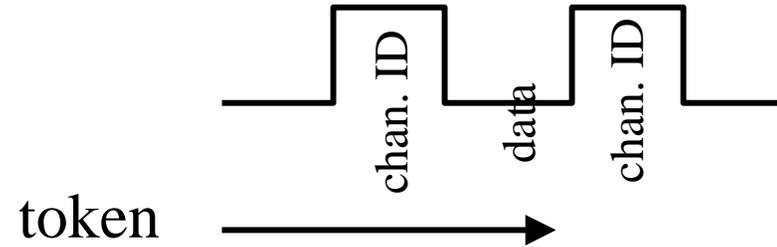


BE clock \ Duty cycle	40%	50%	60%
100MHz	Blue	Blue	Blue
72.4MHz	Blue	Green	Blue
50MHz	Blue	Green	Blue

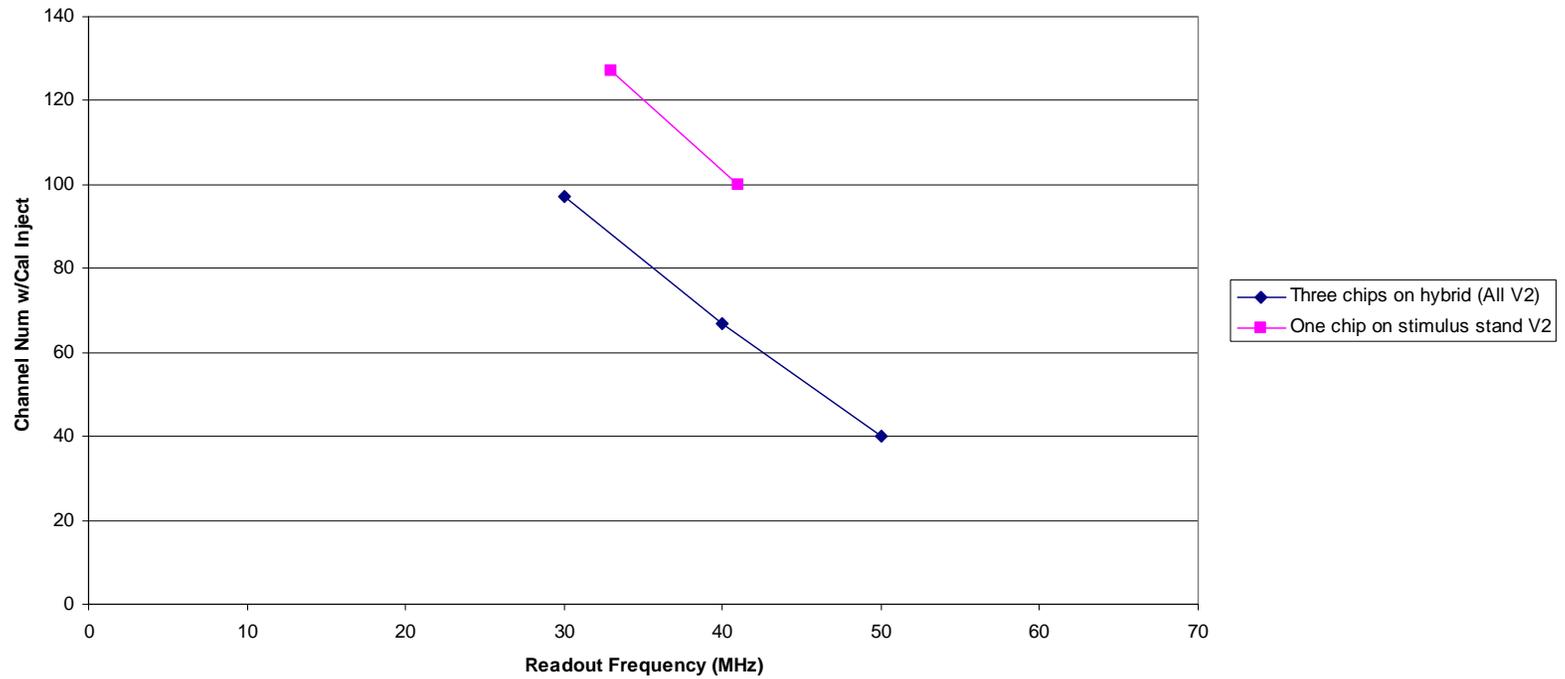
Usual
operation
range

- ✓ confirmed by single chip operation.
- ✓ confirmed by hybrid (4chip).

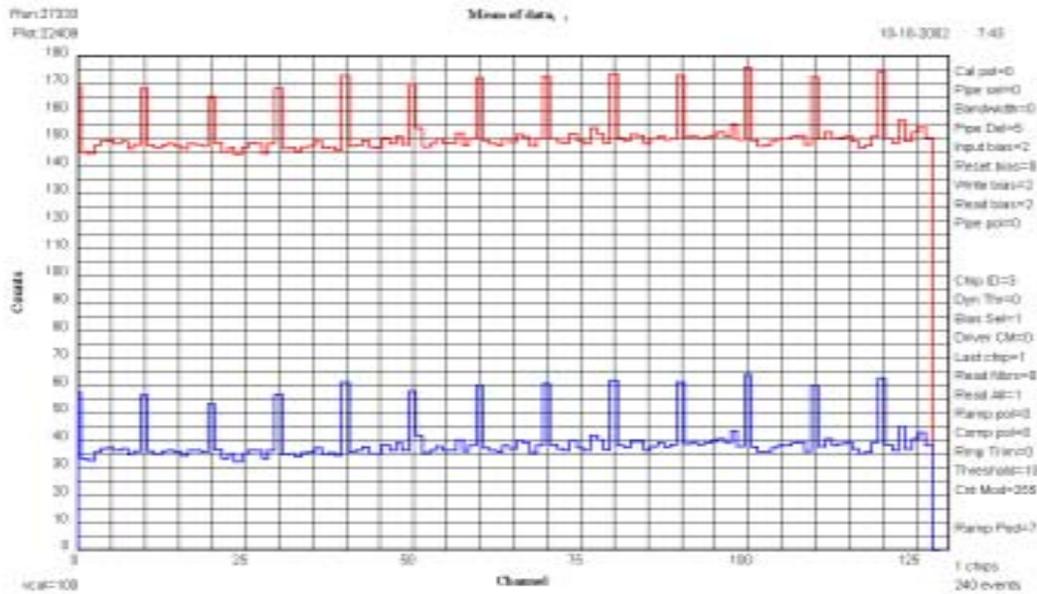
Double readout



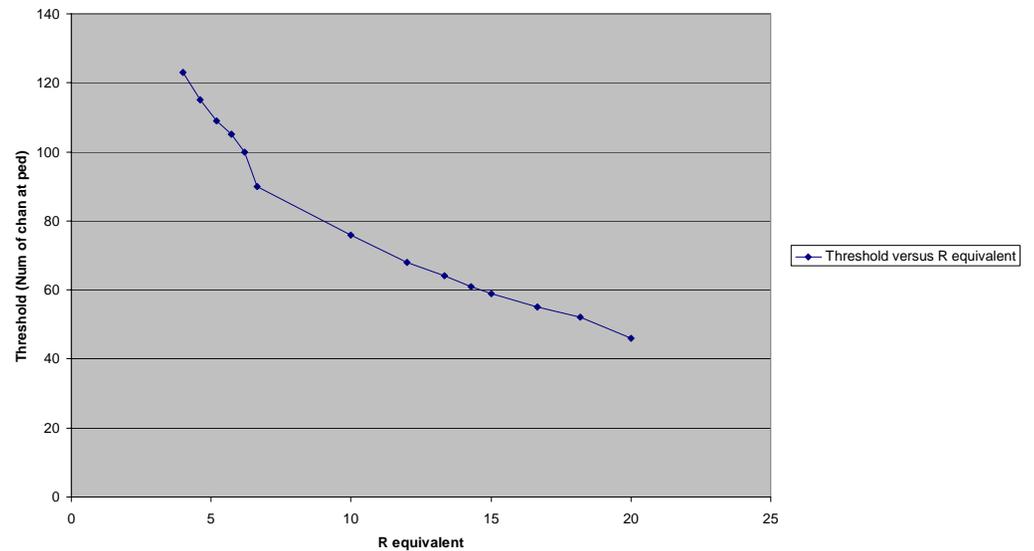
Double Readout as a Function of Frequency



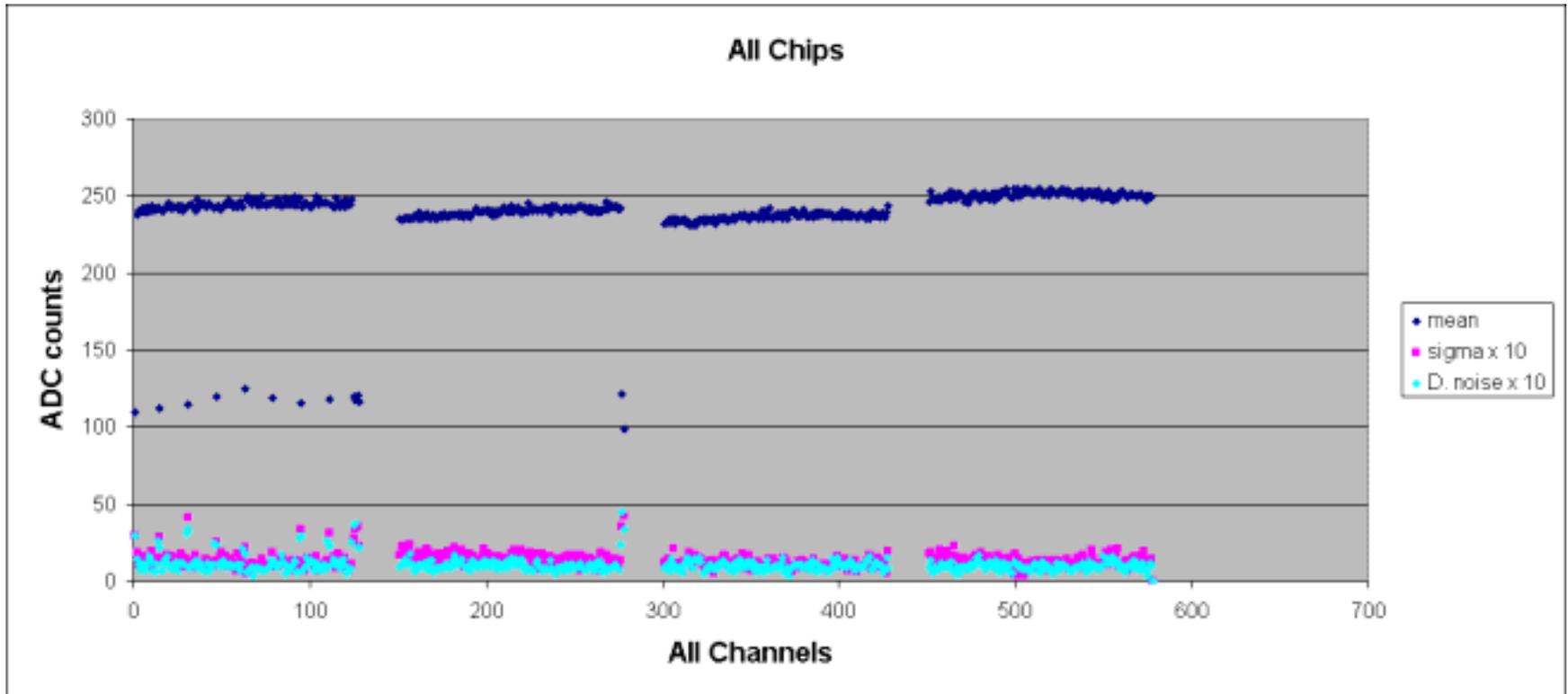
Real Time Pedestal Subtraction



Threshold versus R equivalent



Multi-chip operation



- Read-neighbor works fine with adjacent chip.
- Other configuration bits works OK across the chip.

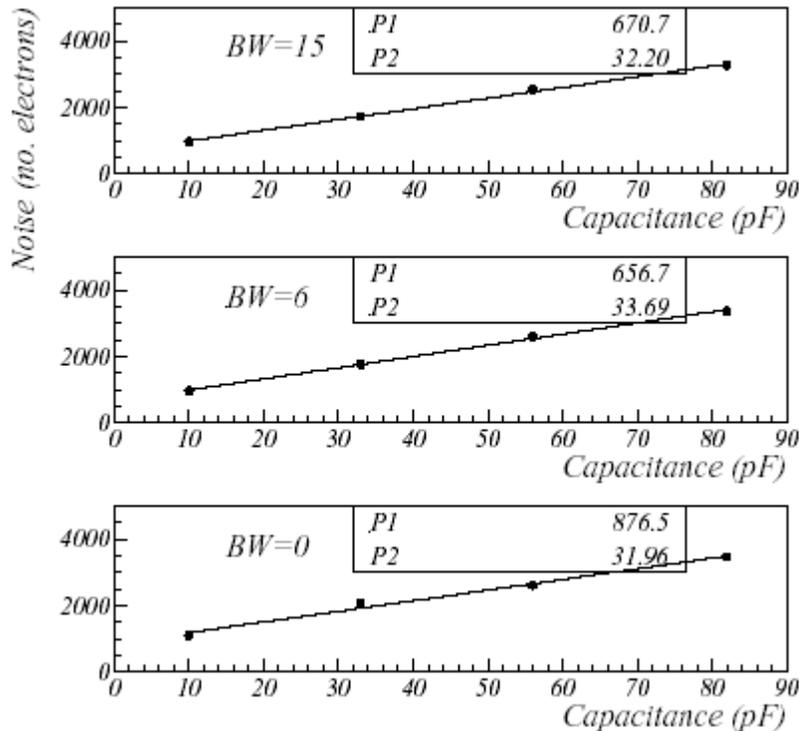
Gain measurement

BW	10pF	33pF	40pF
LBL(50MHz equivalence)	#electrons / ADC count		
0	877	923	
6	936	1009	
15	1013	1217	
FNAL(latest)	#electrons / ADC count		
0	700		679
6	714		849
15	676		1043

- Still discrepancy.
- Chip dependence, channel dependence, or...
← needs more work.

Noise (defined as RMS of pedestal distribution)

@LBL



For **fixed BW** setting (=15)
→ rise time not fixed

	@LBL	Tom's frontend
10pF	993	794
20pF	1315	1034
30pF	1637	1434

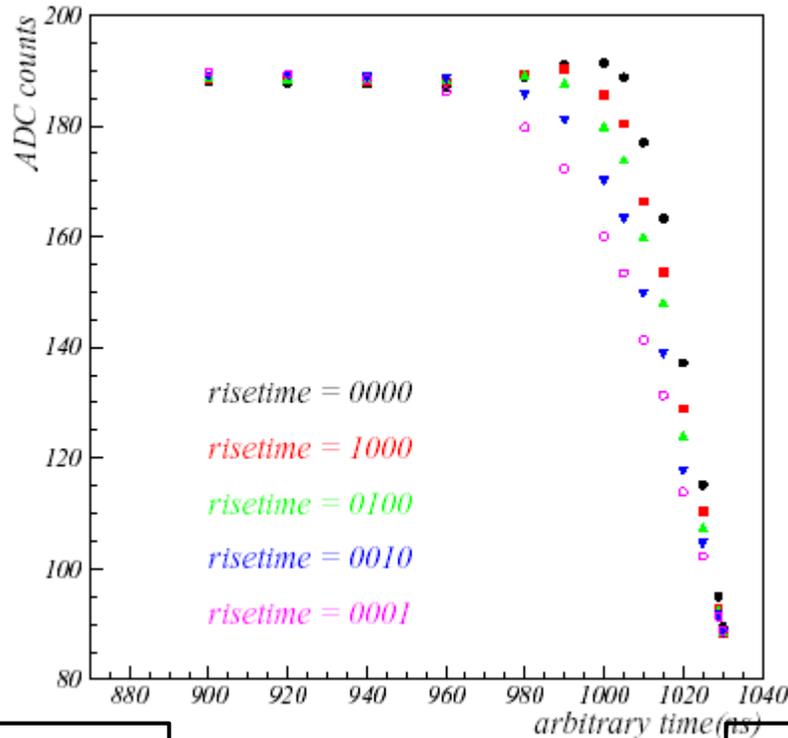
← (~500 electrons) of additional setup noise?
 (Note this is <0.5ADC counts)

Noise --- continued

- For **fixed rise time** (69ns) by Tom:
ENC $\cong 300 + 41C$ (2025e⁻ @40pF)
cf. this was 450 + 43.5C for the front end test chip.
- Spec. < 2000e for 40pF @ 100ns rise time.
→ Tom's result indicates very good noise performance.
(even the LBL result meets the spec.)
- **Version dependence?**
Should not exist, but the purpose of test is to check or confirm something which should be...
- **Chip to chip variation?**
- There seems to exist common mode (or other) noise in the FNAL setup. We need to solve this to make the noise study possible.

Rise time measurement by digital info.

- Most of the front-end measurement has been done by Tom Zimmerman using analog signals. But some can be done with digitized information. ← This is important as a cross-check, and for massive tests.



Rise time (ns)

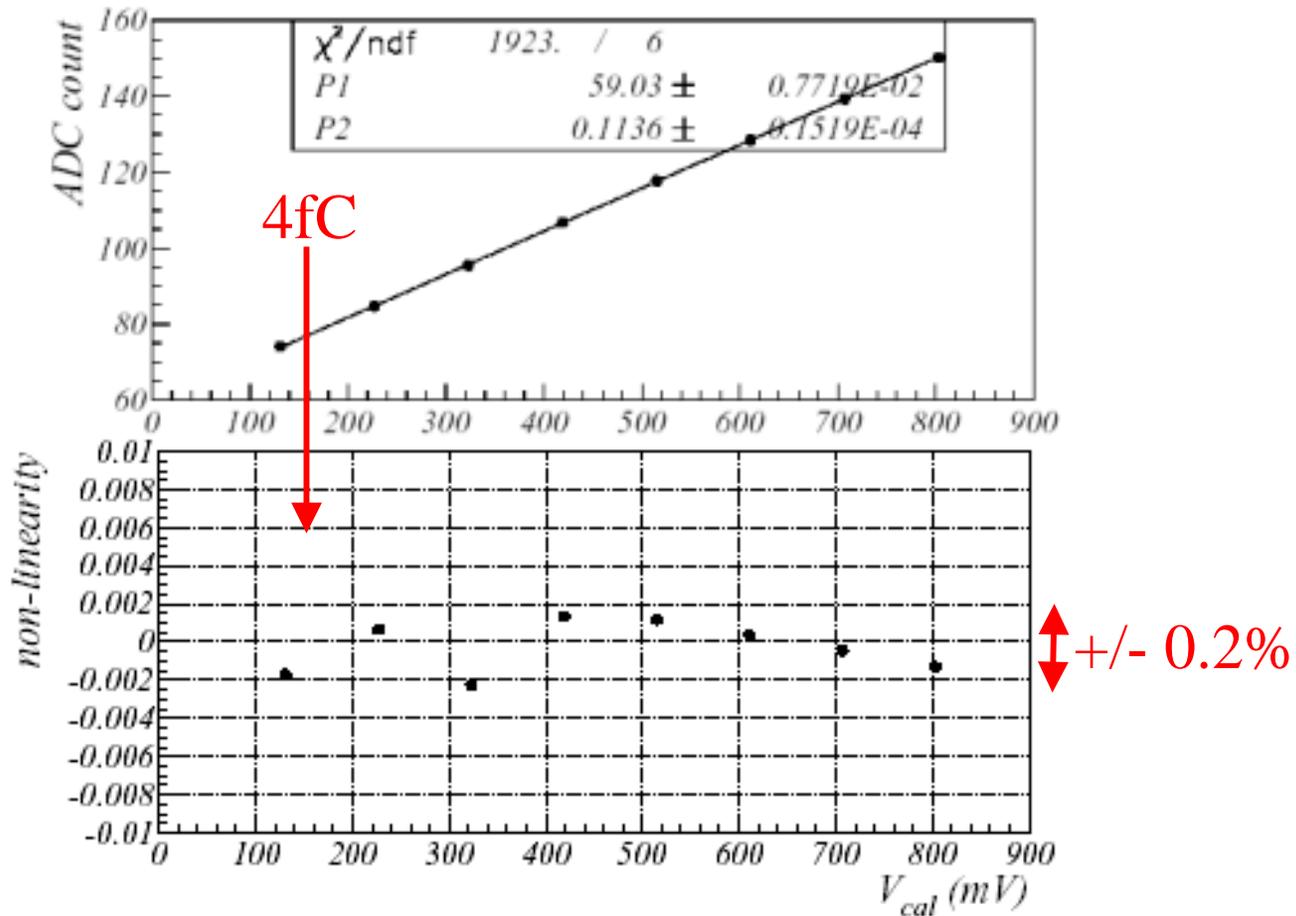
BW	10pF	33pF
0	19.0	37.9
1	22.8	45.3
2	27.2	53.1
4	35.1	65.4
8	48.3	81.5

Design: $25\text{ns} + (\text{BW} \times 4\text{ns})$ for 10pF



Non-linearity measured by cal_inject

- Non-linearity \equiv ADC(meas) – Expectation(by the fit)



- Note!! This includes not only ADC but also the front-end.

Data output driver

- Measured the voltage between bus and bus-bar (differential signal with 100Ω termination).

Output driver current

bit	Meas.	design
001	5.6mA	5.6mA
010	9.4mA	9.2mA
100	13.2mA	13.4mA

- Also measured the rise time and fall time to be $\sim 3\text{ns}$.

1. Preamp

Gain		3mV/fC	×
Gain uniformity	y	5% over	×
Input capacitance		10pF 50pF	×
Reset time		adjustable for 60-100ns any allowed	×
Resolution	t	4bits	×
ENCe		< 1000e	×
Linearity		on linear pulses up to 20fC. Non-linearity < 0.05mV.	×
Dynamic range		>200fC	×
Reset settling time		< 1μs for y initialization.	×
Calibration		40fC external switched to input.	25fF

2. Amp

Gain		3 to 5.	×
Gain uniformity	y	5% channel to channel.	×
Reset time		10ns 40ns.	×
ENCe	at input	< 500e	×
Linearity		on linear up to 20fC input	×
Dynamic range		>40fC at input.	×
Reset time		< 20ns for y initialization.	×
Pedestal uniformity		< 500e input channel to channel.	×
		input coll.	failed

3. ADC

Rate	3 bits				×
Resolution	4bits				×
Linearity	0.5%	between 0 and	1/V	μ s	×
Counter	8 bit	106MHz rate.			×
Differential	non-linear	y	< 0.5B.		needs to be checked

4. Data driver

Current source range	21025mA		×
Rise and fall times	>2ns and <4ns.		×
Bi-directional	All bus pads are I/O for D0.		×
Single use	No additional	t.	×

5. TN/BN pins

BN/TN pins	Only active initialize		??
Priority in/out	registers configuration	input/output	
	initialize		×
	Priority changing	no	×
	Priority high	initialize	×

6. Control functions

Ramp	Counter Reset	In formal to Reset . In Dynamic pedestal subtraction Counter Reset is generally.	ter Reset is		×
Preamp Reset & CF	k	Preamp Reset should	ays function		×
PRD1		indep	tly of CF	k state.	×
PRD					×

Register configuration

Check for the ~~AD~~ ~~CF~~ ~~parameters~~ ~~for~~ ~~_inject~~,
~~etc~~.

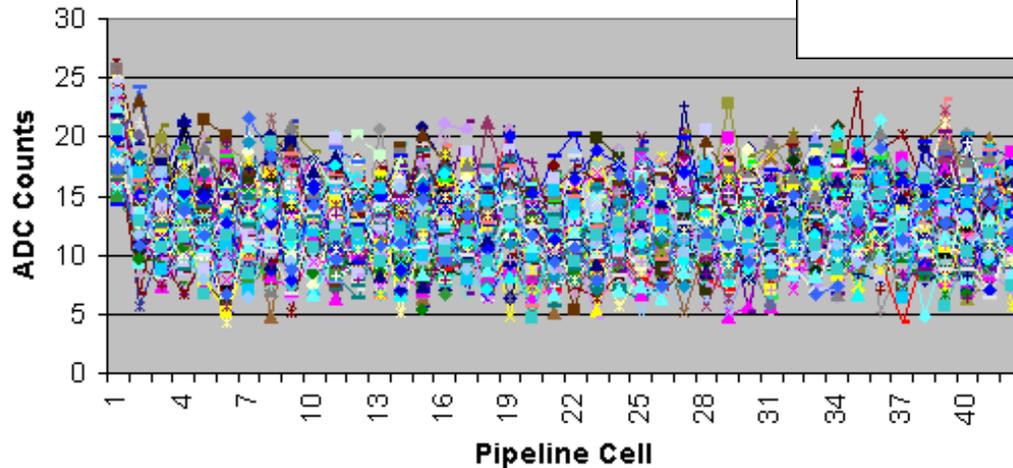
Cal_inject	×
Bandwidth	×
Ramp	×
Preamp	t
Written	t
Write	t
Depth	×
Driver current	×
Threshold for sparsification	×
Counter mode	×
Chip ID	×
Position	×
Read-neighbor	×
Read channel 63	×
Read channel 127	×
Pedestal adjustment	×
Reversed Polarity	×

Yield

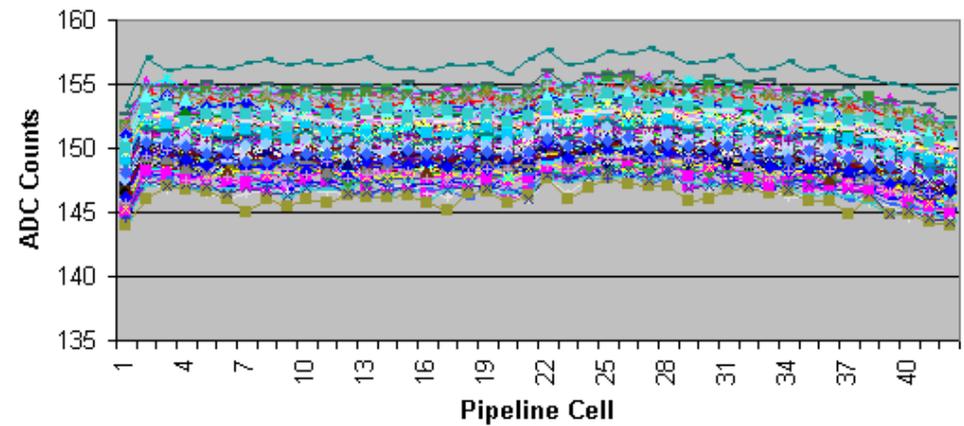
For all channels and pipeline cells, the following three items have been tested on hybrids.

- Pedestal
- Noise
- Cal_inject

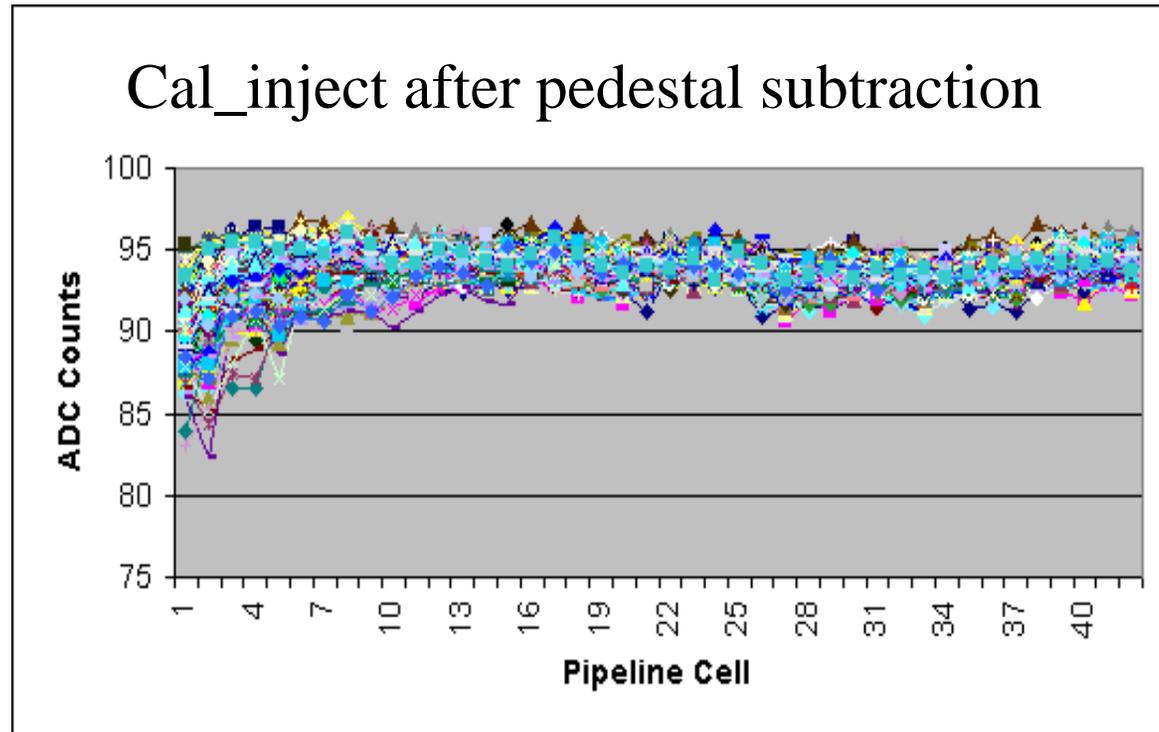
Total noise x 10



Average pedestal



Yield --- continued



- 17 chips tested on the hybrid. 16 seems OK. → 94%.
(7 out of 17 is ver.2, 10 is ver.1.)

Summary & Plan

- Check list going through most of the specification. But not all of them. → Do we add more? (To do list by Maurice)
- **The most are within the specification.**
- The pedestal non-uniformity (across channels) seems to be caused by the comparator. Not fully understood yet.
- Yield: 16/17 (=94%) ← Very preliminary.
 - Chip to chip variation (eg. Gain, pedestal)
← wafer level testing.
 - Temperature dependence.
 - Yield and long term effect. ← on the hybrids.
 - Full chain readout test with D0 DAQ configuration.