Status of SVX4 Testing

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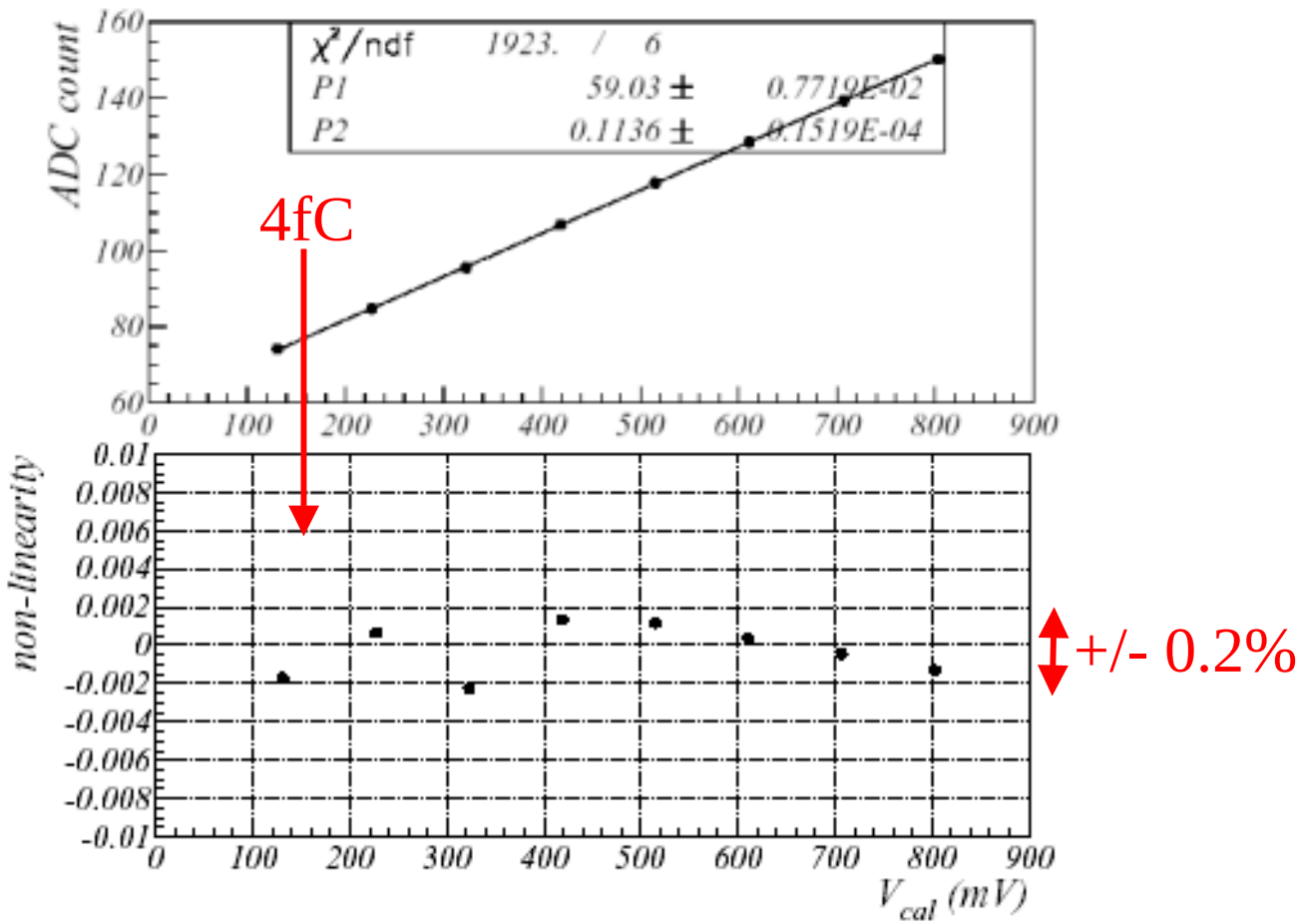
- Check list based on the specifications. These are very detailed tests. ⇐ some examples.
  - ADC
  - Back-end
  - Front-end
- Still working on gain and noise measurement.
- Another observation on the comparator.
- The D0 operation issue is one the most important ones, but not mention here.

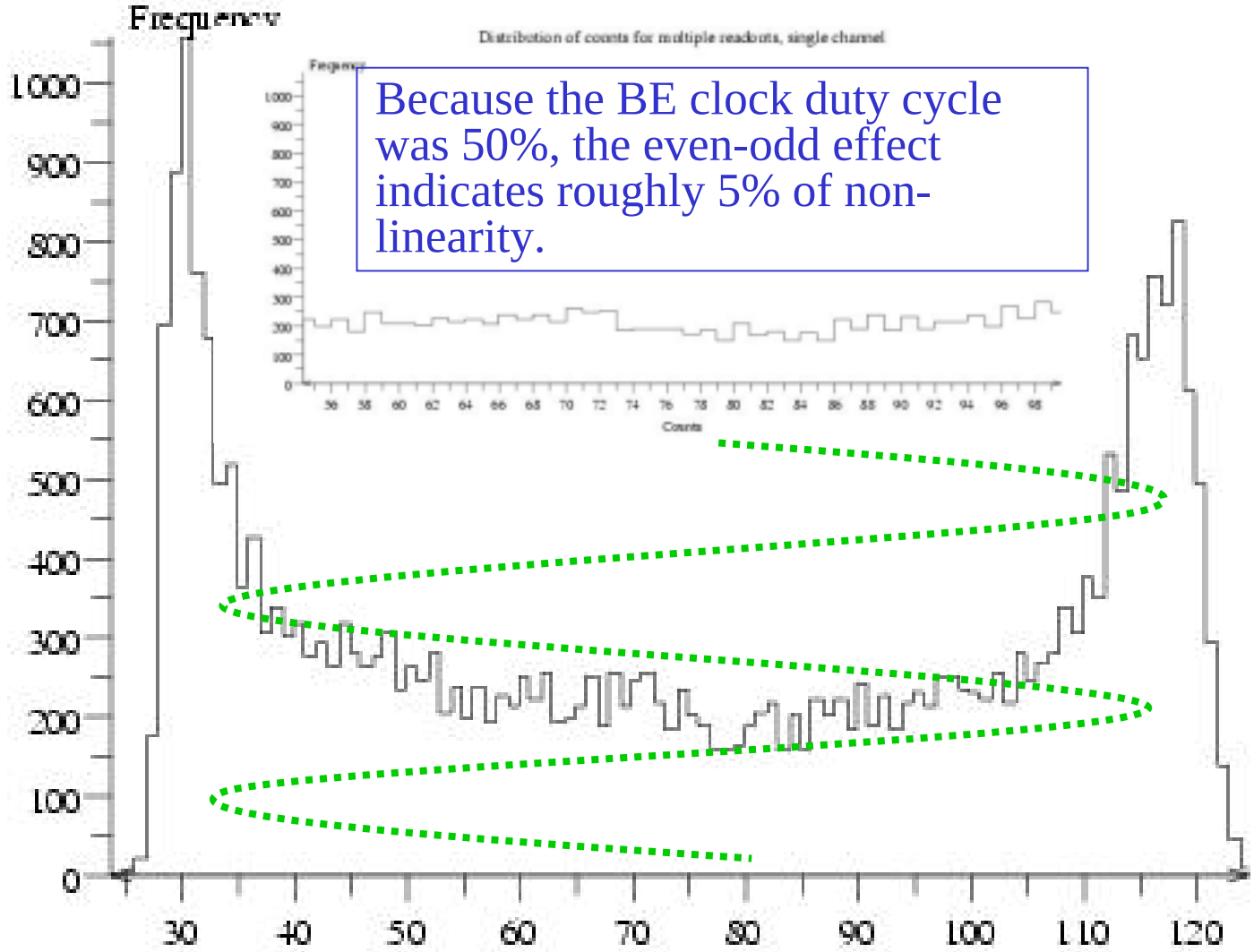
Non-linearity measured by cal_inject

- Non-linearity ≡ ADC(meas) – Expectation(by the fit)



- Note!! This includes not only ADC but also the front-end.

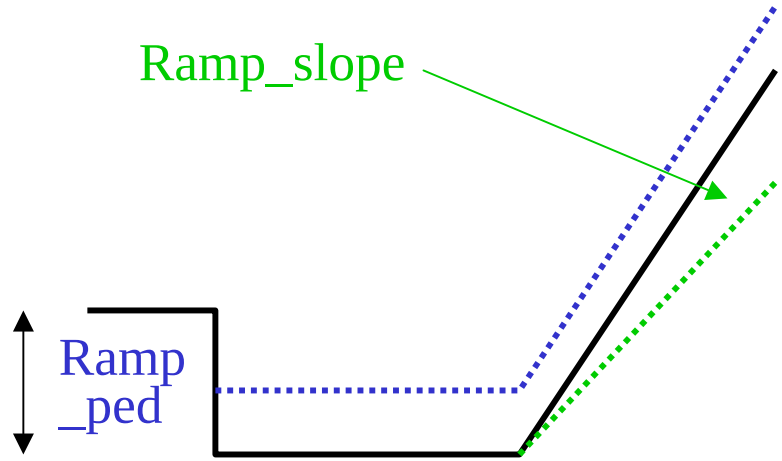
Differential non-linearity measured by random sine wave



Because the BE clock duty cycle was 50%, the even-odd effect indicates roughly 5% of non-linearity.

- More quantitative additional test would be nice.

Configuration bits for ADC



Ramp_ped

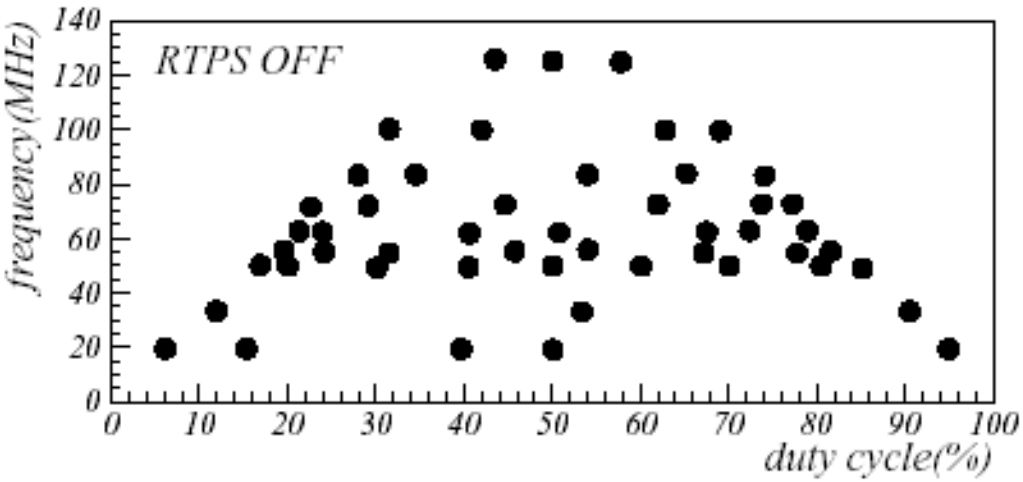
Decimal setting	Bit stream (LSB-MSB)	V_{ped} (mV)
0	0000	-286
1	1000	-268
2	0100	-243
3	1100	N/A
4	0010	-191
5	1010	-167
6	0110	-141
7	1110	-119
8	0001	-94.8
9	1001	-70.9
10	0101	-50.1
11	1101	-26.2
12	0011	close to zero
13	1011	19.8
14	0111	45.1
15	1111	65.8

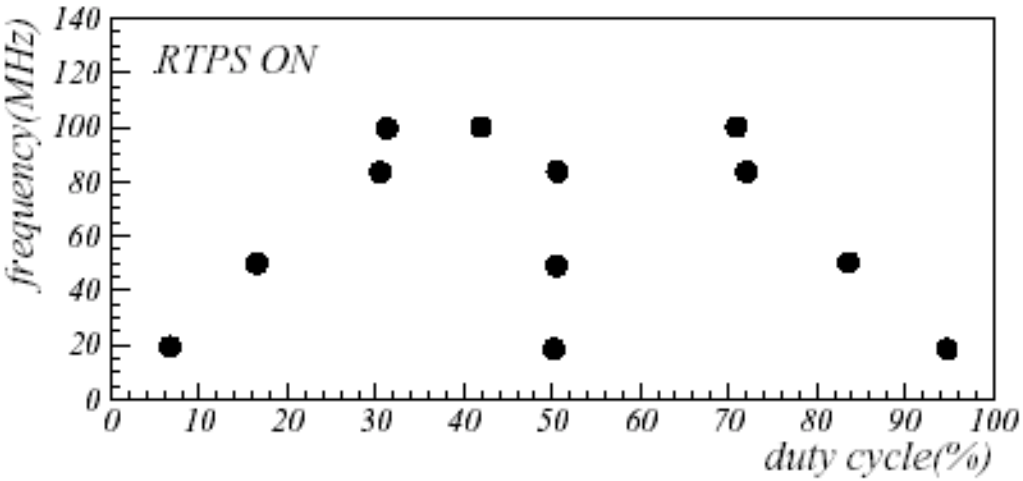
Ramp_slope

bit stream (bit0, bit1, bit2)	measure	design
000	0.471	0.471
001	0.243	0.236
010	0.162	0.157
011	0.122	0.118
100	0.161	0.157
101	0.120	0.118
110	0.097	0.094
111	0.083	0.079

- Ramp_ped is binary weighted as designed.
- Ramp_slope = 0.5(mV/ns) / [1+2(bit0)+2(bit1)+1(bit2)]

Frequency Scan (thanks to Len for fixing the DAQ problem) & Output driver



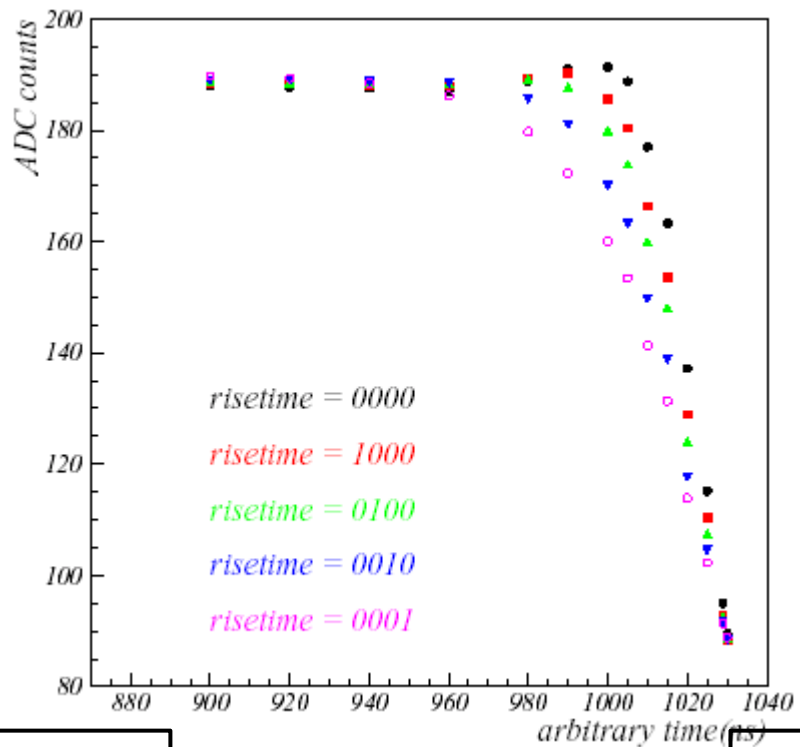


Output driver current

bit	Meas.	design
001	5.6mA	5.6mA
010	9.4mA	9.2mA
100	13.2mA	13.4mA

Rise time measurement by digital info.

- Most of the front-end measurement has been done by Tom Zimmerman using analog signals. But some can be done with digitized information. ← This is important as a cross-check, and for massive tests.



Rise time (ns)

BW	10pF	33pF
0	19.0	37.9
1	22.8	45.3
2	27.2	53.1
4	35.1	65.4
8	48.3	81.5

Design: 25ns+(BWx4ns) for 10pF

Gain measurement by external charge injection

- This is needed to measure the capacitance for cal_inject.
- Gain ≡ #electrons / ADC count

@LBL w/ 35MHz (50MHz equivalent)

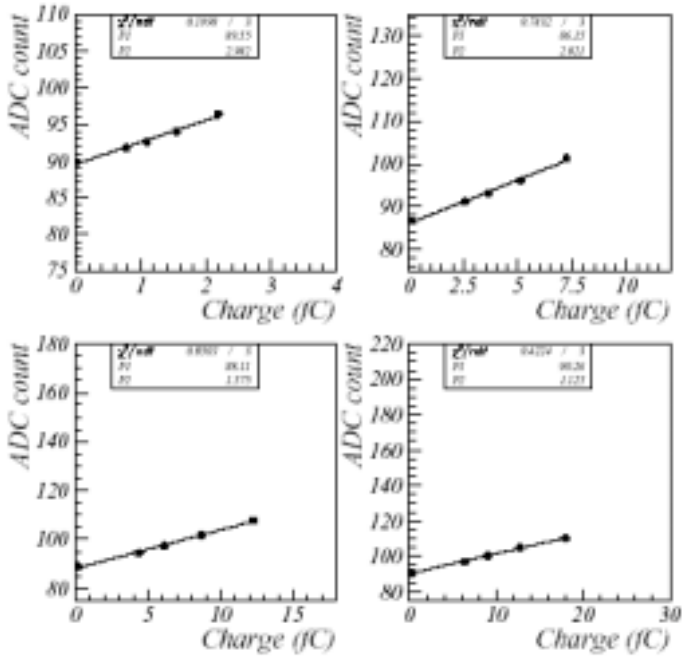
BW	10pF	33pF	56pF	82pF
0	1253(877)	1318(923)	1343(940)	1507(1055)
6	1337(936)	1441(1009)	1632(1142)	2071(1450)
15	1447(1013)	1739(1217)	2532(1772)	2930(2051)

@FNAL w/ 50MHz

BW	10pF	20pF	30pF	40pF
0	694	676	694	725
6	738	820	938	1042
15	898	1116	1250	1429

Gain -- continued

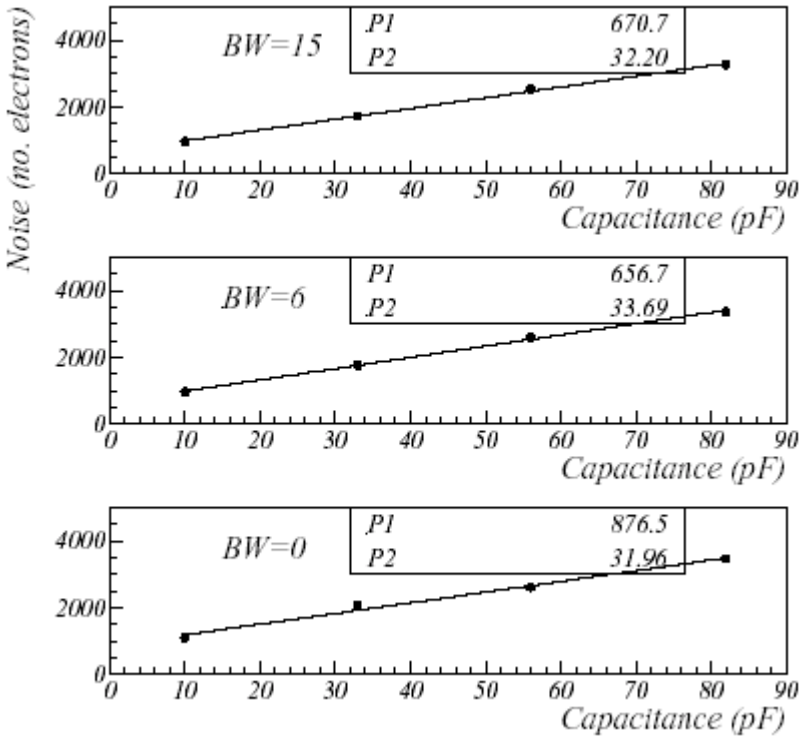
- Capacitance of cal_inject
  - ❑ Design: 25fF
  - ❑ Tom: 26fF
  - ❑ LBL: 24fF
  - ❑ FNAL: 29fF



- Measurement error? (LBL has more statistics and more data points compared to FNAL.)
- Pedestal dependence on the time interval between comp_reset and ramp_reset (= actually the time when the comparator fires). FNAL measurement is sensitive to this.

Noise (defined as RMS of pedestal distribution)

@LBL



For fixed BW setting (=15)

➔ rise time not fixed

	@LBL	Tom's frontend
10pF	992	794
20pF	1315	1034
30pF	1637	1434

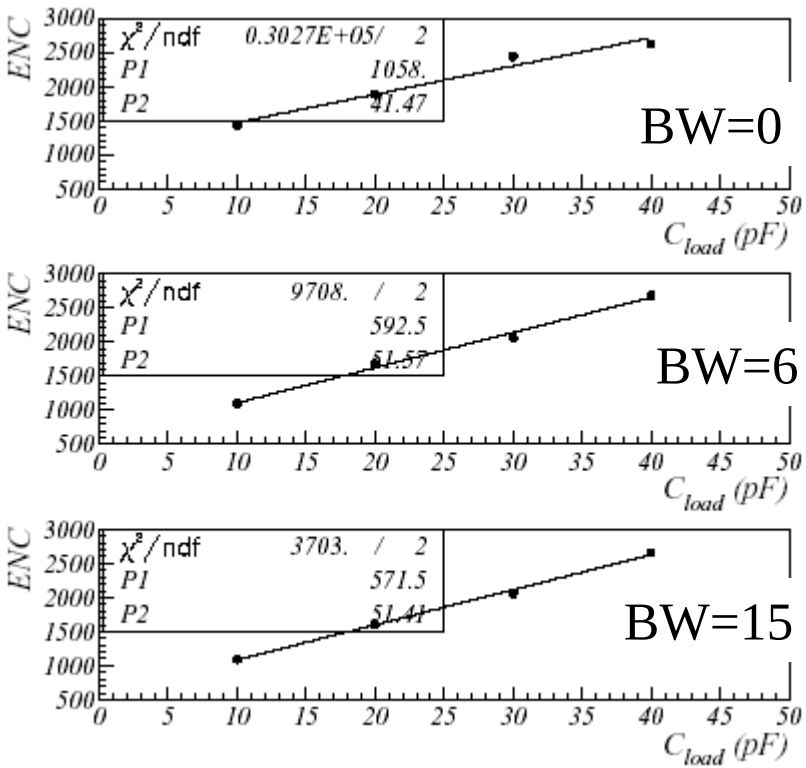
🡐 (200~300 electrons) of common mode noise? (Note this is <0.2ADC counts)

cf. For fixed rise time (69ns) by Tom: ENC ≅ 300 + 41C

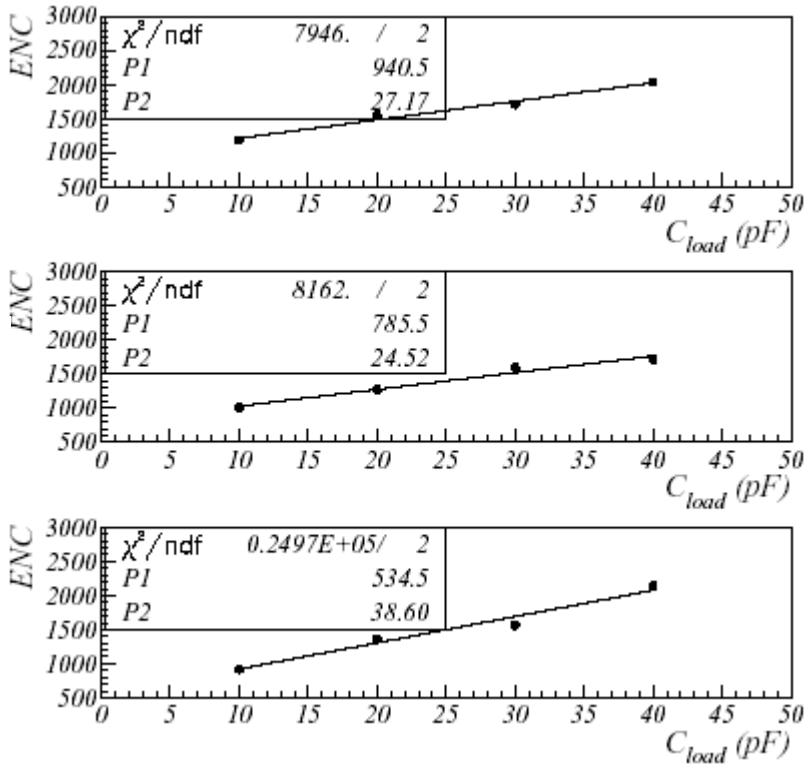
(2025e^- @40pF)

Noise – most recent measurement @FNAL

Total noise



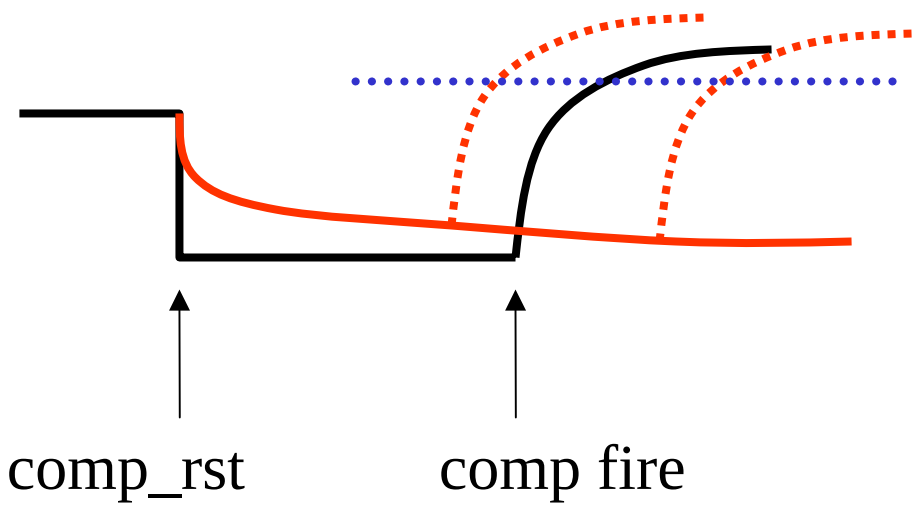
Differential noise



- The differential noise is close to the LBL's total noise.
- Existence of additional noise. (this changes the slope rather than the offset. Why???)

Comparator issue

Signal in the output buffer (Recall Len's good explanation at the collaboration meeting):

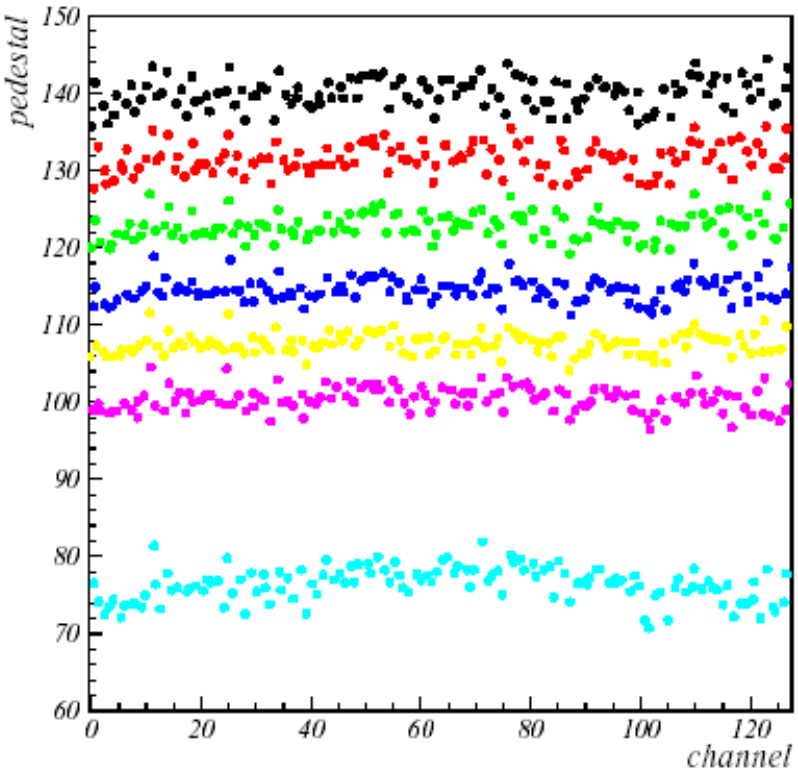


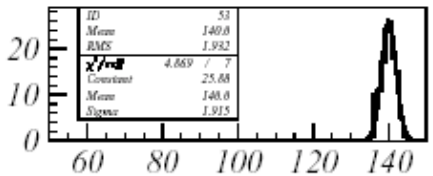
➔Internal delay depends on the time interval between comp_rst and when the comparator fires.

➔Pedestal should depend on this time interval.

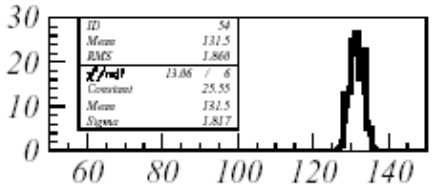
➔Expect pedestal increase for larger interval.

Observation 0

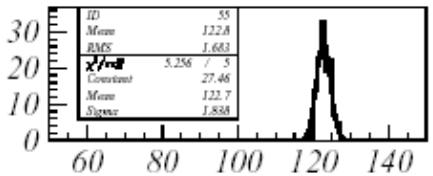




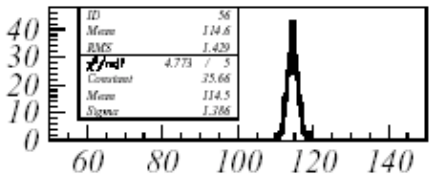
FE 5 Ped 3



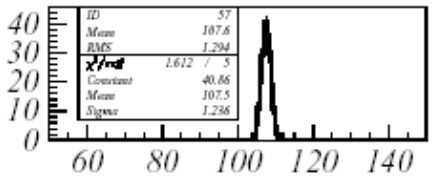
FE 5 Ped 4



FE 5 Ped 5



FE 5 Ped 6



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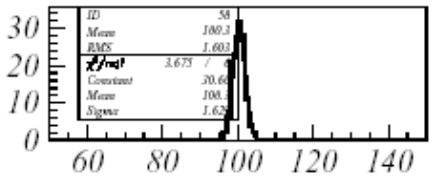
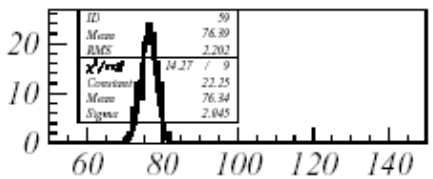
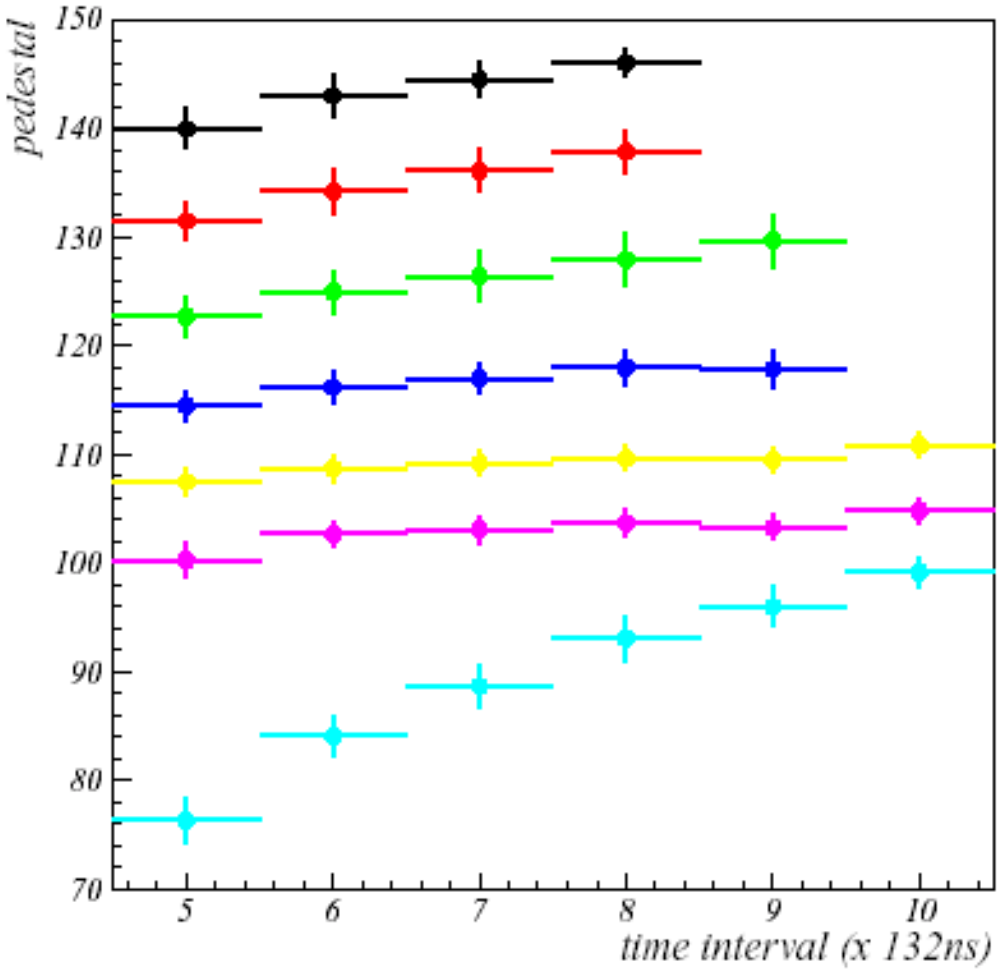


FE 5 Ped 8



FE 5 Ped 9

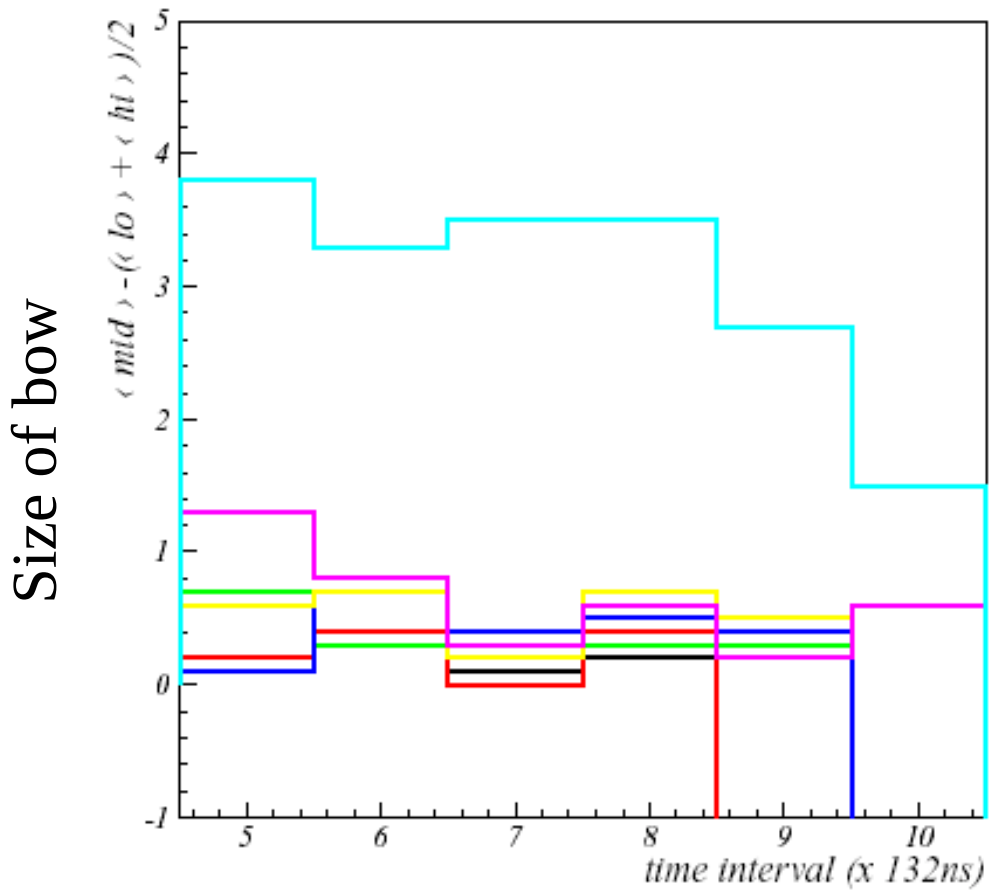
Observation 1



Between comp_rst and ramp_rst

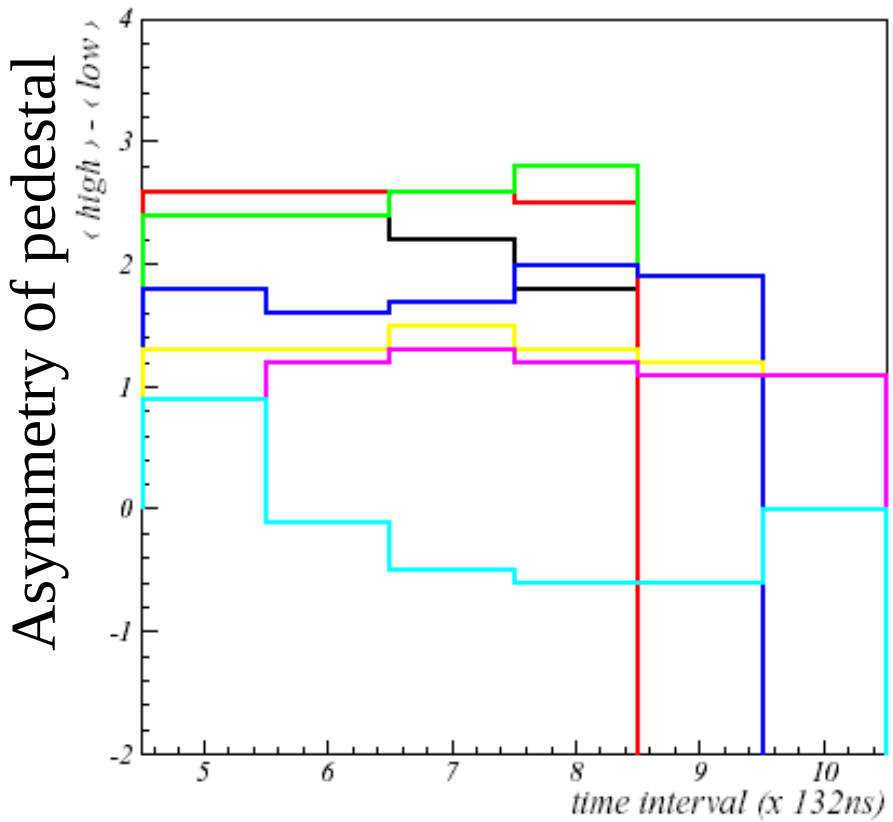
- The behavior is consistent with the expectation.
- NOTE!! What relevant here is the time interval between comp_rst and when comparator fires, i.e. longer is more stable.
- A setting with higher pedestal value has longer time interval internally. ⇐ the dependence is less.

Observation 2



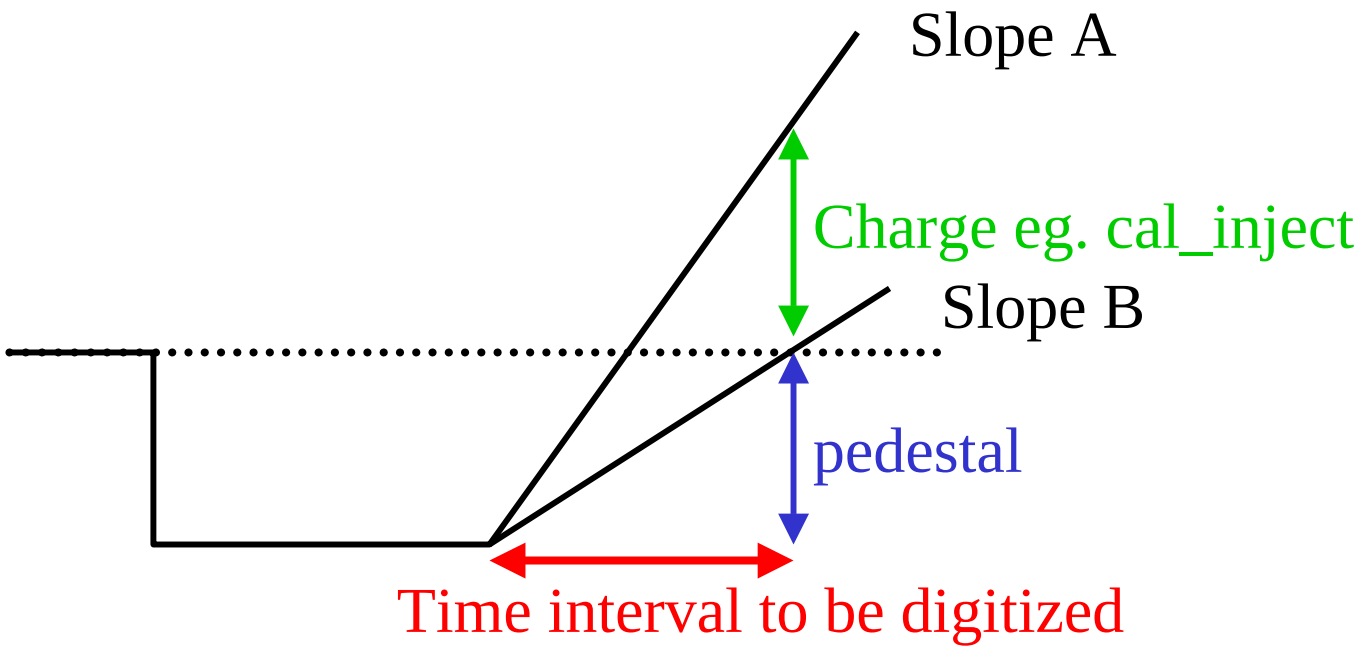
- The bow disappears after the long time interval. (= after the comparator reaches the saturation point, or stabilization.)

Observation 3



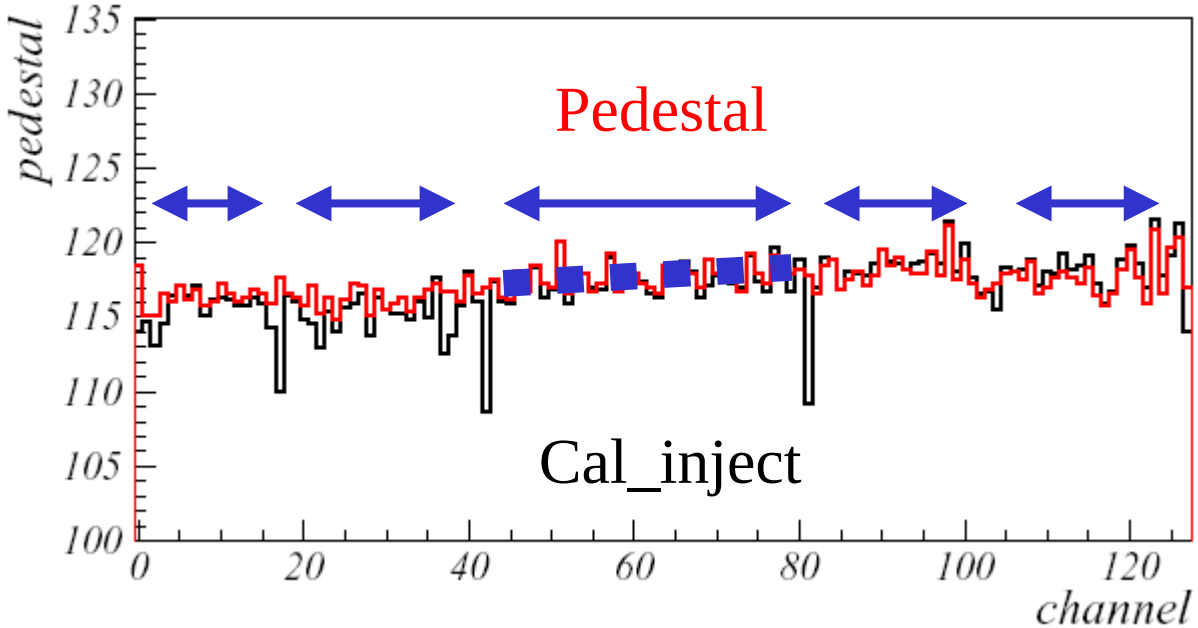
- No bow, but slope exists…
- All we know is that the comparator seems to cause the non-uniformity of pedestal. Tom says the comparator performance is not robust by its design, for example, the geographical effect.
- But we don't understand the geographical effect which really brings the non-uniformity.

No dependence on the input to ADC?



- Adjust the injection charge so that ADC counts with slope A is the same as the pedestal with slope B.
- When slope A = 2(slope B), for example, the non-uniformity should be as twice as slope B, if the non-uniformity comes from the input to ADC. (assuming the cal_inject is uniform across the channel.)

Channel to channel variation



Slope in each region

	1st	2nd	3rd	4th	5th
ped	0.046	0.028	0.027	0.039	0.057
cal	0.048	0.027	0.028	0.011	0.066

- The shape is consistent each other both visually and numerically.

➔ No effect from the input.

Summary & Plan

- Check list going through most of the specification. But not all of them. ➔ Do we add more?
- The most are within the specification except for:
  - Pedestal non-uniformity across channels.
  - D0 operation in ADC setup (latching PRD1).
  - Pipeline cell dependence of pedestal.
- The pedestal non-uniformity (across channels) seems to be caused by the comparator. Not fully understood, but redesign is necessary in any case. ➔ Testing the other things may be a good strategy.
  - Wafer level testing.
  - Temperature dependence.

  My personal plan
  - Irradiation.
  - Yield and long term effect.