Design of an upgraded D0 Silicon Micro Strip Tracker for Run 2b

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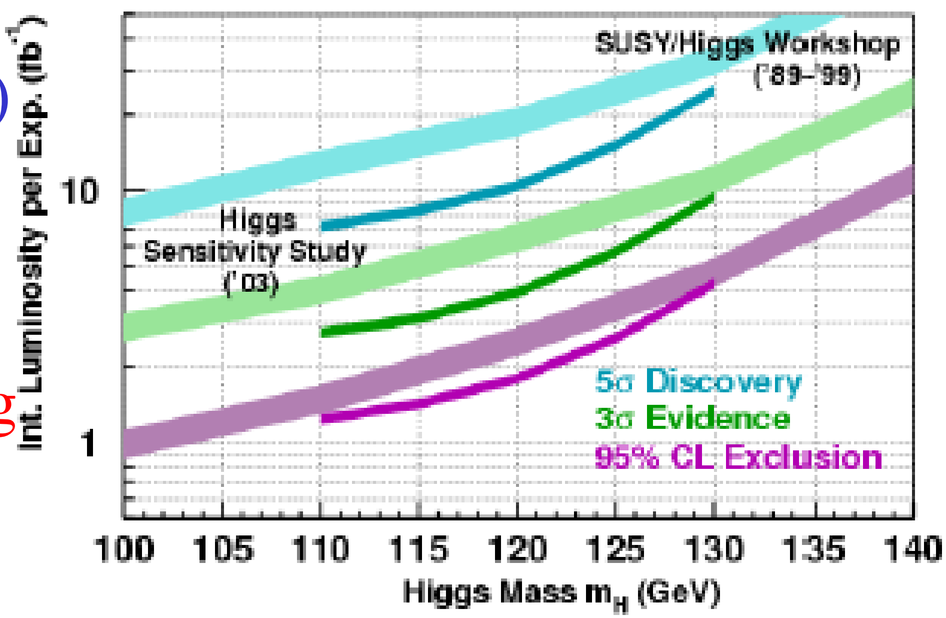
for D0 run 2b silicon tracker group

Outline

- Physics motivation
  - General and the innermost layer (Layer 0)
- Design
  - Design considerations
  - Mechanical design
  - Readout schematics
- Prototype of each element
  - Sensor
  - Readout chip and hybrid
  - Readout module and stave
- Layer 0
  - Analog flex cable
  - Grounding scheme
- Summary and Conclusion

Physics Motivation

- Design for integrated luminosity of 15 fb^{-1}
  - Present silicon tracker is expected to withstand 2–4 fb^{-1}
- Increase in instantaneous luminosity benefits from enhanced pattern recognition capability → more layers of silicon
- B tagging by means of the longer life time
  → better impact parameter resolution
  → measurement at position close to the decay point
  $\sigma \sim \sigma_{meas}(1+R_{in}/R_{out})$
  (0.11 for run2b, 0.27 for run2a)
- Higgs sensitivity better than old estimates ← one of the largest contributions comes from the improved b-tagging thanks to the addition of a layer at smaller radius



Design Consideration

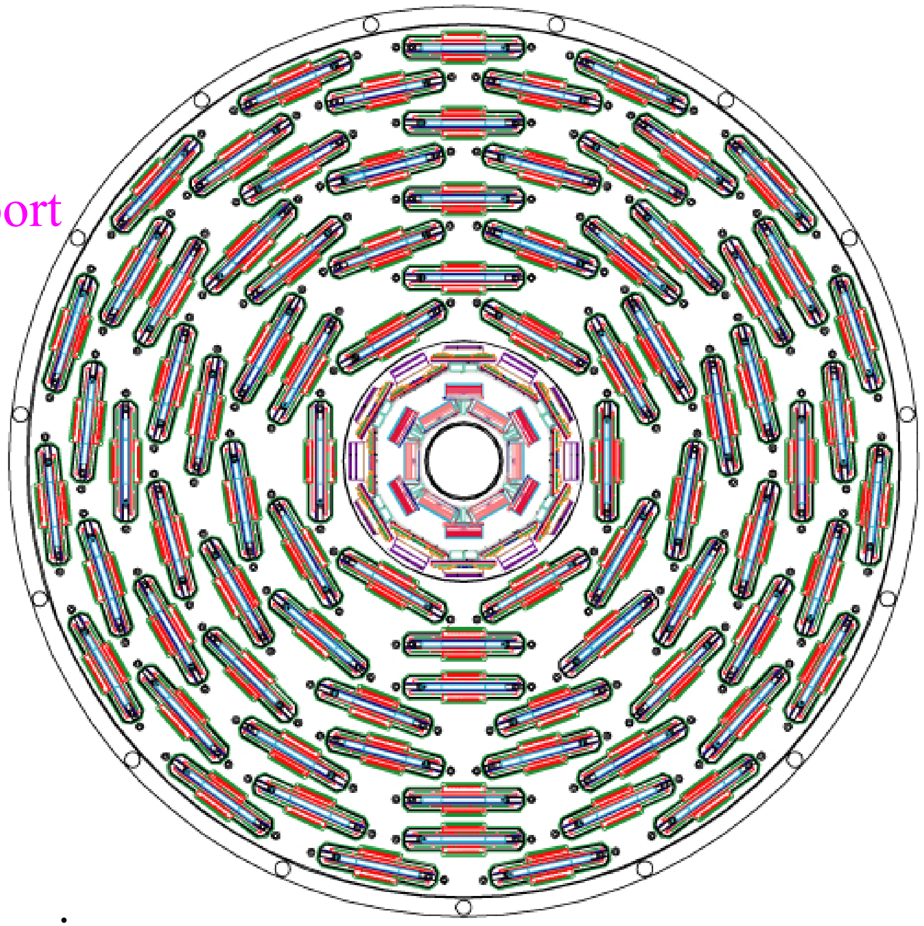
- Design Principles
  - Improved performance for high p_T physics
  - Minimize cost and risk
  - Full replacement, minimum shutdown time
- Benchmarks
  - $\sigma(p_T)/P_T \sim 3\%$ at 10 GeV/c
  - $\sigma(d_0) < 15\ \mu m$ for $p_T > 10$ GeV/c
  - b-tagging efficiency of ~ 65% per jet

→ Consequence

- ➢ Adding innermost layer for improved resolution
- ➢ Adding outer layer for pattern recognition enhancement (#layers = 4 for present detector → 6 for Run 2b)
- ➢ Modular design minimizes the number of different element types to reduce fabrication complexity
- ➢ Single sided sensors only

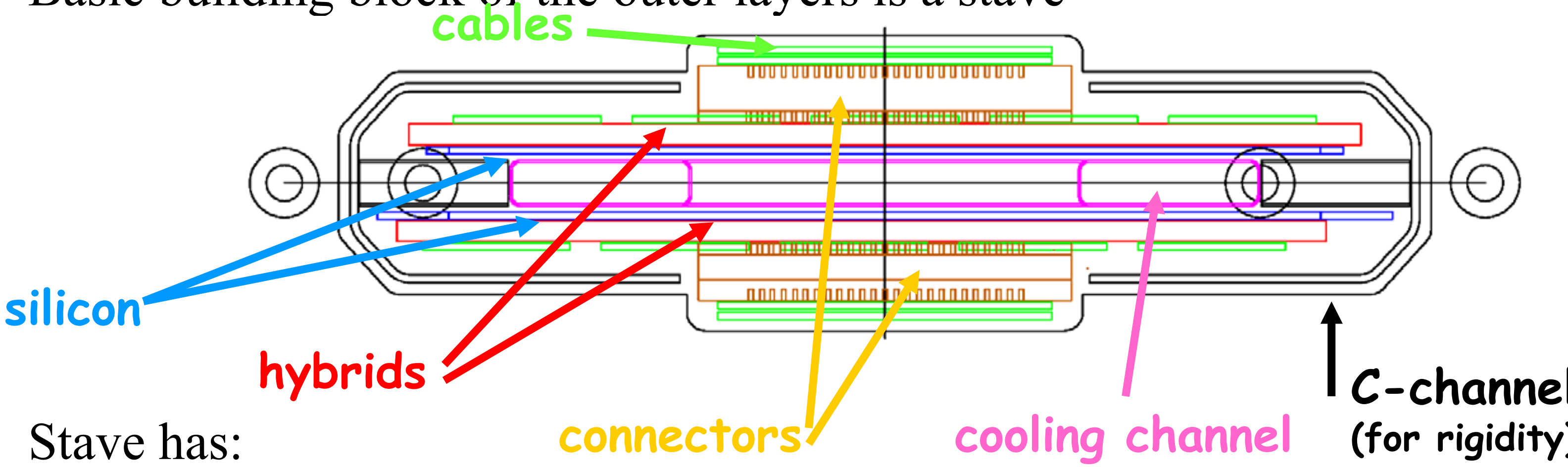
Design Overview

- Six layer silicon tracker, divided in two radial groups
  - Inner layers: Layers 0 and 1
    - 18mm < R < 39mm
    - Axial readout only
    - Mounted on integrated support
    - Assembled into one unit
  - Outer layers: Layers 2-5
    - 53mm < R < 164 mm
    - Axial and stereo readout
    - Stave support structure
  - All sensors intermediate strips
- Employ single sided silicon only, 3 sensor types, axial strips
  - 2-chip wide for Layer 0
  - 3-chip wide for Layer 1
  - 5-chip wide for Layers 2-5
- No element supported from the beampipe



Outer Layers – Staves

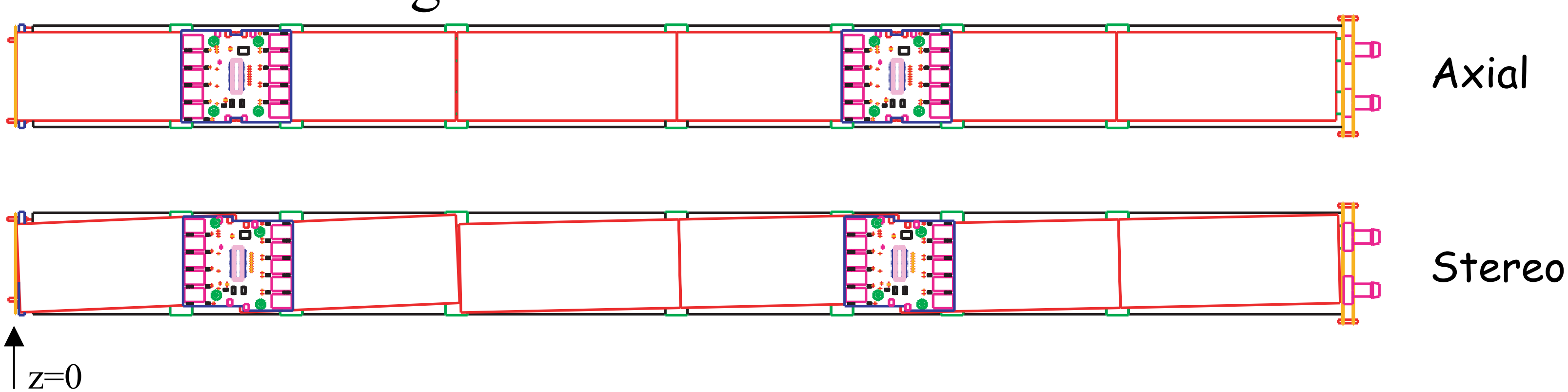
- Basic building block of the outer layers is a stave



- Stave has:
  - silicon sensors mounted on both sides of core
  - axial measurements while sensors on the opposite provide small angle measurements
    - stereo angle obtained by rotating the sensor
  - core with positioning and reference pins and PEEK cooling tubes
  - Total of 168 staves
  - C-shells at edge of stave provide stiffness
- Staves are positioned and supported in carbon fiber bulkheads at z = 0 and z = 605 mm.
  - Locating features on stave provide the alignment

Readout Module

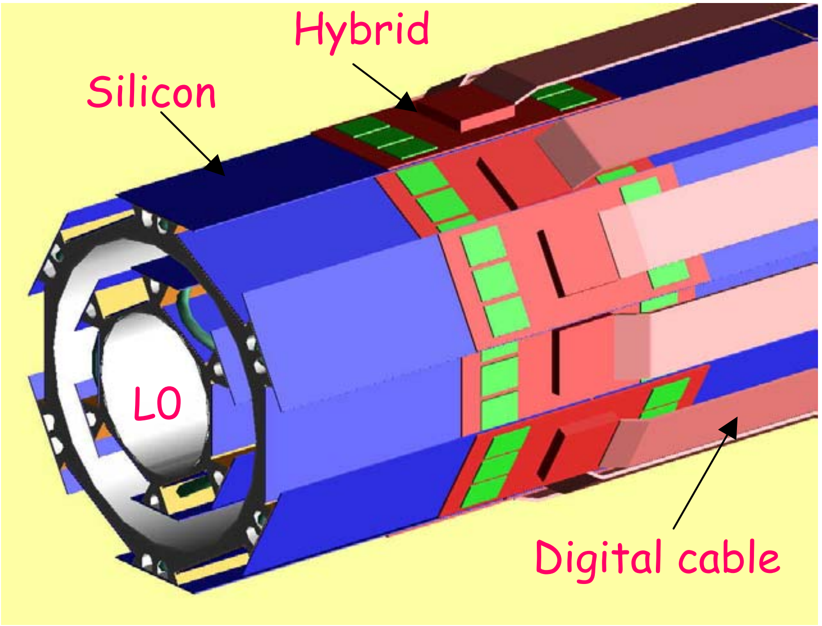
- Each stave has four readout modules
- Readout module length varies with z-position.
  - For all layers, the modules closest to z = 0 are 200 mm long
  - Those furthest from z = 0 are 400 mm long
- Four Readout module types
  - 10-10 (axial, stereo)
  - 20-20 (axial, stereo)
  - Ganged sensors will have traces aligned (sensors are 10cm long)
- Module configuration

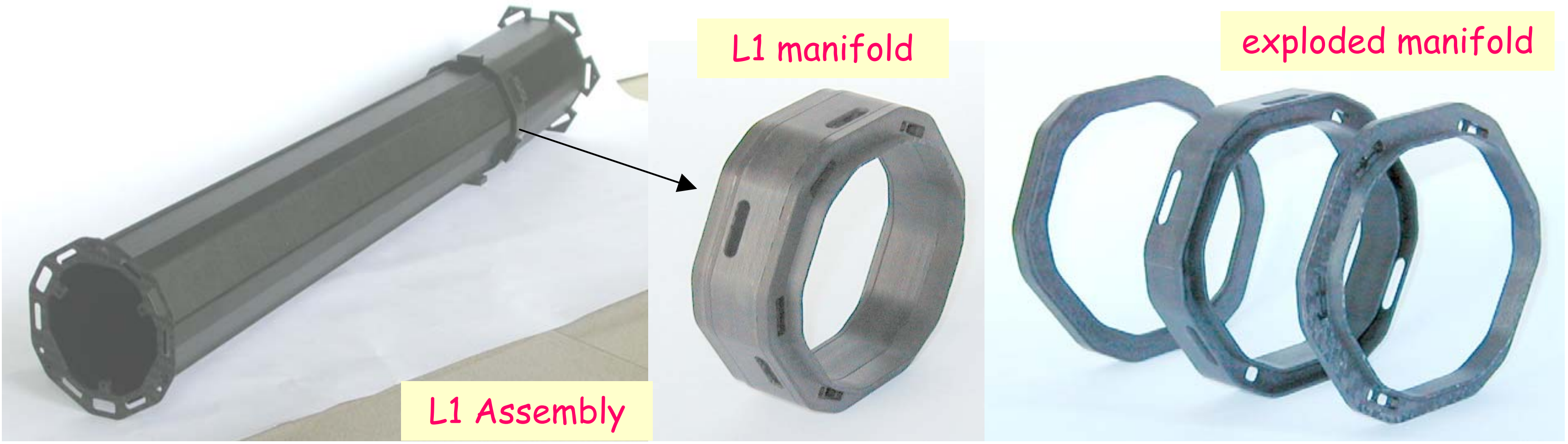


- Each readout module serviced by double-ended hybrid
  - Each hybrid has two independent readout segments

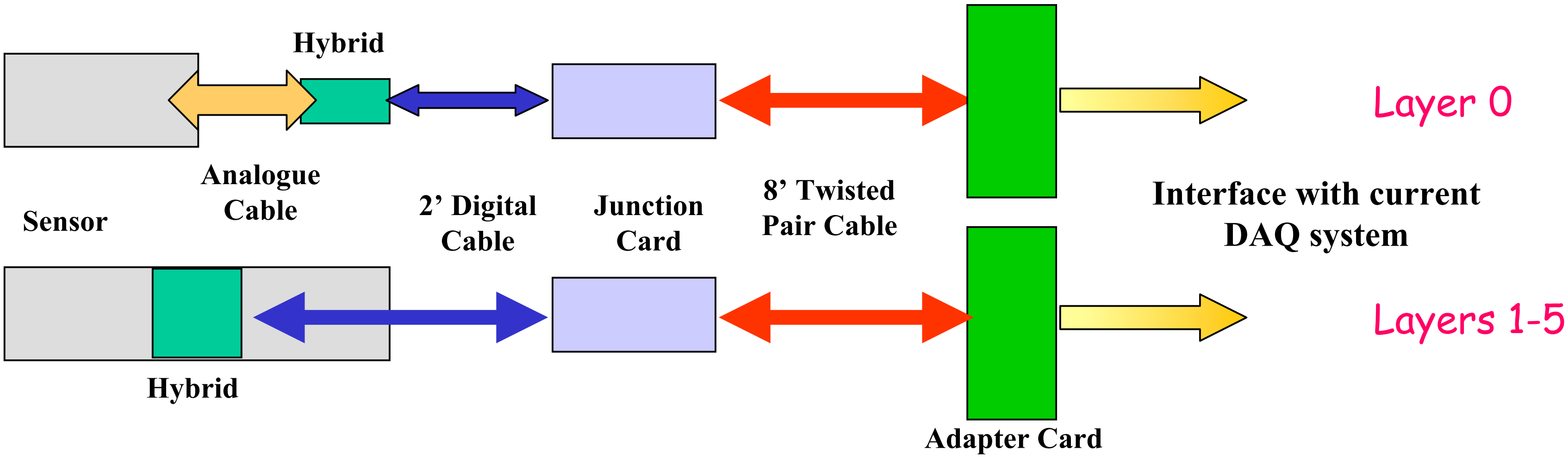
Layer 1 Support Structure

- Readout electronics mounted on the sensors:
  - Power dissipation of 0.5W/chip
  - Power dissipation of < 0.1 W/sensor after 15 fb^{-1}
- Pre-prototypes made of all L1 components
  - Inner tube and castellated structure
  - Cooling manifold components machined and connectors to cooling tubes
  - Connection and support membranes





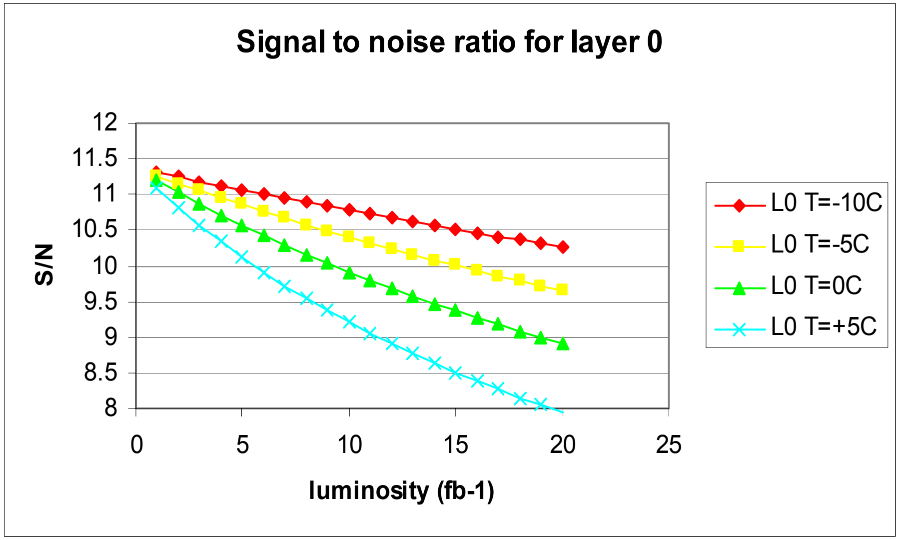
Readout Schematics



- Layers 1-5: Hybrids mounted on silicon
  - Hybrid →digital cable → junction card → twisted pair → Adapter Card
- Layer 0: Hybrids mounted off-board
  - Analogue Cable → Hybrid → digital cable → junction card → twisted pair → Adapter Card
- Readout with SVX4 chips operated in SVX2 mode

Sensor – Radiation Damage Issues

- Parameters for detector
  - V_{depl} after irradiation
  - Signal to Noise ratio
- Requirements
  - S/N ratio > 10 after 15 fb^{-1}
  - $V_{depl} \ll V_{break}$ to allow for over-depletion for full charge collection

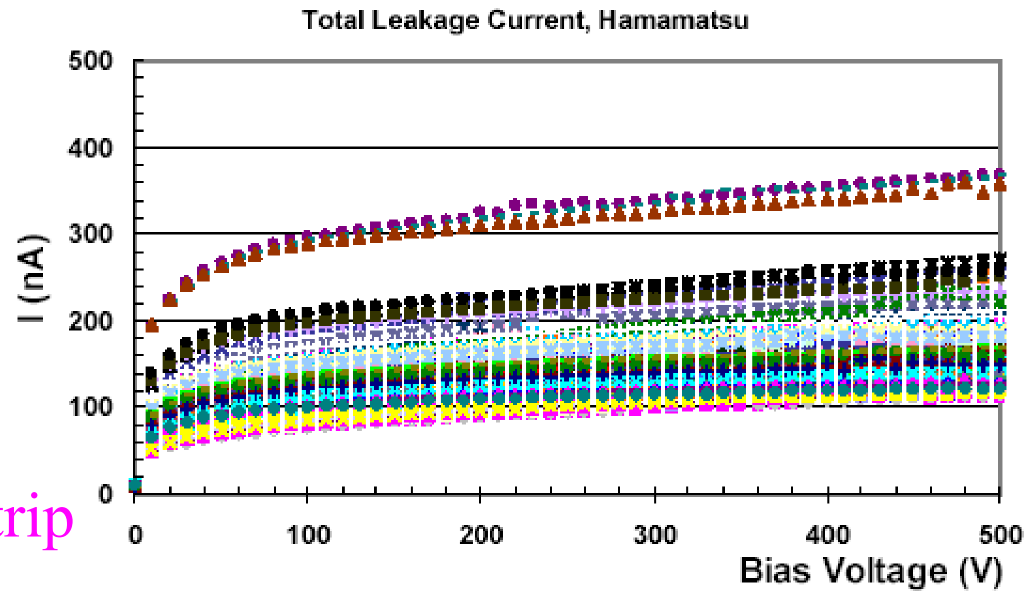


Layer	T_silicon (C)
Layer 0	-10
Layer 1	-5
Layer 2	0
Layer 3	>0
Layer 4	>0
Layer 5	>0

- More detail about the radiation issue by F. Lehner

Layer 2–5 Sensors

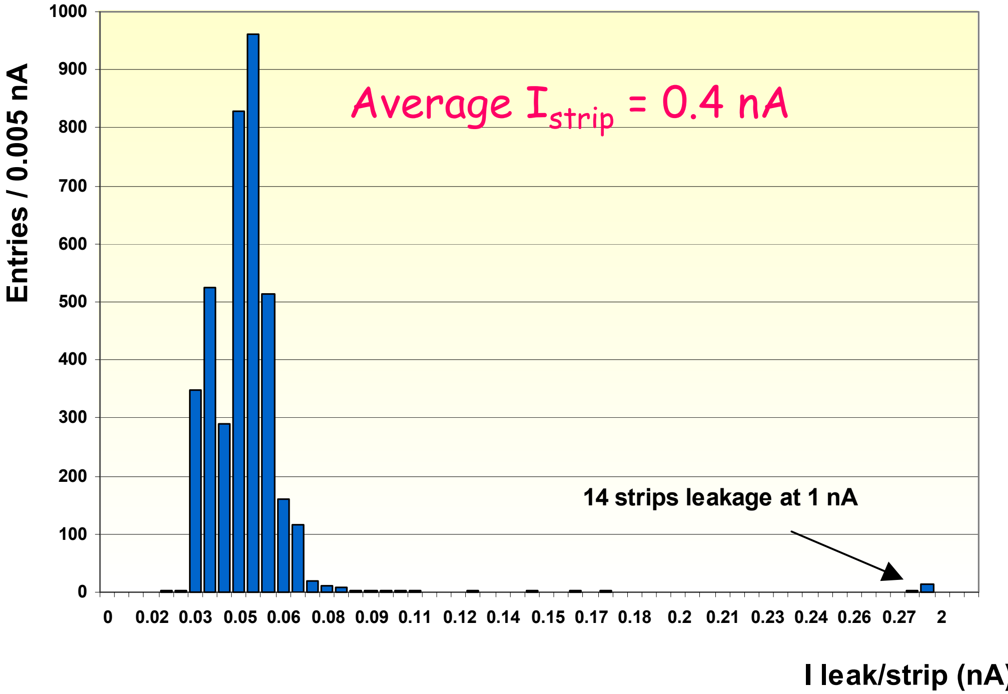
- 5-chip wide, 60μm pitch, intermediate strips, 40.34 × 100 mm cut dimension
- Order placed for 100 prototype sensors, May ’02; sensors shipped Nov. 29
- Hamamatsu’s internal QA program indicates sensors are of very high quality
  - Bulk tests
    - No single sensor exceeding leakage current of 400 nA
  - Strip tests
    - Only three sensors have a total of 8 strip defects



- Sensor production in progress: received 260, 270 more ready for shipment

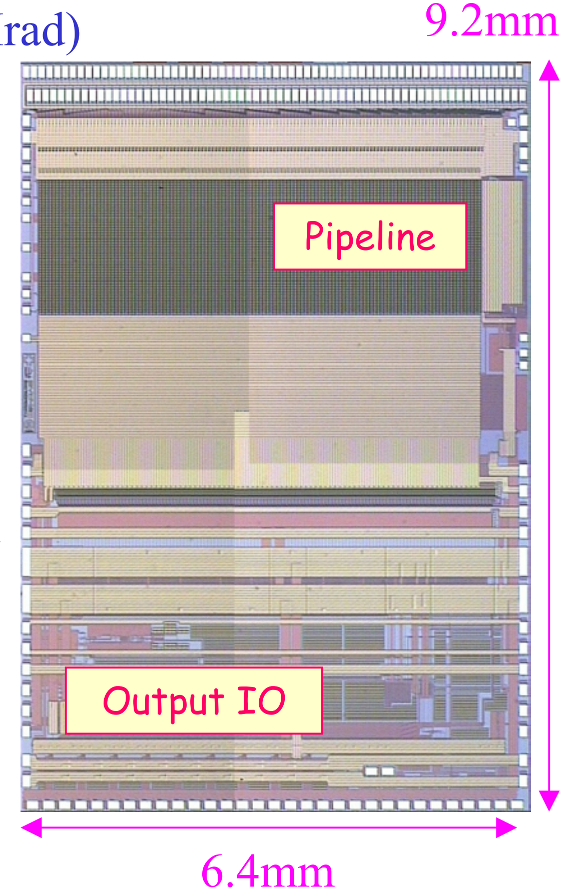
Layer 1 Sensors

- 3-chip wide, 58μm pitch, intermediate strips, 24.3 × 79.4 mm cut dimensions
- Order placed for 10 prototype sensors, April ’02; sensors shipped Sept. 21
- Hamamatsu’s internal QA program indicates sensors are of good quality
- strip leakage current for all 10 sensors at full depletion voltage
  - average strip current of 0.4 nA
  - 14 strips have a current of 1 nA
  - specification: $I_{strip} < 10$ nA



SVX4 Chip

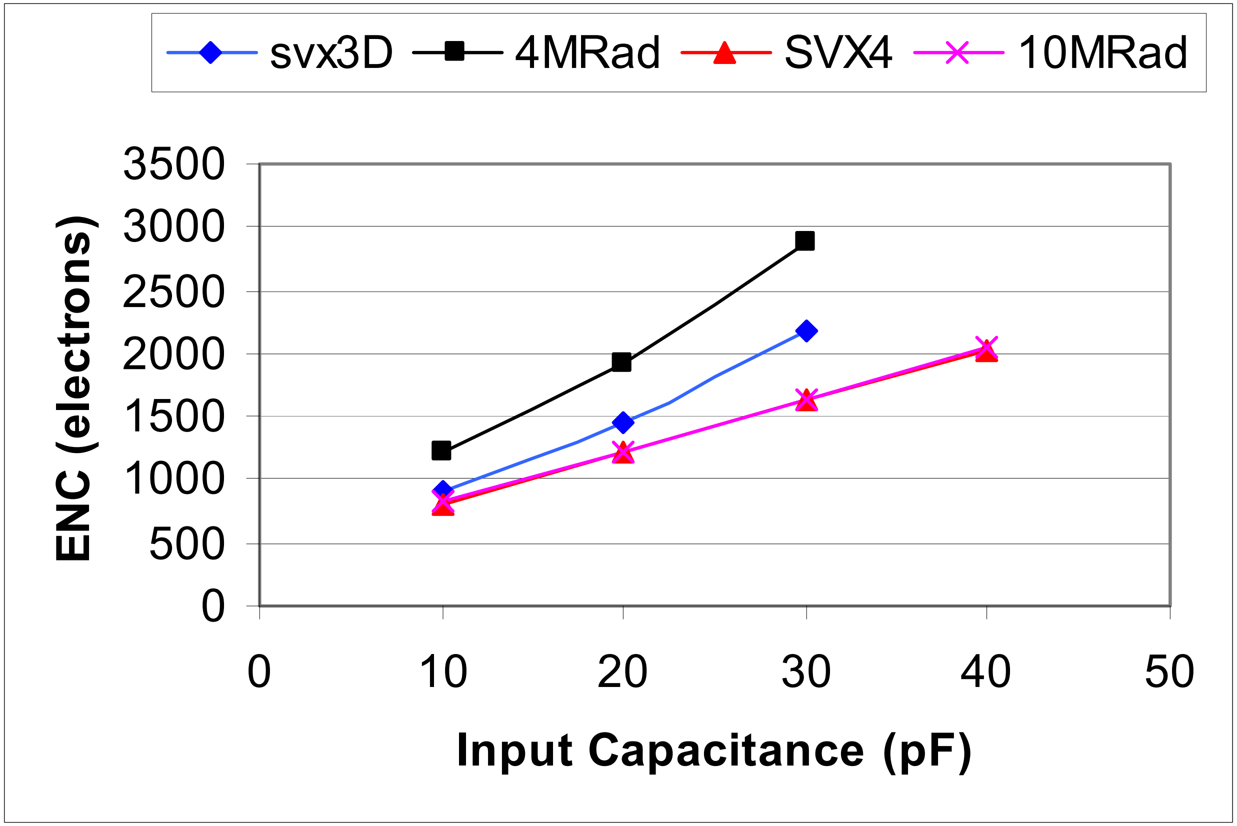
- DZero and CDF (Fermilab and LBL) developed new readout chip SVX4
  - Successor of SVX2 and SVX3 chip
  - 0.25 μm technology, intrinsically rad-hard (>30Mrad)
  - 128 inputs and 46+1 pipeline cells
  - 8-bit ADC with sparsification
  - 53 MHz readout, 106 MHz digitization
  - Programmable test pattern for calibrations, ADC ramp, preamp bandwidth
  - Pinhole clamping
  - 2.5 V, power measured to 0.3 W/chip
- First version ready in June 2002
  - Fully functional chip, used for hybrid/module/full readout chain prototyping
- Second version ready in May 2003
  - Improved ADC design – good uniformity of pedestals
  - First test results all positive → accepted as a final version: 24 wafers ready
  - Ready for production → signoff completed



SVX4 Chip – continued

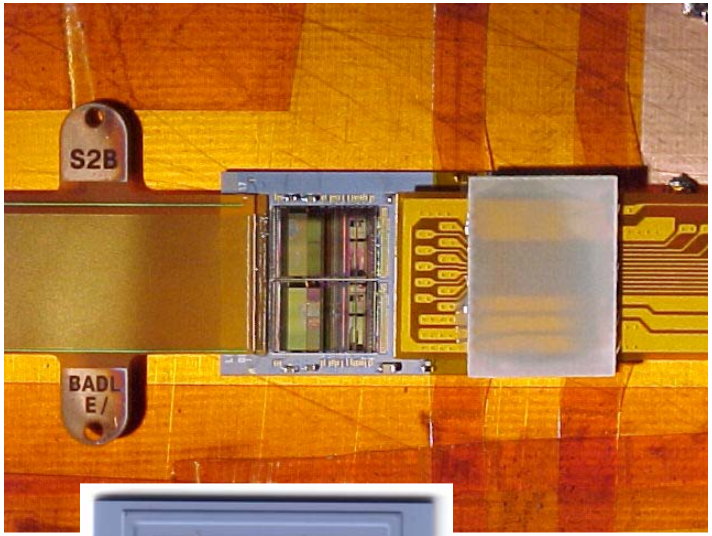
- Noise
  - For fixed rise time (69ns): ENC ≅ 300 + 41C (2025e⁻ @40pF)
  - Spec. < 2000e for 40pF @ 100ns rise time.

  ➔ very good noise performance.



Hybrid

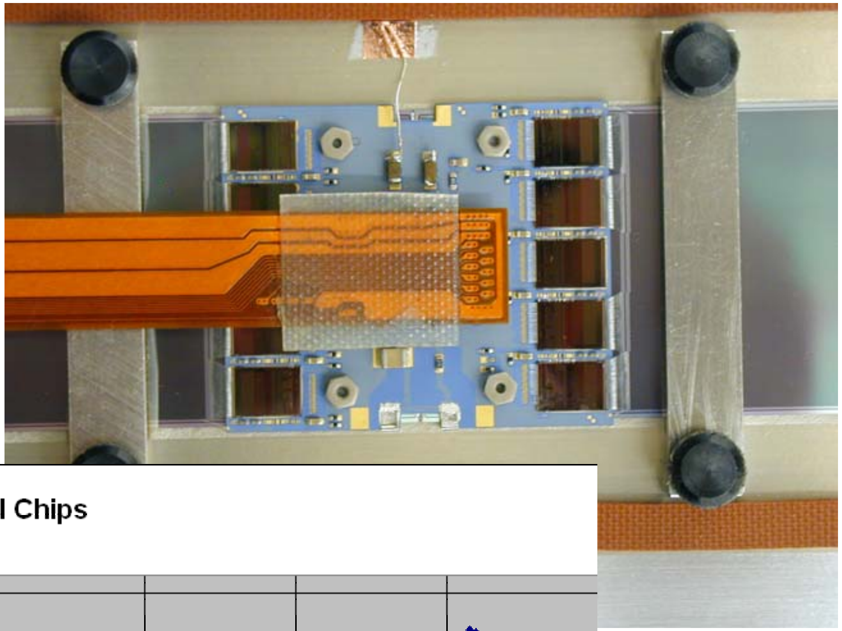
- Four types of hybrids
  - Layer 0 : 2 chips
  - Layer 1 : 6 chips, double-ended
  - Layers 2-5 : 10 chips, double-ended (Axial & Stereo)
- Thick film printing technology
  - 380 μm Beryllia ceramic substrate
  - Six metal layers
  - Min via size 200 μm
  - Total thickness 950 μm
- On-board AVX connector
- Prototypes of all hybrids fabricated, stuffed and tested
  - Layer 1 and Layer 2-5 hybrids are glued to silicon
    - Have back side pattern to control glue runout

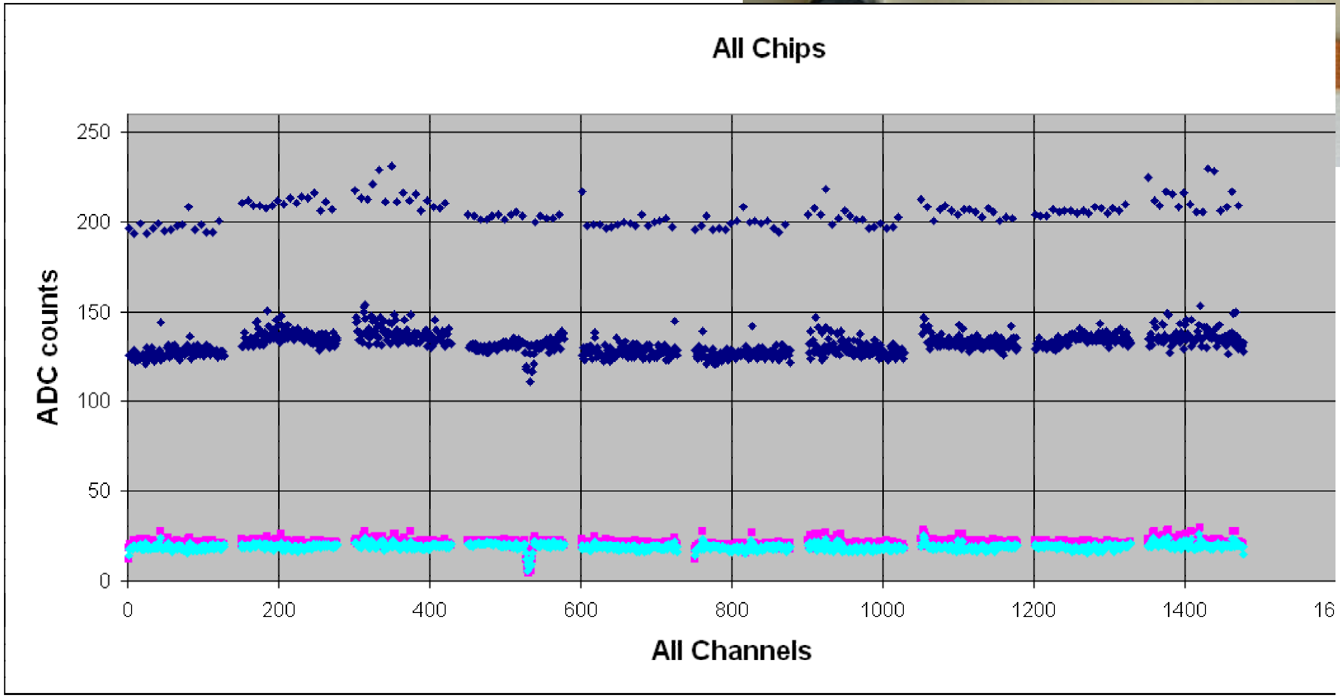


6 chips backplane

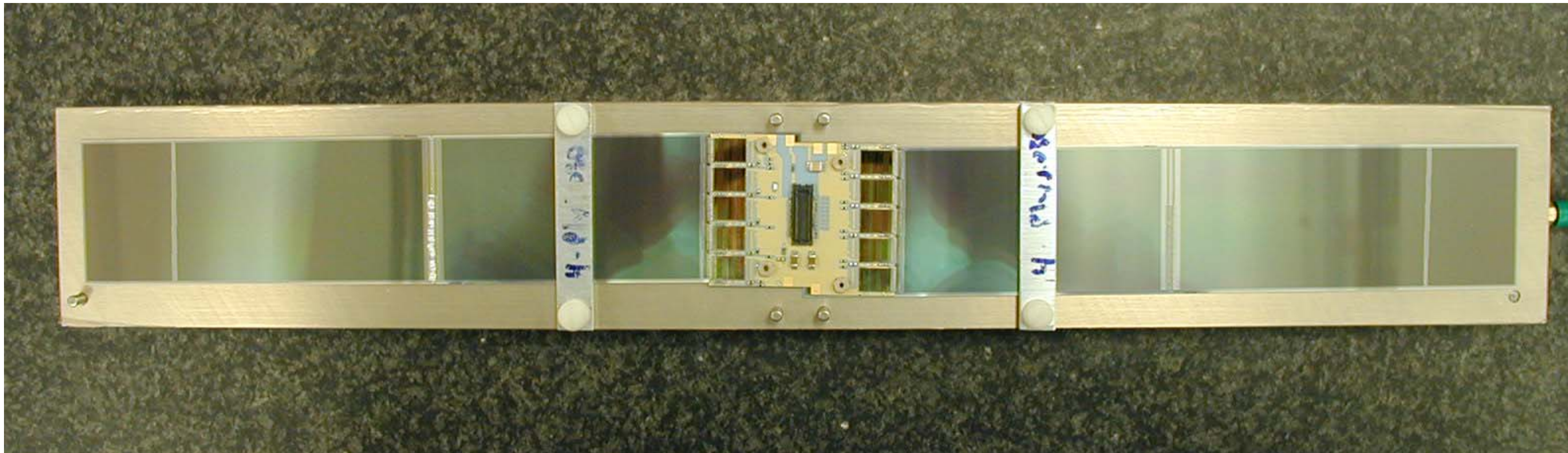
Prototype Readout Module

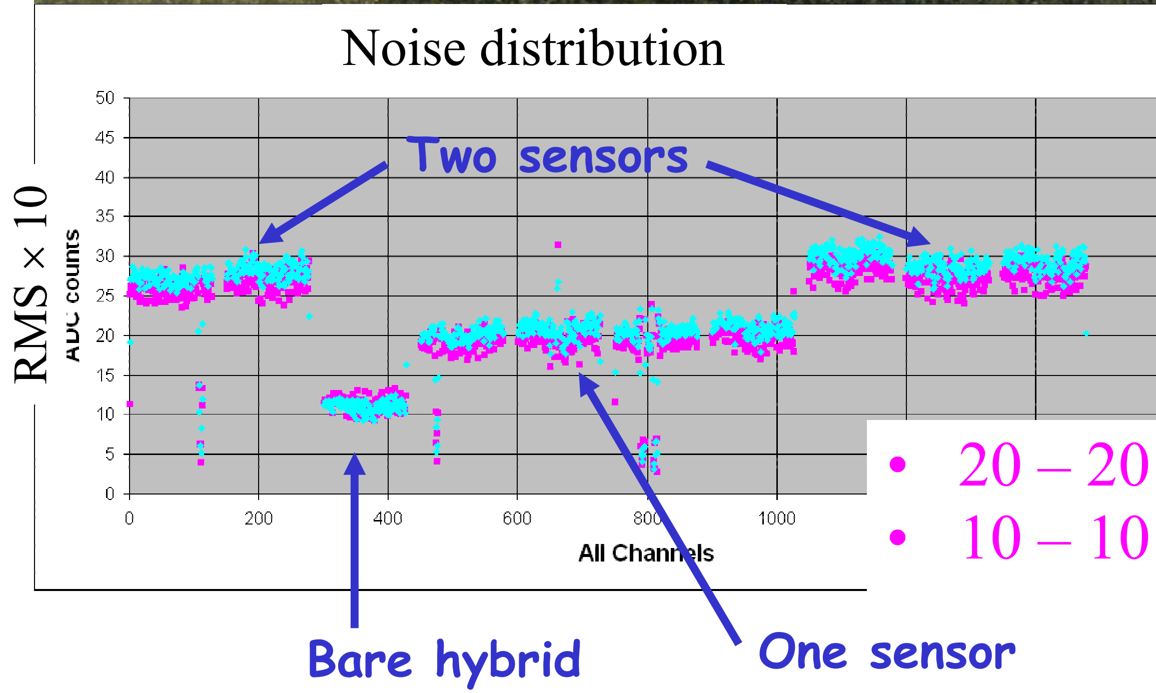
- Prototypes built of all six different readout modules
  - Some fixtures are adequate and will be used for production
  - Fixtures for Layer 1 modules similar to 10-10 modules





Prototype Readout Module – cont'd

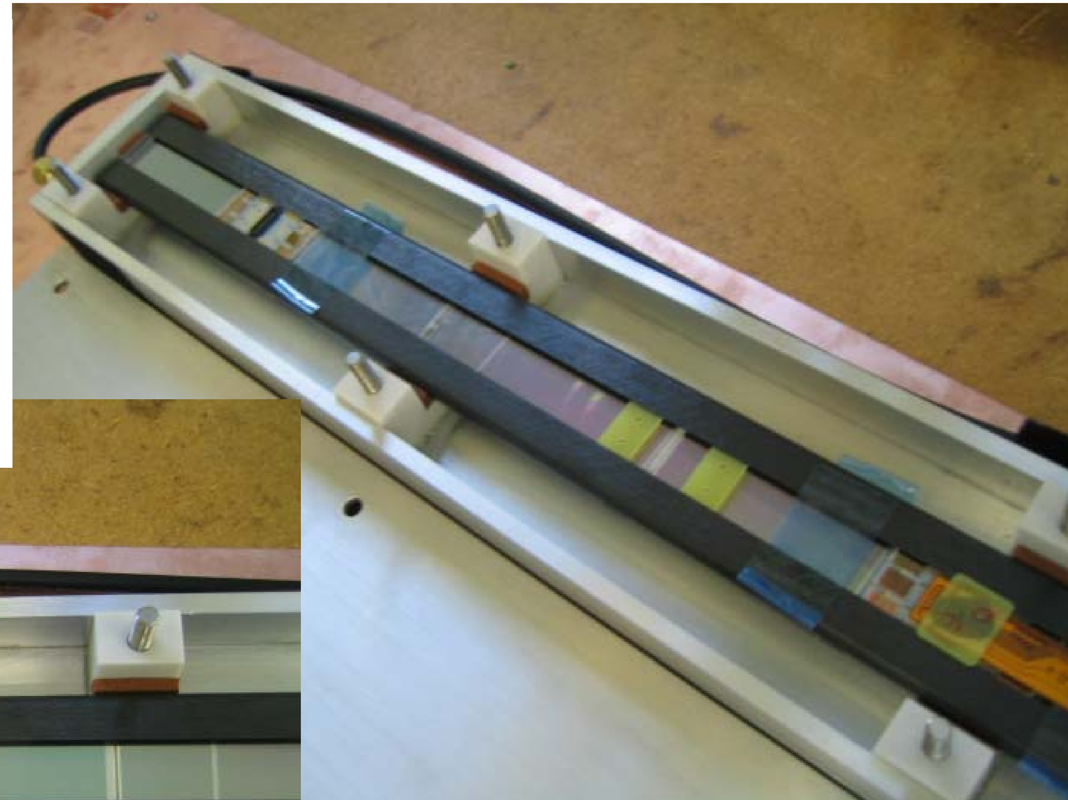


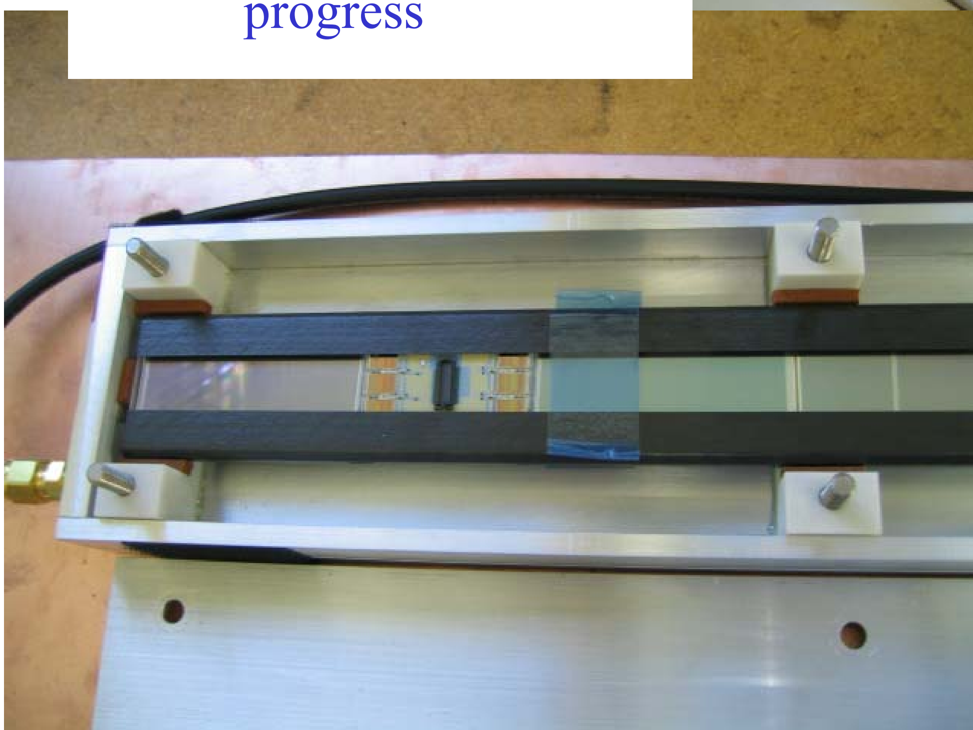


- 20 – 20 modules: S/N = 11
- 10 – 10 modules: S/N = 16

Prototype Stave

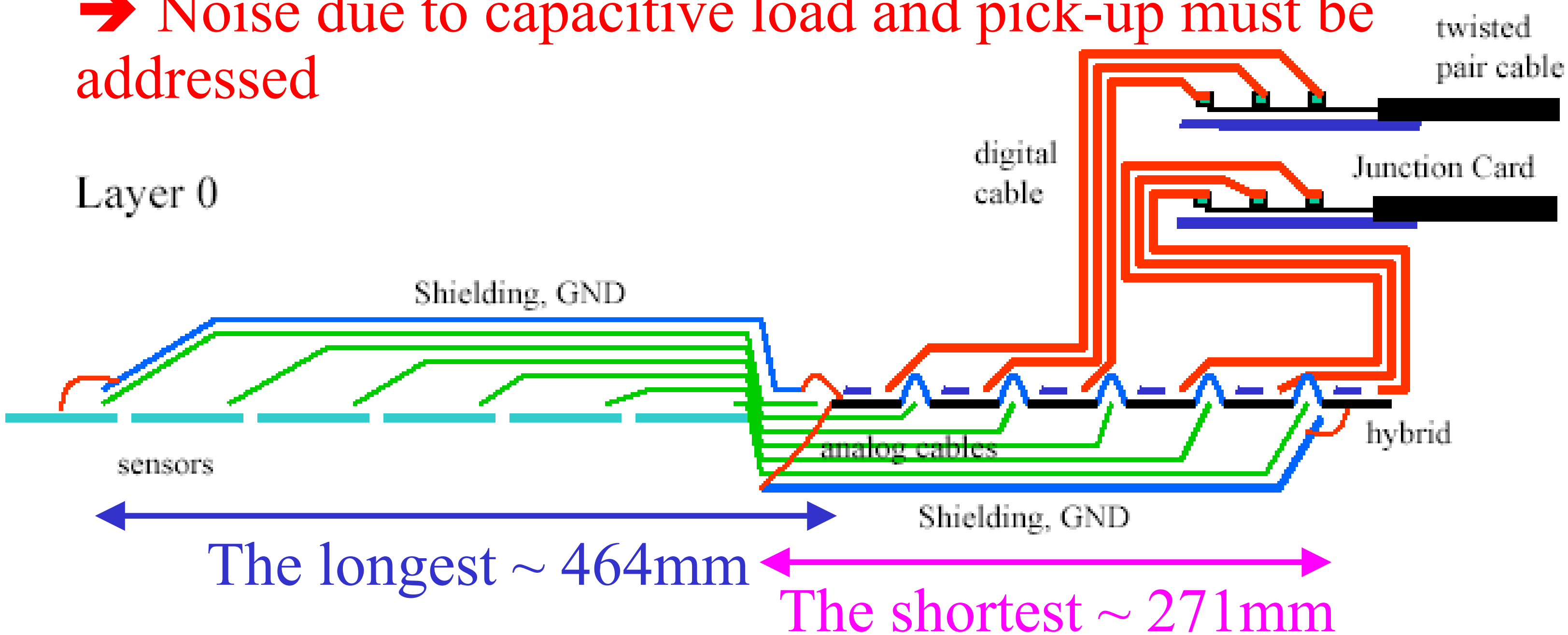
- Both mechanical and electrical ones
- Electrical stave with cooling
  - Readout testing in progress





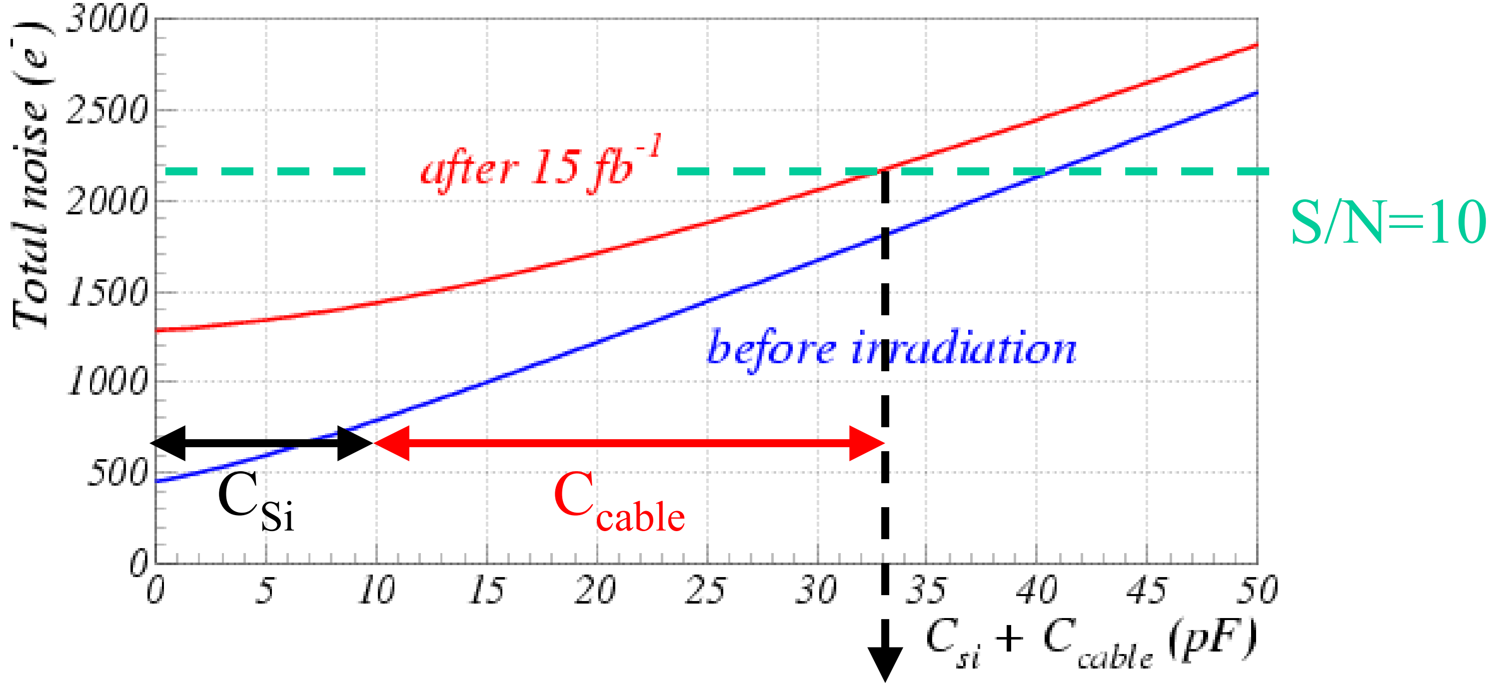
Concept of Layer 0

- SVX4 chip cannot sit on the sensors because of the cooling and space constraints
  ➔ Signal must be read out from the sensor to the chip
  Also bias voltage and its return must be provided
  ➔ Low mass analog flex cable
  ➔ Noise due to capacitive load and pick-up must be addressed



Analog Cable Constraints

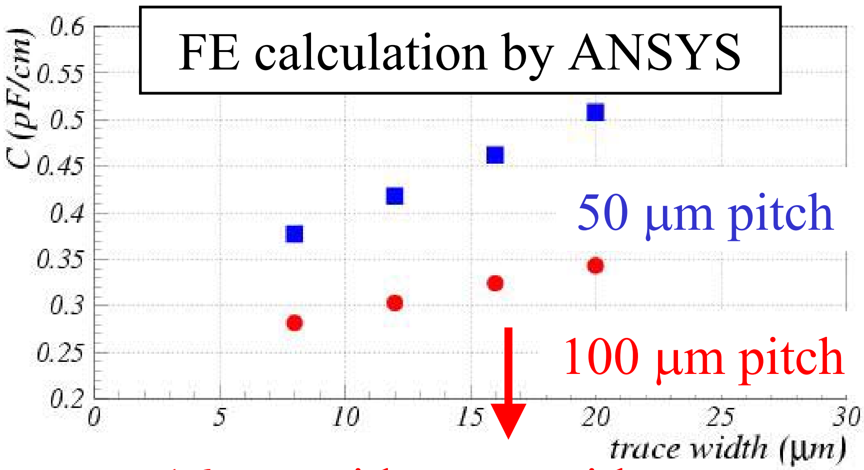
Total noise estimates VS total capacitance ($C_{si} + C_{cable}$)



S/N=10 after 15fb^{-1} ➔ C_{cable} < 23pF for 46.4cm long cable

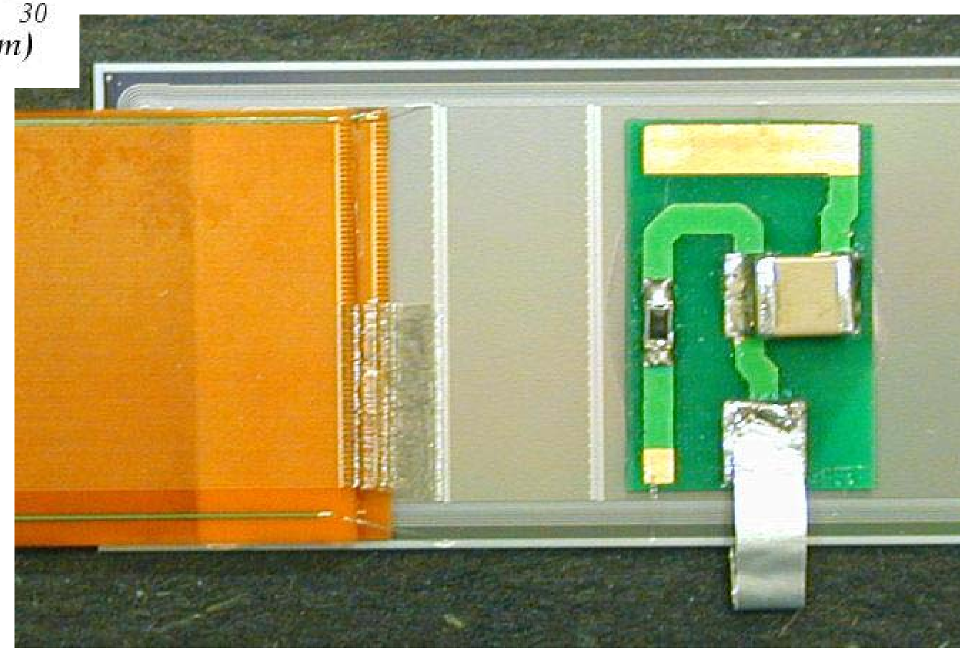
➔ C_{cable} < 0.5pF/cm

Analog Cable Design



16 μm wide trace with ~100μm pitch satisfies the requirement of <0.5pF/cm

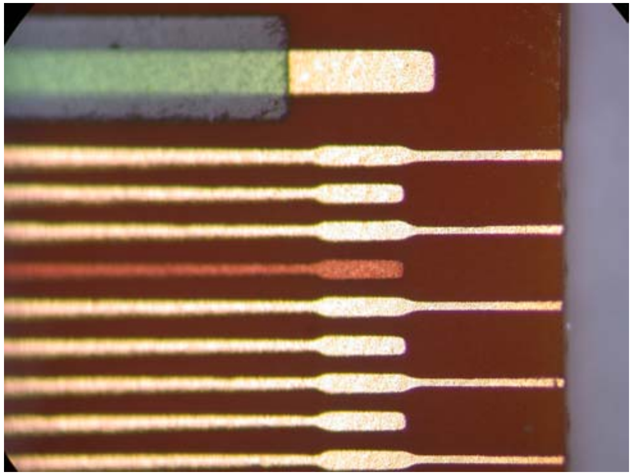
- 91μm trace pitch
- 16μm trace width
- 50 μm thick polyimide (Kapton type) substrate
- Two cables laminated at the edges with 45μm offset



- Use technically simpler solution which maintains low capacitance.

Prototype Analog Cable by Dyconex

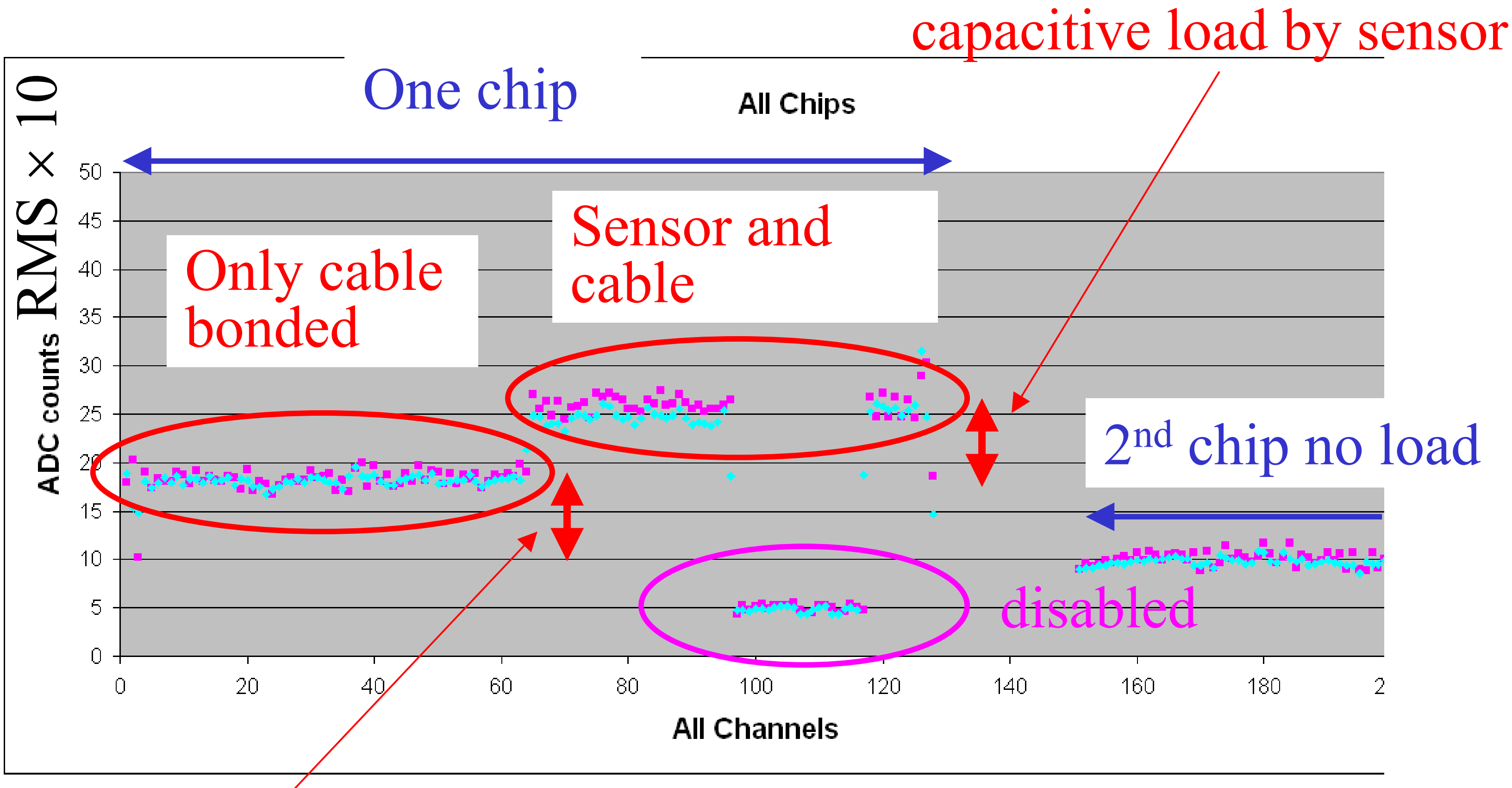
- All cables are Ni-Au plated (~1.2μm) over the full length, solder mask only on HV+GND traces
- Visual inspection of cables:
  - look for unplated (copper) pads



- The latest prototype: no single opens out of 40 cables
  - 129 traces→one open is allowed
  - Trace width on cables: 9-12μm for 3rd ~19μm for 4th prototypes

Capacitance (one to neighbors) ~ 0.35pF/cm measured by LCR meter.

Capacitance Estimates from Noise



capacitive load by cable (0.8ADC~600e)

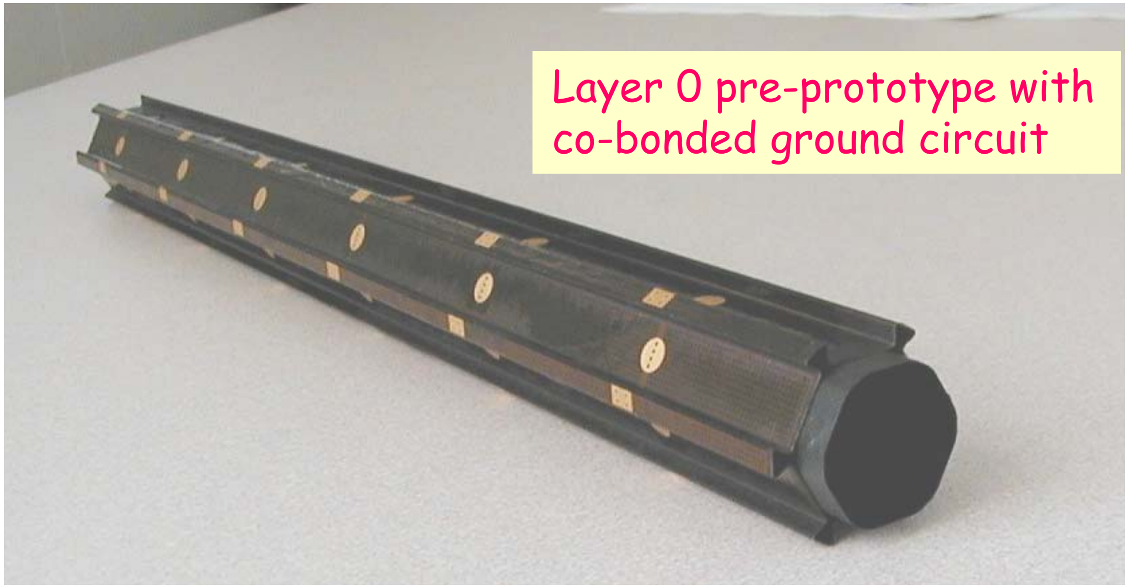
SVX4 ENC: const+41C ➔ 600e indicates C = 15pF for ~45cm

Layer 0 Support Structure

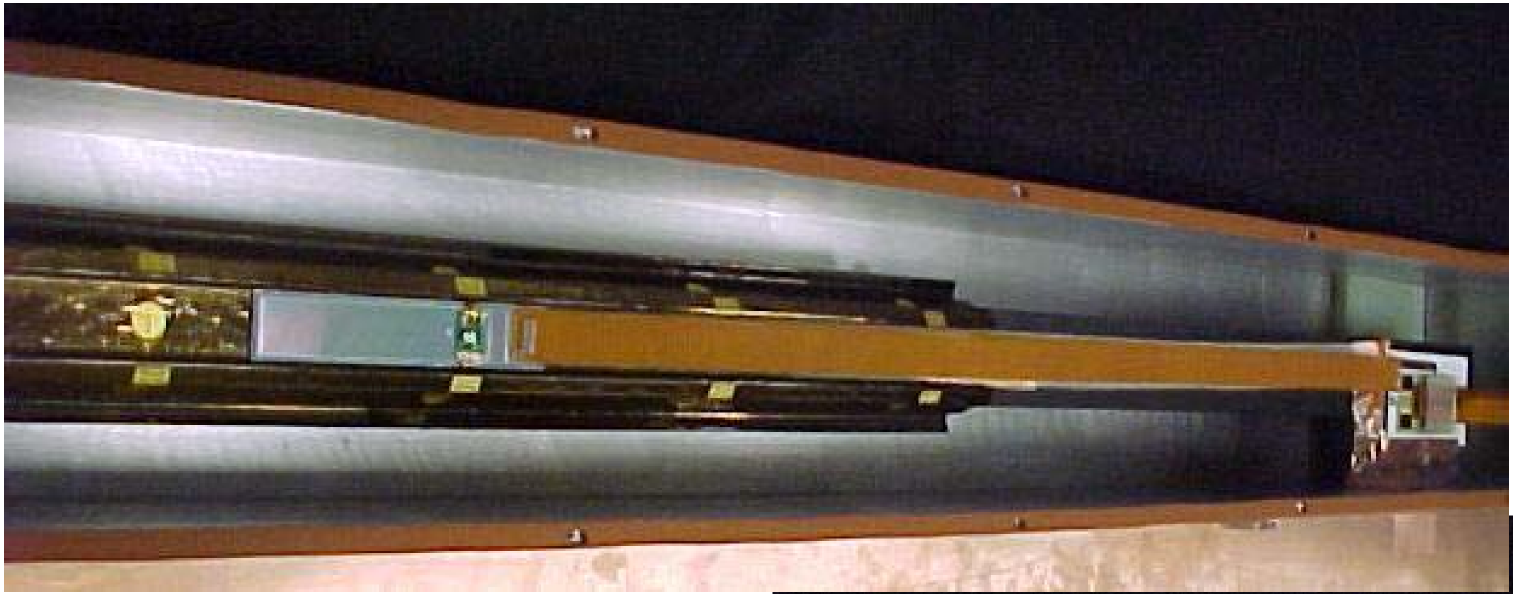
- Inner shell, carbon fiber
  - 12-sided
  - 4 layers [0,90]s lay-up
- Cured thickness = 0.22 ± 0.01 mm

- Outer shell, carbon fiber
  - 12-fold crenellated geometry
  - 6 layers [0,20,-20]s lay-up
- Cured thickness = 0.31 ± 0.01 mm

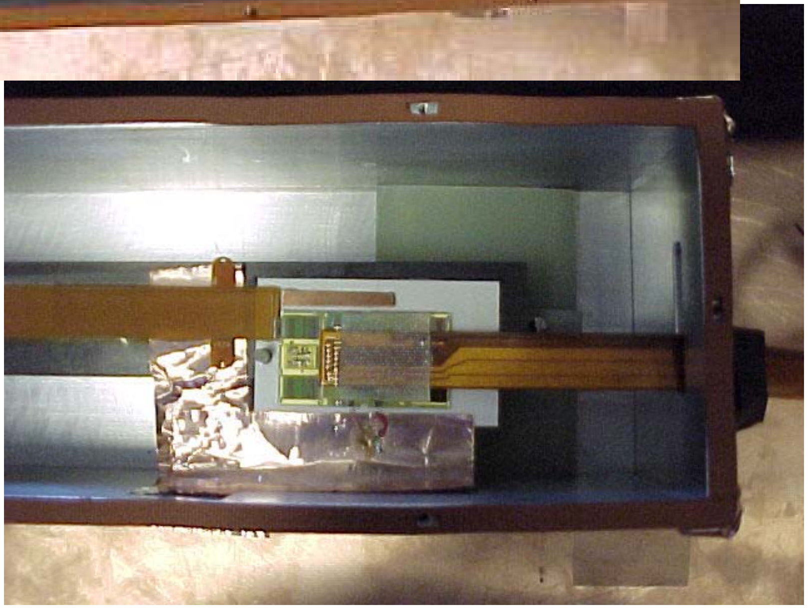
- All FEA analyses, mechanical and thermal, completed
- All L0 and L1 prototype fabrication tooling completed and evaluated
  - deflection ~5 μm under applied load of 400 grams (distributed 200gr nominal load)
- Certified fabrication procedures for L0 prototype production by making pre-prototypes



Layer 0 Prototype Module on Structure

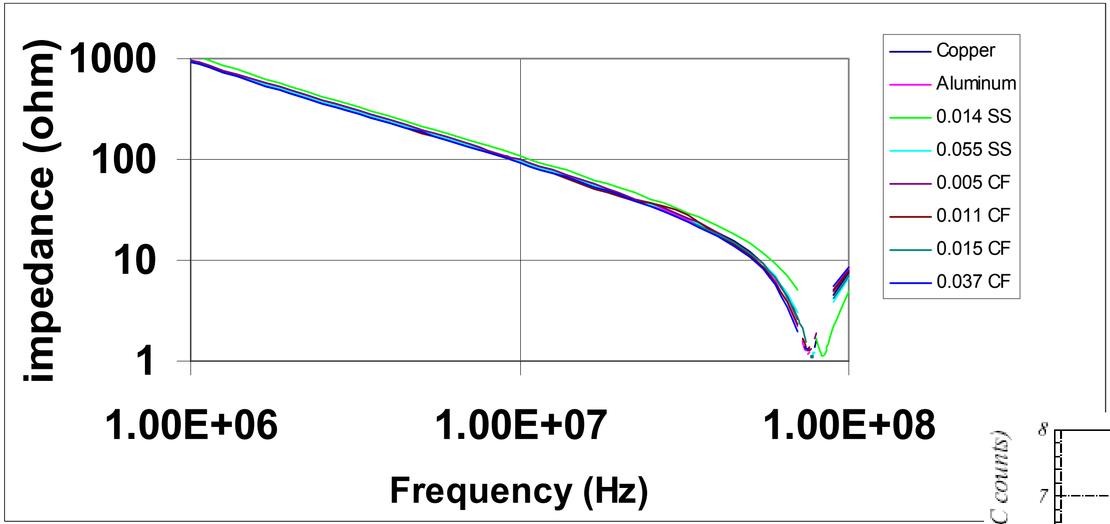


- Sensor directly mounted on carbon fiber structure
- Hybrid also on the carbon fiber structure in real detector (not in the photograph at right)



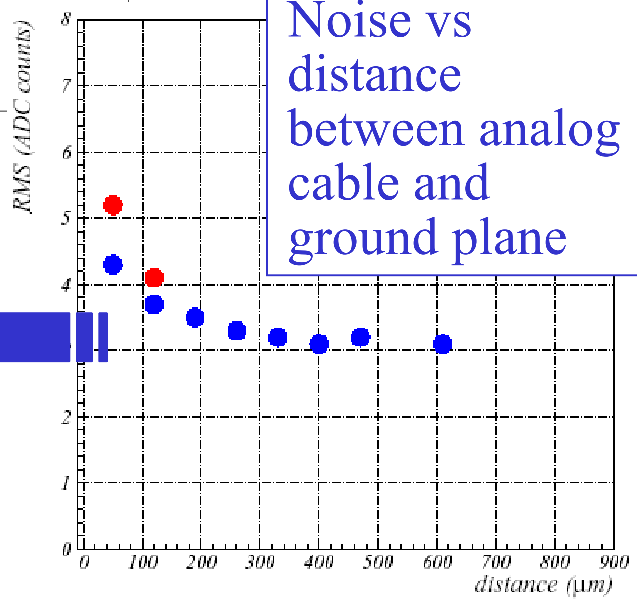
Application of Carbon Fiber

- Carbon fiber has high conductivity



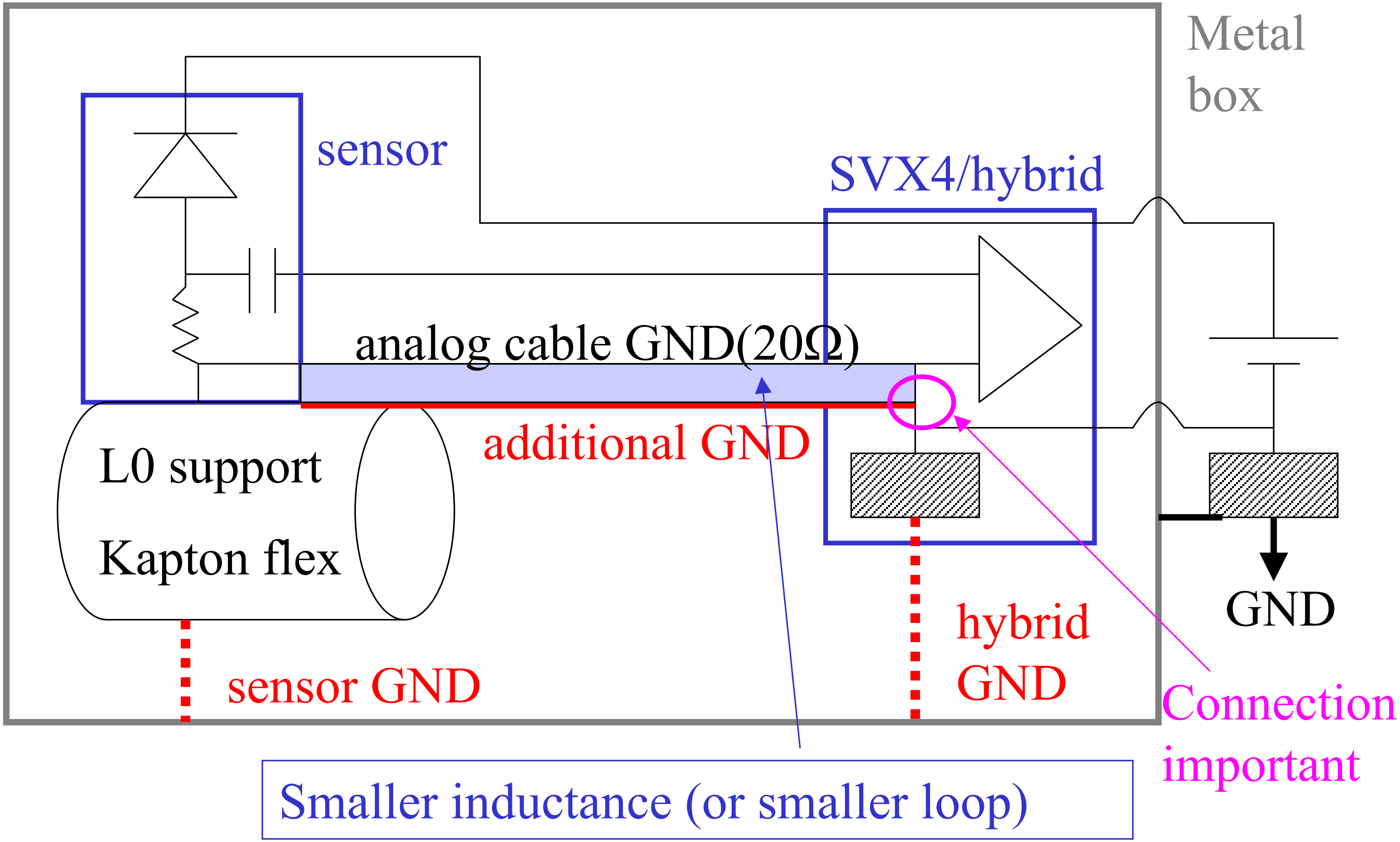
➔ Special caution needed in grounding scheme

- Sensor/analog cable can be coupled to the support structure capacitively
- Controlling proximity between detector and support structure is important



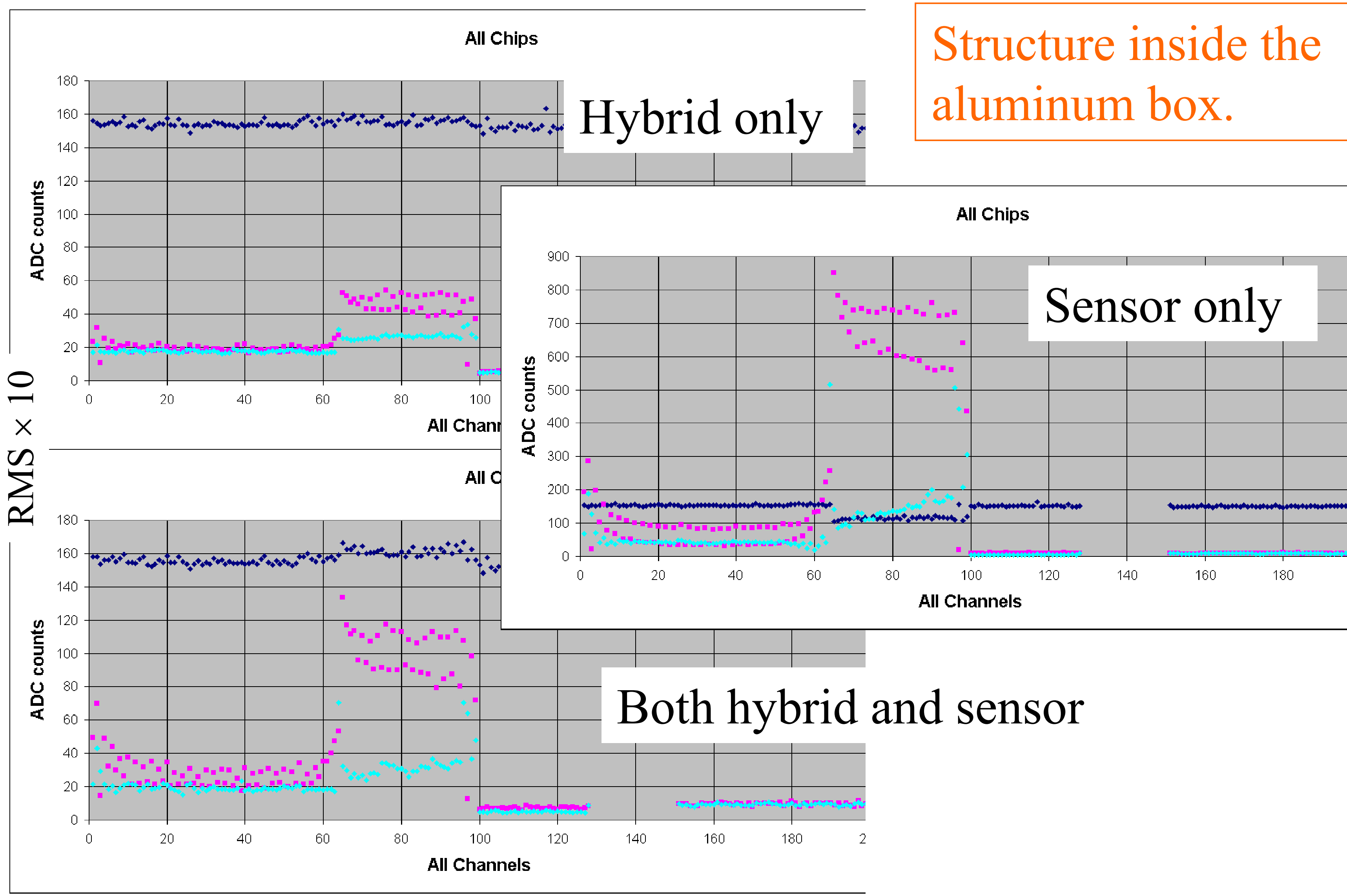
Noise vs distance between analog cable and ground plane

Grounding Study

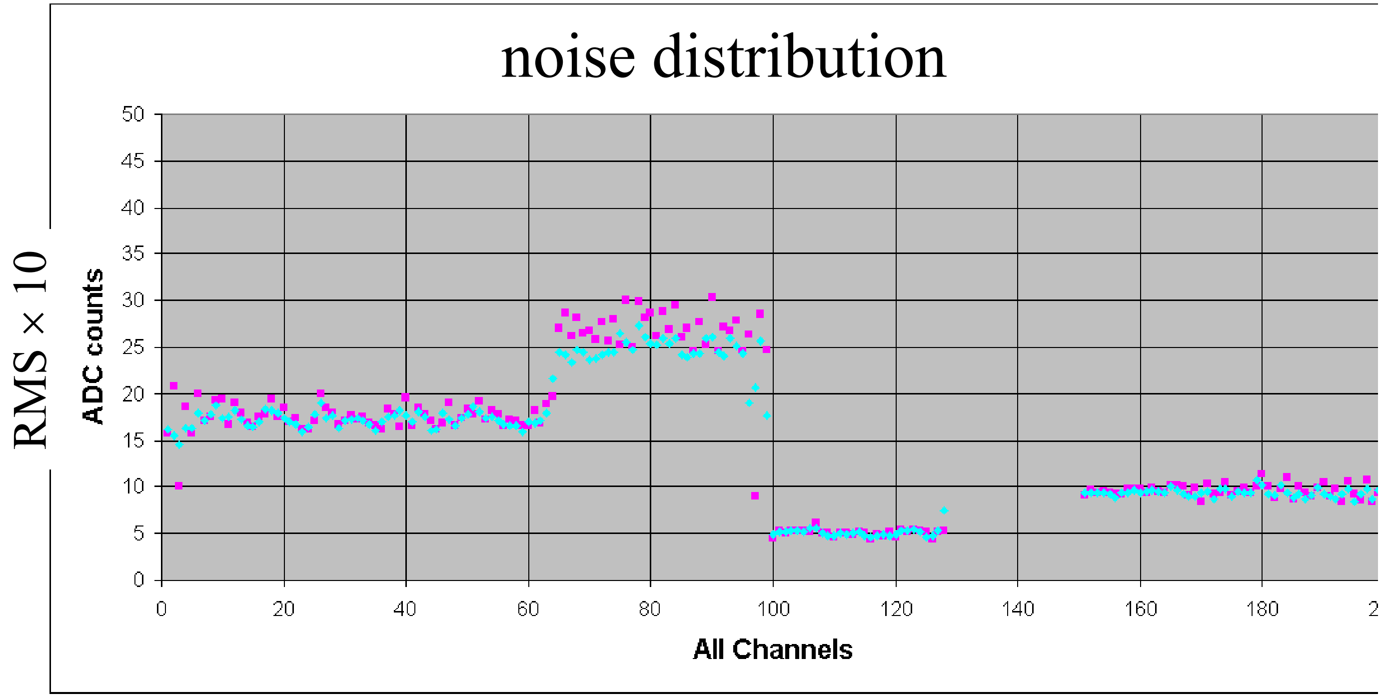


Grounding Study – cont'd

Structure inside the aluminum box.



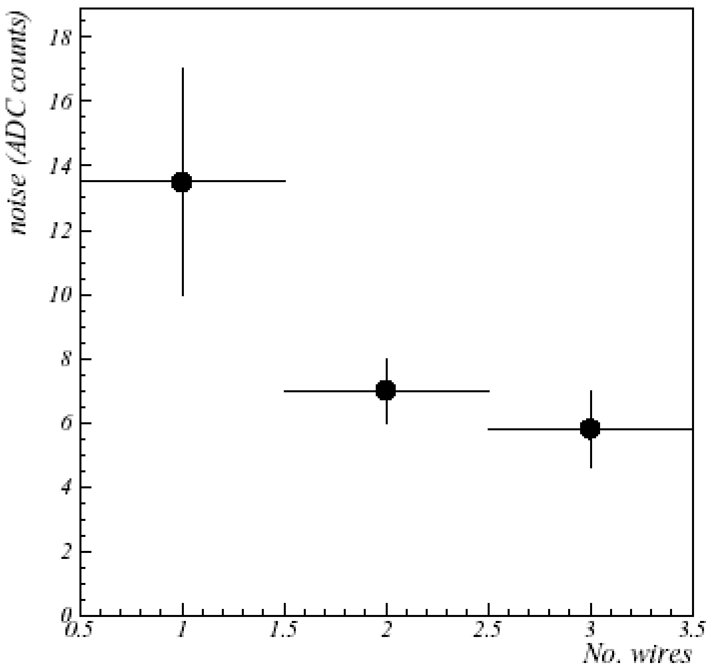
Grounding Study – cont'd

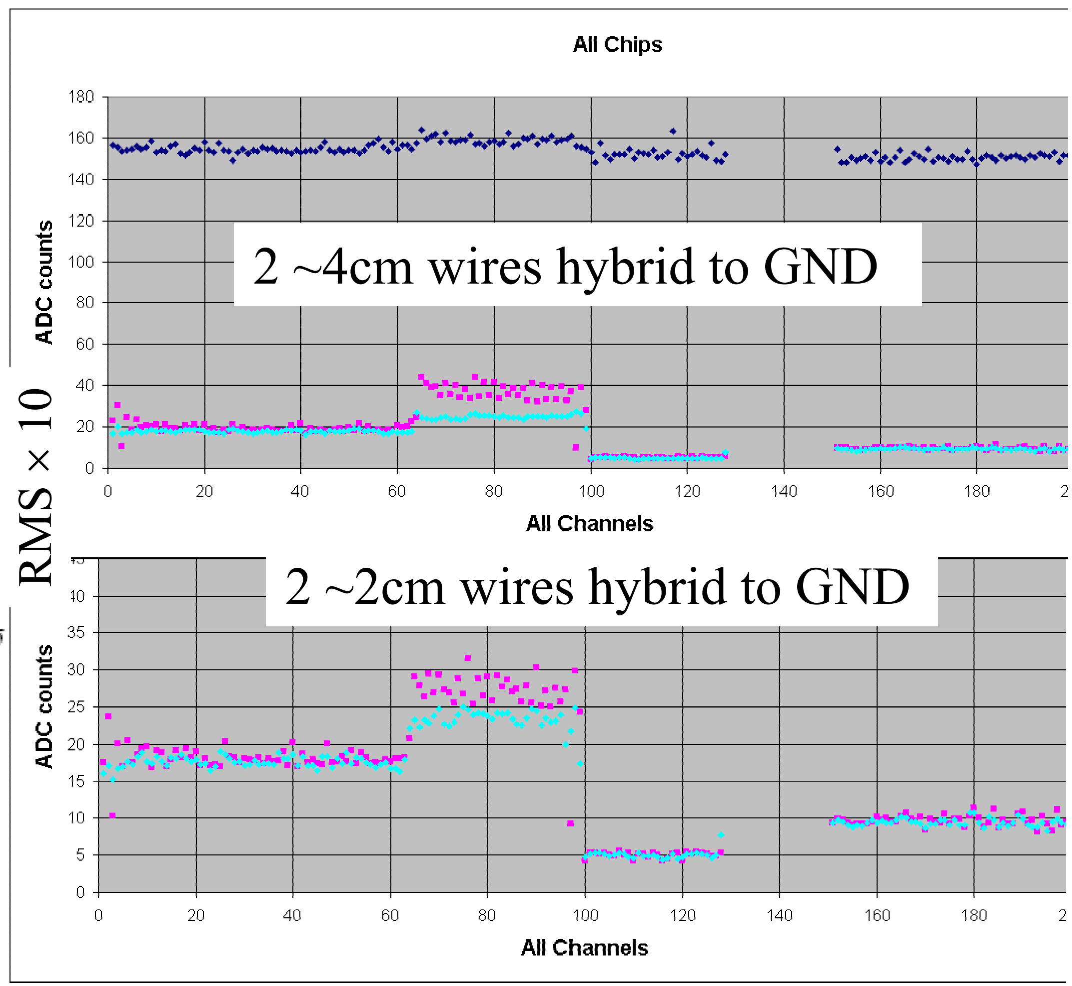


- After adding extra ground connection just below the analog cable (and achieving low inductance ground connection at hybrid ← see next slide), S/N maintained to be ~ 11

Importance of Low Inductance Connection

- In frequency range of our interests, low impedance connection is equivalent to low inductance connection

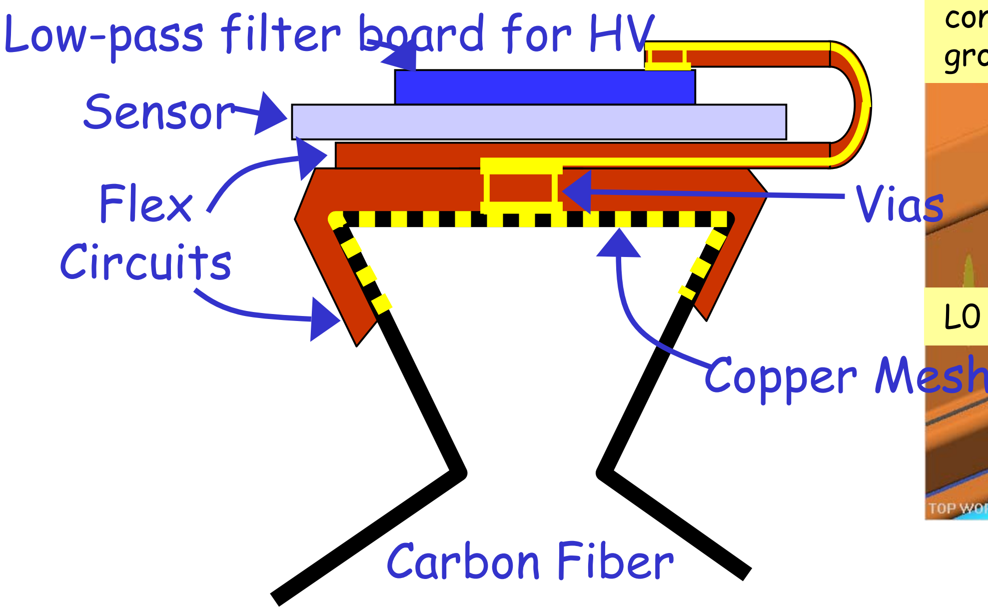


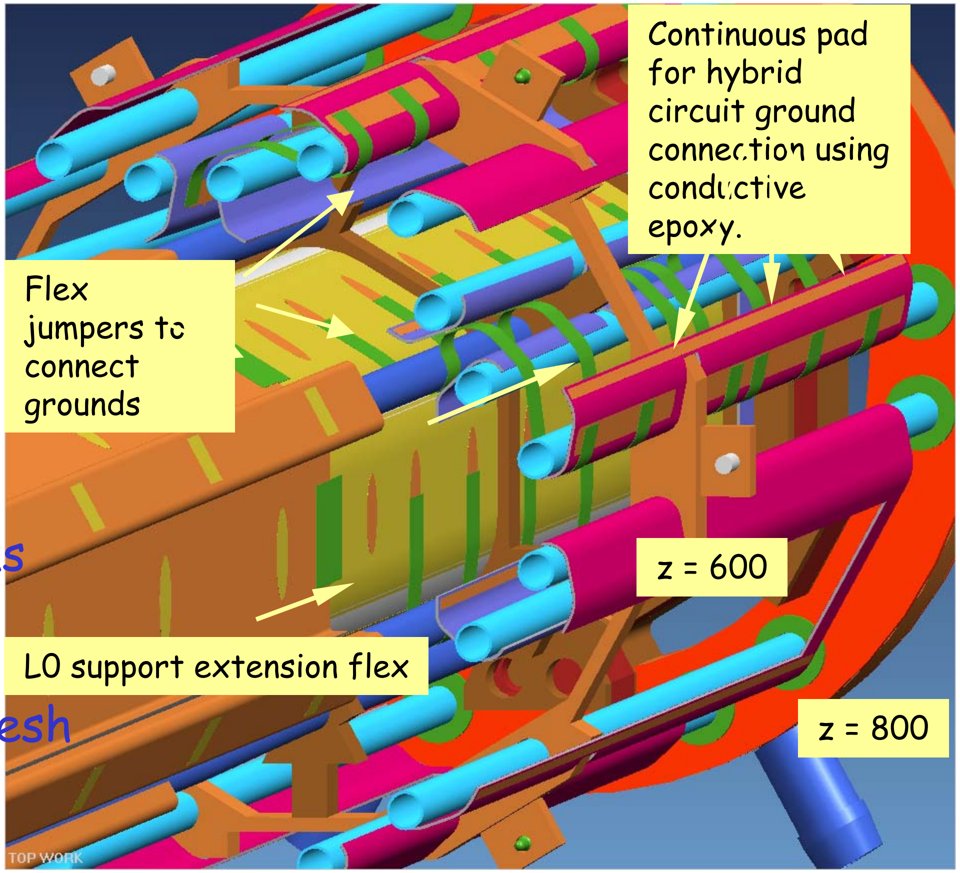


- Clearly indicates low inductance connection reduces noise

Grounding Scheme

- Any conductor, i.e. carbon fiber support structure must be grounded with low inductance
- 114+ flexible printed circuits will be implemented to address grounding for L0





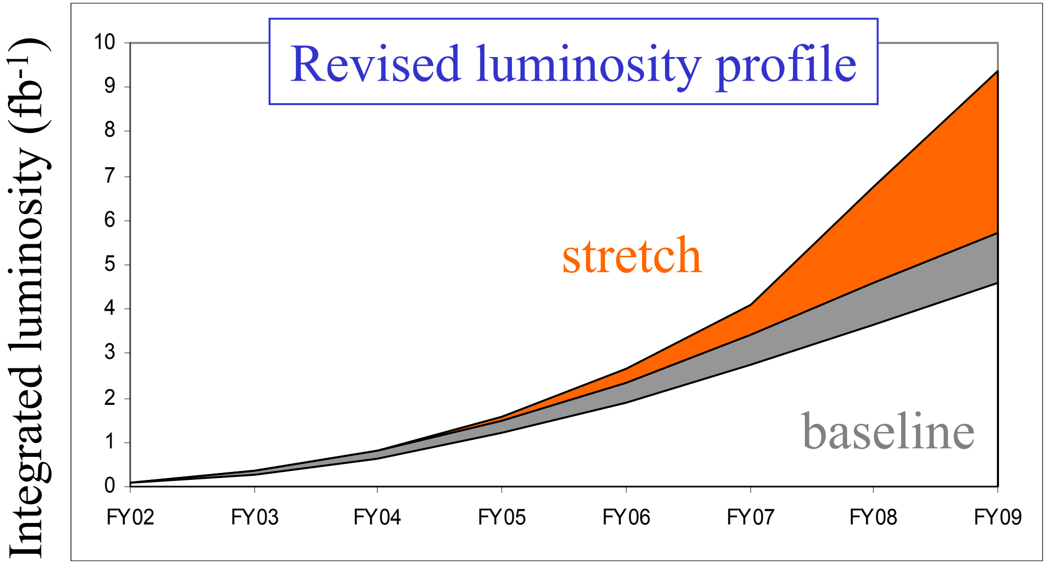
Status

Component	Vendor	Design	First Prototype Ordered	First Prototype Delivered	Second Prototype Ordered	Second Prototype Delivered	Final Order
L0 Sensors	HPK	✓					
L1 Sensors	HPK	✓	✓	✓			
L2 Sensors	HPK	✓	✓	✓			✓
Analogue Cable	Dycx	✓	✓	✓	✓ ✓	✓ ✓	
L0 Hybrid	Amitr.	✓	✓	✓	✓		
L1 Hybrid	CPT	✓	✓	✓	✓		
L2A Hybrid	CPT	✓	✓	✓	✓	✓	
	Amitr.	✓	✓	✓	✓		
L2S Hybrid	CPT	✓	✓	✓	✓		
Digital Cable	Honey	✓	✓	✓	✓ ✓	✓ ✓	
	Basic	✓	✓	✓	✓ ✓	✓ ✓	
	Century	✓	✓	✓	✓ ✓	✓ ✓	
Junction Card		✓	✓	✓	✓	✓	
Twisted Pr. Cable		✓	✓	✓	✓	✓	
Adapter Card		✓	✓	✓	✓	✓	
Purple Card		✓	✓	✓	✓	✓	✓
Test Stand Elctr.		✓	✓	✓			✓
High Voltage		✓					✓
Beampipe		✓					✓

Summary

- Design close to the final
  – A robust, straight-forward design has been developed
- Special focus on grounding of Layer 0
  – Reliable analog flex cable developed
  – Low inductance ground connection very critical
  – Flex circuit to achieve such low inductance connection to carbon fiber support structure
- Expected performance excellent
  – b-tagging capability thanks to Layer 0
  – design for 15fb^{-1}
- Project has prototyped all components of the design 🡐 remaining technical issue seems to be minor
- Final production orders have been started
- Project was on right track for completion in late 2005
- However…

Conclusion



Lifetime of present detector is estimated to be 3.6fb^{-1} with large uncertainty

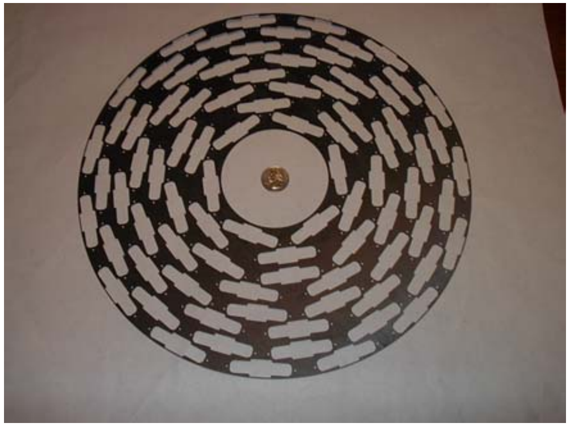
- Silicon upgrade has been terminated although D0 collaboration believes the upgraded detector is really needed
- As a proof of principle, Layer 0 and stave will be fabricated
- Possibility of installing only Layer 0 (with modified design) into the present detector

…backup slides

Stave and Other Support Structures

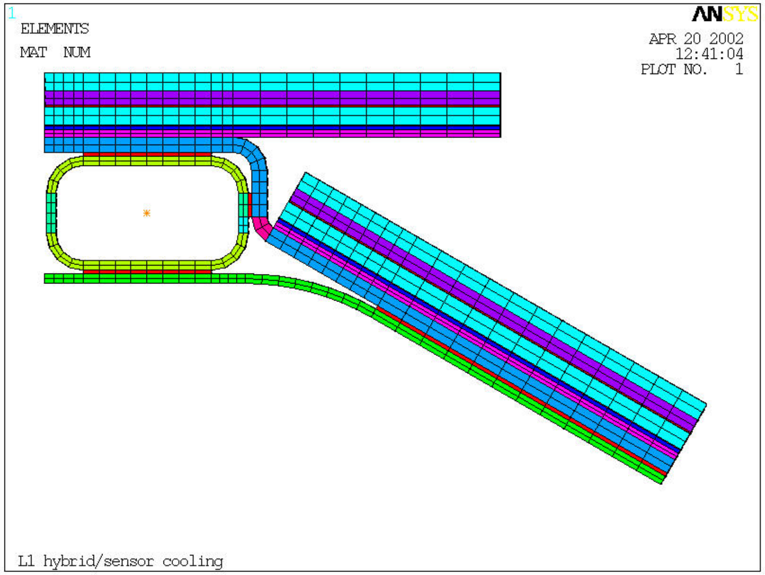
- Stave measurements – no outstanding issues
  - Stave core thickness
  - Robustness of stave core through temperature cycles
  - C-channel deflection and twist
  - Thermal performance with dummy hybrids
  - Stave flatness after module installation
  - Stave deflection creep
  - Silicon deflection under negative pressure (-5 psig)
  - Forming of PEEK cooling tubes and leak tightness
  - tube, glue joint tube-nozzle, glue joint nozzle cilran tube
  - Reference pinholders and alignment tolerances
  - Ongoing leak test of PEEK tubes

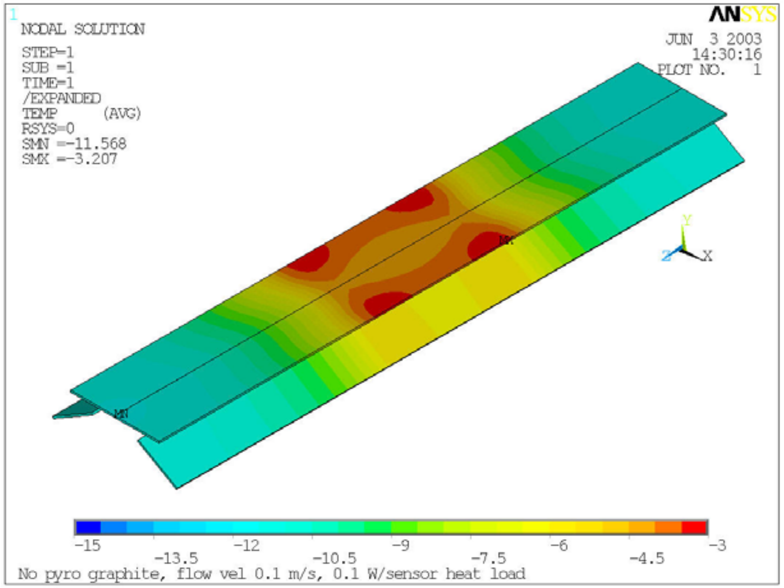
- Bulkhead measurements
  - Deflection to transverse and radial load
  - Placement of locating rings, now to few micron accuracy employing CMM as pick and place machine



Layer 1 Cooling

- Hybrids mounted on sensors; desired temperature of sensors -5 ^{0}C
- Cooling lines embedded in castellation

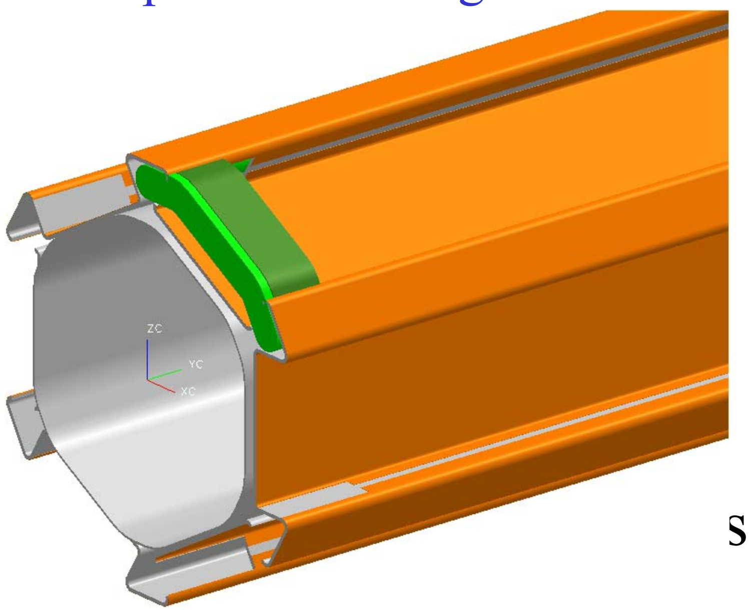


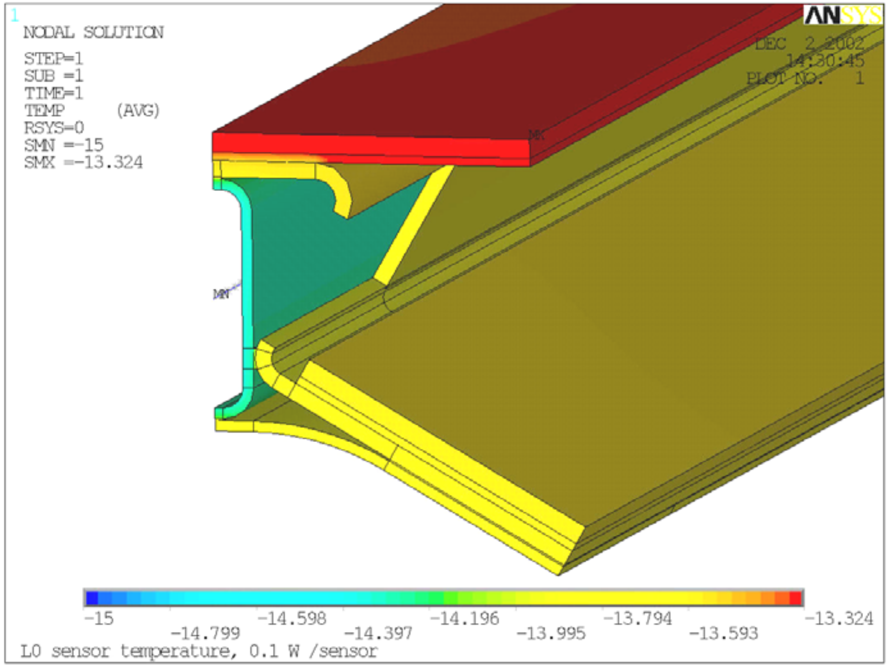


- Configuration in FEA analysis
  – $T_{coolant}$ = -15 ^{0}C, flow velocity 0.1 m/s, 40% ethylene glycol in water mixture
  – Maximum sensor temperature would be -3.2 ^{0}C for L1-B
    0.5 W/chip, 0.1 W/sensor, no pyrolitic graphite, added conductive epoxy at cooling tubes

Layer 0 Sensor Cooling

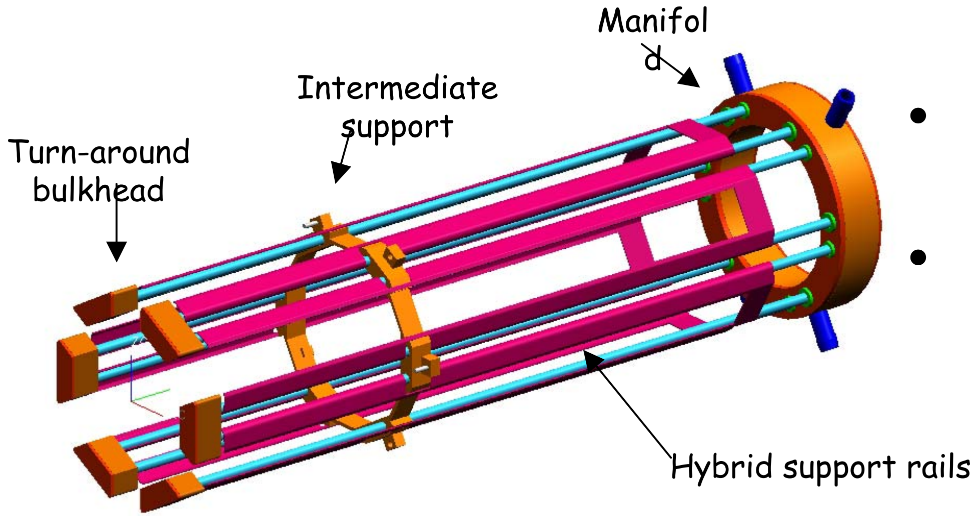
- Sensors cooled to -10 ^{0}C to minimize radiation damage; hybrids mounted outside tracking volume
  - Independent cooling lines for sensors and hybrids

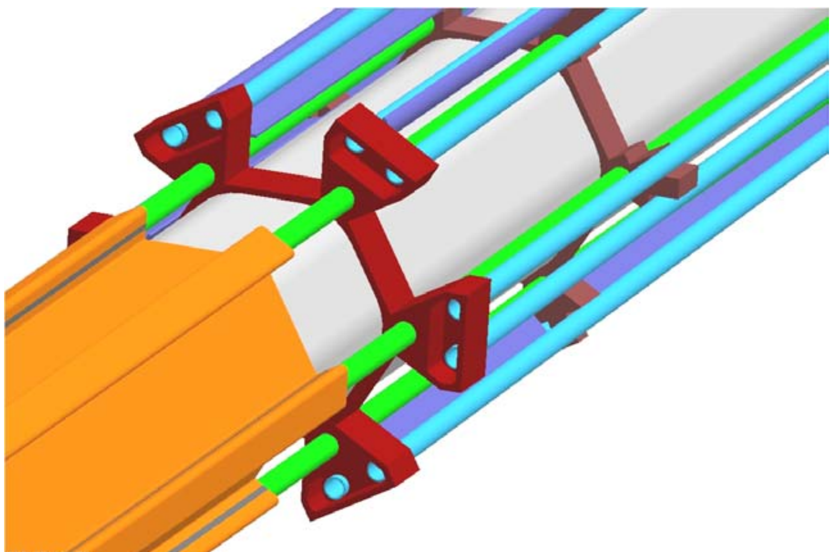




  - $T_{coolant}$ = -15 ^{0}C, flow velocity 0.2 m/s, 40% ethylene glycol in water mixture
  - Maximum sensor temperature would be -13.3 ºC (-12.85 ^{0}C)

Layer 0 Hybrid Cooling





- Independent cooling system for hybrids
- Hybrids mounted on pairs of support rails
  - Carbon fiber cooling fins that connect to the coolant tubes
  - Configuration in FEA analysis
    - 0.5 W / SVX4 chip
    - $T_{coolant}$ = 15 ^{0}C, flow velocity 0.2 m/s
    - 40% ethylene glycol in water mixture
  - Maximum hybrid temperature is -1.2 ^{o}C (0.82 ^{0}C)
  - Increase in coolant temperature is 2.02 ^{0}C

Material Budget

- Total material budget inside the tracking volume at normal incidence

Layer 0 Average Material Budget		
Item	avg. %X0	Fraction
Silicon Sensor	0.576	38.1%
HV insulation	0.054	3.6%
CF tube	0.085	5.6%
Coolant	0.133	8.8%
Support Structure	0.391	25.8%
Analogue Cables	0.274	18.1%
Total	**1.513**	**100%**

Layer 1 Average Material Budget		
Item	avg. %X0	Fraction
Silicon Sensor	0.454	15.5%
HV insulation	0.038	1.3%
CF tube	0.105	3.6%
Coolant	0.182	6.2%
Support Structure	0.388	13.2%
Digital Cables	0.741	25.2%
Hybrids	0.827	28.2%
Outer Shell	0.200	6.8%
Total	**2.935**	**100%**

Minimum total radiation length is 14.5% X_0 for full detector at normal incidence

Stave Material Budget				
Item	avg. %X0	Fraction	Weight (g)	Fraction
Silicon Sensor	0.681	27.1%	36.093	23.0%
SVX4 chips (5x2)	0.036	1.4%	1.933	1.2%
Hybrid	0.508	20.2%	20.724	13.2%
CF tube	0.114	4.5%	12.075	7.7%
Coolant	0.197	7.8%	17.100	10.9%
Stave Core	0.117	4.7%	11.563	7.4%
Stave Support	0.305	12.1%	32.157	20.5%
Readout cables	0.557	22.1%	25.135	16.0%
Total	**2.515**	**100.0%**	**156.780**	**100.0%**

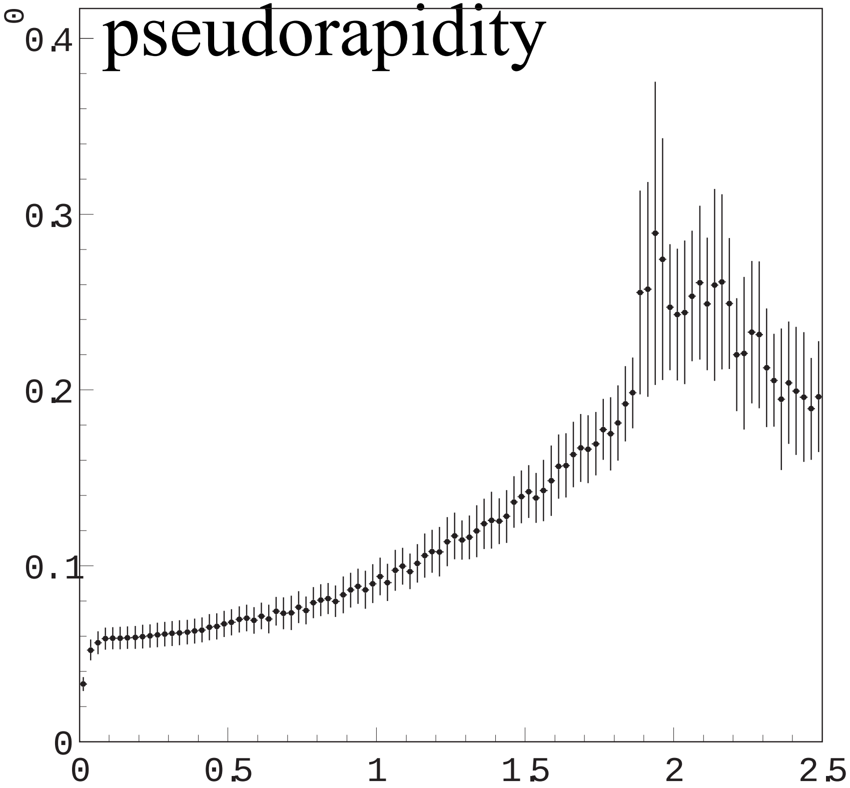
Material Budget outside Tracking Volume

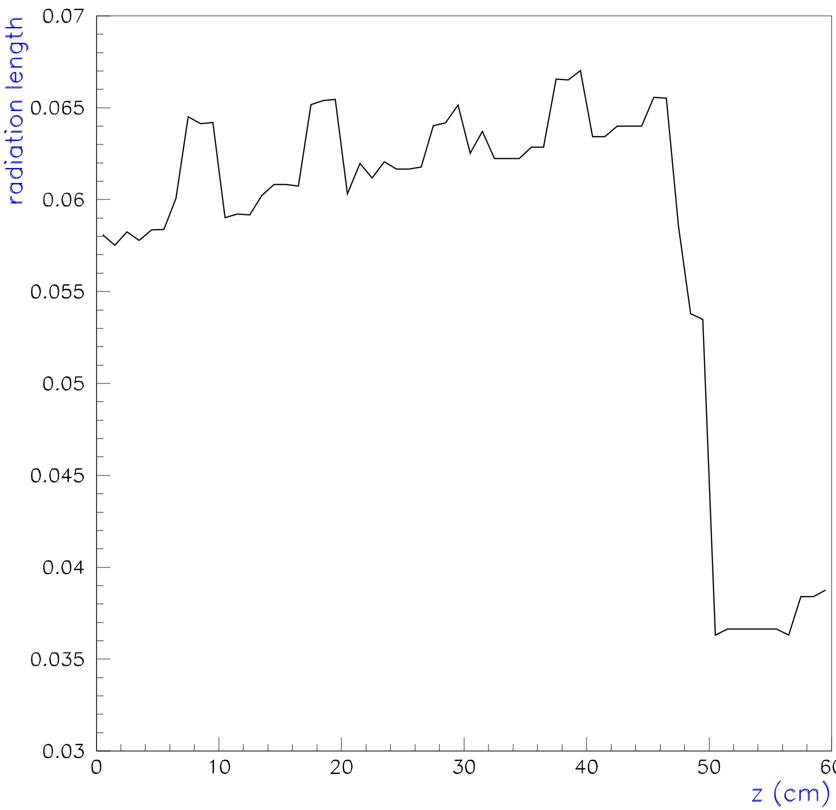
- Layer 0 has hybrids outside tracking volume
  - Inside tracking volume: layer 0 + layer 1 = 1.5 X_0 + 2.9 X_0 = 4.4 X_0

Layer 0/1 Average Material Budget Hybrid Region		
Item	avg. %X0	Fraction
L0 Hybrids	2.644	44.3%
L0 Digital Cables	0.971	16.3%
Analogue Cables	0.259	4.3%
L0 Coolant	0.268	4.5%
L0 Cooling Tubes	0.424	7.1%
L0 Support	0.581	9.7%
Digital Cables	0.212	3.5%
L1 Coolant	0.084	1.4%
L1 Cooling Tubes	0.081	1.4%
L1 Shells	0.451	7.5%
Total	**5.975**	**100.0%**

Summary Material Budget

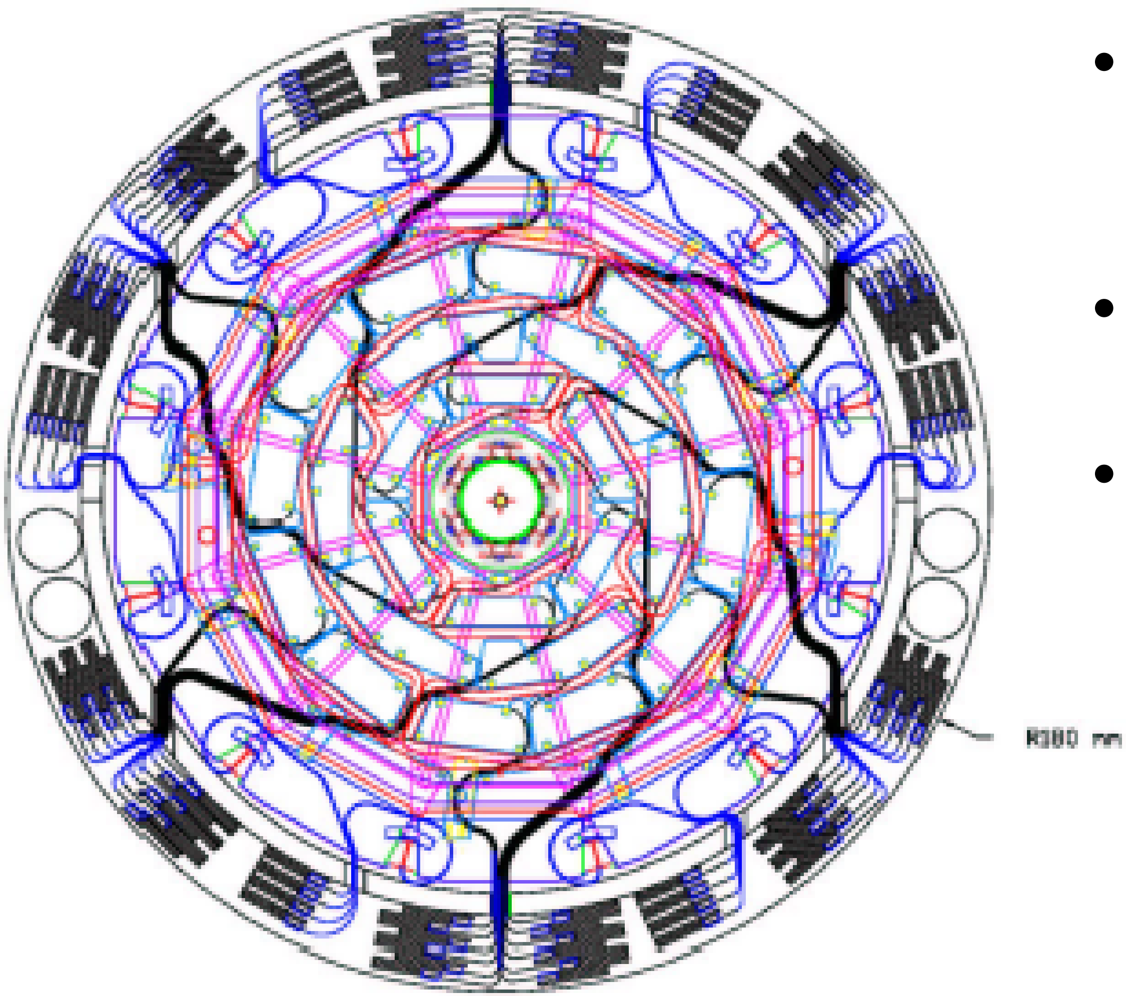
- Fraction of a radiation length as function of pseudorapidity





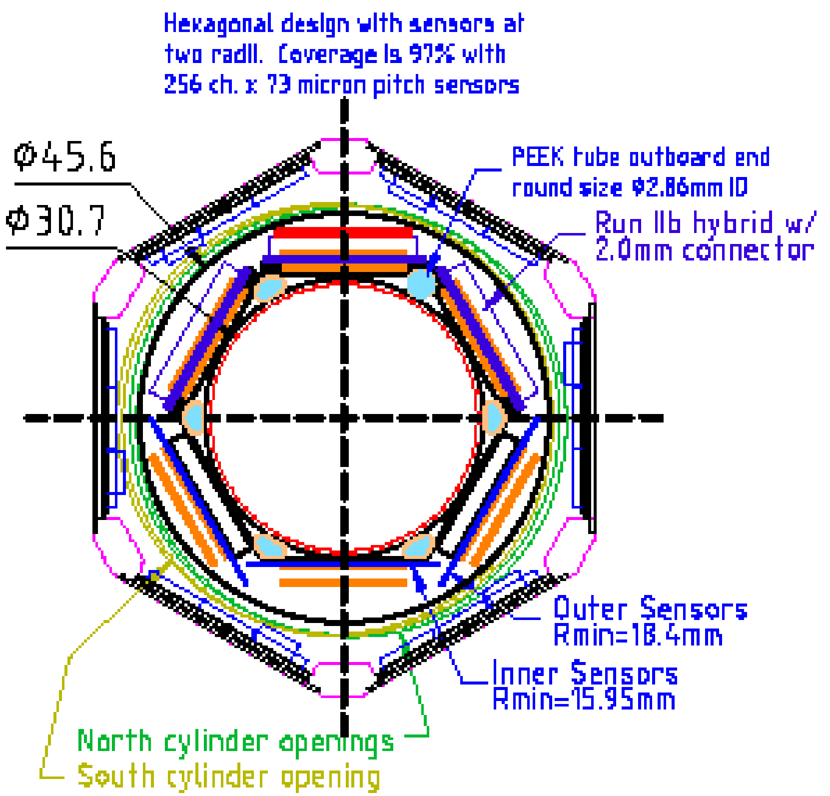
Material of beampipe included in simulation

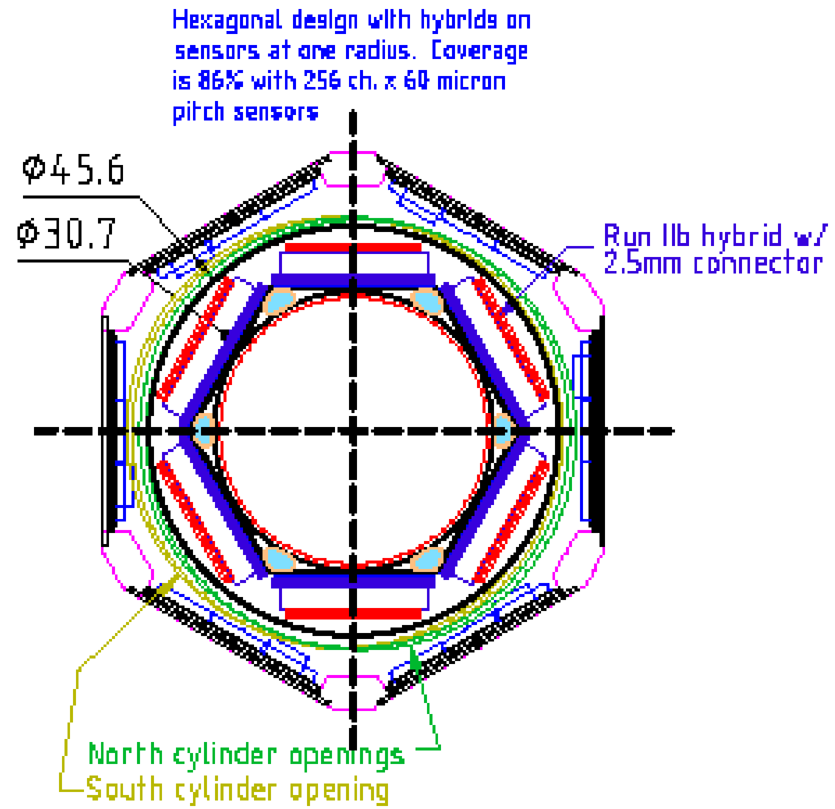
Idea of New Layer 0



- New Layer 0 inside the present run 2a detector
- This is not yet proposal stage
- Many design details remain to be developed
  – Does it fit?
  – Analog cable?
  – SVX4 or SVX2?

Another Idea of New Layer 0





Coolant passages are 5.5 sq. mm area, 9mm perimeter. Assuming coolant flows full length of beam pipe [1.8m] at this size we get a flow of 0.06 lpm per tube at dP = 3 psi. We suffer dT = 0.84 C cooling the hybrids on the inlet side.