

# Layer 0 in D0 Silicon Tracker for Run2b

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## Abstract

We report on the status of R&D of the innermost layer of D0 Silicon Tracker for Run2b. The emphasis is placed on the noise studies.

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The ultimate purpose of D0 Run2b Silicon Tracker is to tag a b-jet by looking for a displaced vertex. The good impact parameter resolution, therefore, is one of the most crucial requirements for the Silicon Tracker. Because the impact parameter resolution is determined by the ratio of innermost and outermost radius of the tracker in addition to the single hit resolution, it is essential to have the innermost layer as close as possible to the beam interaction region. The Layer 0 (L0) is an innermost layer of the Silicon Tracker to improve the impact parameter resolution for the reason above, sitting on 1.8 cm away from the interaction point. Our goal is to keep the S/N ratio better than 10 after accumulating  $15 \text{ fb}^{-1}$  of data.

While the L0 is very attractive in terms of physics, to build the L0 is technically very challenging because of the radiation hard environment

and the tight space constraints. The space constraints require us to read out the raw signal from the silicon sensor to the SVX4 readout chip mounted out of the fiducial region along the beam direction ( $\equiv \pm z$ ). We use the flex printed circuit cable for the readout, referred to as analog cable. There are twelve sensors for one azimuth coverage. Half of them is read out to  $+z$  direction, and the other half to  $-z$ . The maximum cable length is 43.5 cm.

There are two serious issues related to the noise caused by the analog cable. The first is a front-end noise of the readout chip due to the large capacitive load. The second is a pick-up noise by the analog cable. Below we describe the design and testing of the analog cable and L0 prototype, and grounding/shielding studies to address the two issues above.

Because of the requirements of ra-

diation hardness (we expect 10 to 15M rad) and fire safety regulations in Fermilab, Kapton type polyimide is the only possible choice for the substrate of the analog cable. The dielectric constant of the Kapton is 3.5.

The design issue of the analog cable is to keep a good balance between the capacitance and technical difficulty. We started to identify the allowed capacitance by estimating the size of noise. Figure 1 shows the expected noise as a function of load capacitance including both the sensor and analog cable. In the calculation

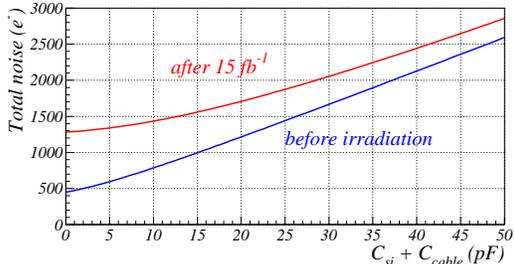


Fig. 1. Expected noise in terms of number of electrons as a function of total capacitance.

of noise, front-end noise, noise due to series resistance, and shot noise are summed in quadrature, assuming the shaping time of 132 ns. Since a minimum ionizing particle creates 22000 electrons by passing through the silicon sensor with the thickness of 300  $\mu m$ , the total capacitance must be maintained below 33.5 pF to keep the S/N better than 10. Subtracting the sensor's contribution, 23.5 pF or 0.53 pF/cm is the upper limit allowed for the analog cable.

Next the capacitance of the cable has

been estimated by the finite element calculation by ANSYS for various configurations. Figure 2, for example, shows the capacitance for different two trace pitches as a function of trace width. Based on these calcula-

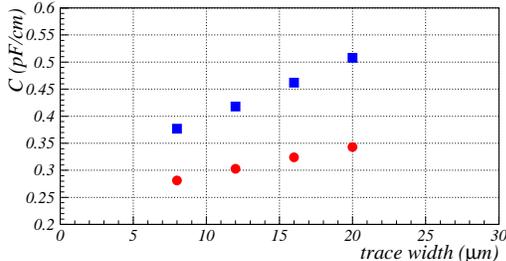


Fig. 2. ANSYS calculations of capacitance as a function of trace width. The red circles (blue squares) for 100(50)  $\mu m$  pitch.

tions, we decided the trace pitch and width to be 91  $\mu m$ , and 16  $\mu m$ , respectively. Because the readout pitch of the sensor and SVX4 chip is about 50  $\mu m$ , and the number of readout channels of the sensor (SVX4) is 256 (128), a pair of the analog cable with 128 signal traces with 45  $\mu m$  offset will be used for a single sensor and two SVX4 chips. Therefore twelve analog cables will be used for the one azimuth region. With this configuration, the capacitive coupling could come from not only the adjacent traces, but also the other cables of the cable stack. Selection of low dielectric material for the spacer of each cable is, thus, crucial to avoid extra capacitive load. We plan to have either meshed polypropylene or punched Kapton sheet as the spacer.

We placed an order of prototyping of the analog cable to Dyconex, Switzerland. They produce the ana-

log cable with plasma etching technology widely used for flex printed circuit. There are already three iterations and five batches of prototyping. The cables from the latest batch has capacitance of 0.35 pF/cm, which meets our specification. It is also verified that 90% of the cables has one or less open traces out of 129 signal traces (one for spare).

As the current CDF experience for their L00 indicates [1], huge pick-up noise is a potential problem for our L0, too. In order to study such noise, we built several prototypes of L0 module. First we confirmed that the noise level is consistent with the expected SVX4 noise performance with the measured capacitance of analog cable. Second we verified that the analog cable actually picks up RF like an antenna. The noise level almost linearly depends on the non-shielded area around the cable. Besides, larger noise is observed for the channel connected to the traces locating on the edge of cable. On the other hand, as farther from the edge, the noise level is smaller. This effect is attributed as the neighboring traces block RF each other. Third we confirmed that floating conductor near the cable brings the significant increase of noise in the localized area. These studies indicate the importance of proper grounding and shielding.

In order to have proper grounding scheme, Carbon Fiber's (CF) electrical characterization was performed because the support structure of the Silicon Tracker is made of the CF. The main conclusion is that the CF is

really a conductor for high frequency AC, such as 10MHz, which is relevant for us because the shaping time of the SVX4 chip is close to it. There is no distinctions among copper, stainless steel, and CF. (The detail is described in another presentation in this workshop [2].) This result implies that CF will work as a shielding material, *IF* it is correctly grounded. Since we have a small circuit on top of the sensor for low-pass filtering of HV, we plan to have a grounding connection between the CF support structure and the ground on the circuit board. To have a mechanically and electrically robust contact to the CF, flex printed circuit with copper mesh will be directly embedded to the CF structure when the CF support structure will be formed.

In summary, we described the R&D of L0 Silicon Tracker for D0 Run2b with the special focus on the analog cable and the related noise issues. The baseline design has been fixed to resolve those noise problems.

## Acknowledgments

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## References

- [1] C. Hill, this workshop.
- [2] B. Quinn, this workshop.