

Layer 0 in D0 Silicon Tracker for Run2b

K. Hanagaki

Fermilab, P.O.Box 500, Batavia, IL, 60510

Abstract

We report on the status of R&D of the innermost layer of the D0 Silicon Tracker for Run2b. Because of the space constraints, the cooling issues and the amount of material, the analog signal from the sensor must be transmitted to the readout chip. This scheme is a potential noise source due to the extra capacitive load and possible RF pickup. We focus on the noise studies to address these issues.

Key words: Silicon Tracker, Flex Printed Circuit Cable

PACS: 29.40.Gx

The ultimate purpose of the D0 Run2b Silicon Tracker is to tag a b -jet by looking for a displaced vertex. In order to improve the impact parameter resolution, the innermost layer, Layer 0 or L0, is placed at 1.8 cm from the interaction point (2.7 cm for the Run2a D0 Silicon Tracker). Our goal is to keep the S/N ratio better than 10 after accumulating 15 fb^{-1} of data.

The space constraints, the cooling issue of the silicon sensor, and the amount of material require us to transmit the analog signal from the sensor to the SVX4 readout chip, which is mounted outside the fiducial region along the beam direction ($\equiv \pm z$)¹. We use a flex printed circuit cable for the readout, referred to as ana-

log cable. There are twelve sensors for each of twelve azimuthal section. Half of them are read out to the $+z$ direction, and the other half to the $-z$. The maximum cable length is 43.5 cm. There are two serious issues related to the noise caused by the analog cable. The first is front-end noise of the readout chip due to the large capacitive load. The second is pickup noise by the analog cable, as the current CDF experience for L00 indicates².

Because of the requirements of radiation hardness (we expect 10 to 15M Rad) and fire safety regulations in Fermilab, Kapton type polyimide is the only possible choice for the substrate of the analog cable. The dielectric constant of the Kapton is 3.5. Figure 1 shows the expected

¹ Int. J. Mod. Phys. A16S1C 1091 (2001).

² C. Hill in this workshop.

noise as a function of load capacitance including both the sensor and analog cable. In the calculation of

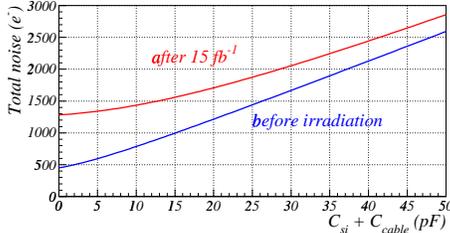


Fig. 1. Expected noise in terms of number of electrons as a function of total capacitance. The ENC of front-end noise used here is $[450 + 43 \times C(\text{pF})]e$.

noise, front-end noise, noise due to series resistance, and shot noise are summed in quadrature, assuming a shaping time of 132 ns. Since a MIP creates 22000 electrons by passing through the $300 \mu\text{m}$ thick silicon sensor, the total capacitance must be maintained below 33.5 pF to keep the S/N better than 10. Subtracting the sensor's contribution, 23.5 pF or 0.53 pF/cm is the upper limit allowed for the trace capacitance of the analog cable.

The capacitance of the cable has been estimated by ANSYS finite element calculation. Figure 2, for example, shows the capacitance for two different trace pitches as a function of trace width. Based on these calculations, we decided the trace pitch and width to be $91 \mu\text{m}$, and $16 \mu\text{m}$, respectively. Because the readout pitch of the sensor and SVX4 chip is about $50 \mu\text{m}$, and the number of readout channels of the sensor (SVX4) is 256 (128), a pair of analog cables each with 128 signal traces with a $45 \mu\text{m}$ offset will be used for a single sensor and two

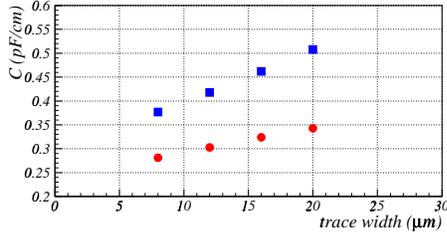


Fig. 2. ANSYS calculations of capacitance as a function of trace width. The circles (squares) for 100(50) μm pitch.

SVX4 chips. Therefore twelve analog cables will be used for one azimuthal sector.

Dyconex in Switzerland³ produced several prototype analog cables with plasma etching technology widely used for flex printed circuits. The traces are made of copper. The bonding pads are gold-plated. There are three iterations and five batches of prototyping. It is verified that 90% of the cables has at most one open trace out of 129 signal traces (one for spare). The capacitance has been measured to be 0.35 pF/cm, which meets our specification. The noise level is also measured by the prototype L0 consisting of the analog cables and the SVX4 chip. The increase of the noise relative to the bare chip, which comes from the extra capacitive load by the cable, is consistent with the measured value of 0.35 pF/cm.

Using several prototypes of L0 modules, we verified that the analog cable actually picks up RF like an antenna. The noise level depends almost linearly on the non-shielded area around the cable. Besides, large-

³ <http://www.dyconex.com/>

er noise is observed for the channel connected to the traces located at the edge of the cable. On the other hand, farther from the edge, the noise level is smaller. This effect is attributed to the neighboring traces blocking RF from each other. We also confirmed that a conductor near the cable, which is not grounded, brings a significant increase of noise in the localized area. These observations indicate the particular importance of having proper grounding and shielding.

Even with a proper grounding and shielding scheme, use of the analog cable requires us to avoid an extra capacitive coupling. The capacitive coupling could come not only from the adjacent traces, but also from the other cables in the stack. The ANSYS calculation indicates, for example, the trace capacitance increases from 0.33 pF/cm (single cable) to 0.45 and 0.57 pF/cm if the cables are stacked and each cable is separated by 200 μm thick material with ϵ_r of 2.0 and 3.0, respectively. This extra capacitive coupling due to the shielding material has been observed as shown in Fig. 3. The even-odd effect comes from that the distance between the two cables and the shield is different. Thus, selection of low dielectric material and the thickness for the spacer between the cables is very important. We plan to have either meshed polypropylene or punched Kapton sheet as the spacer.

The support structure for the two innermost layers will be made out of Carbon Fiber (CF). To design a proper grounding scheme the elec-

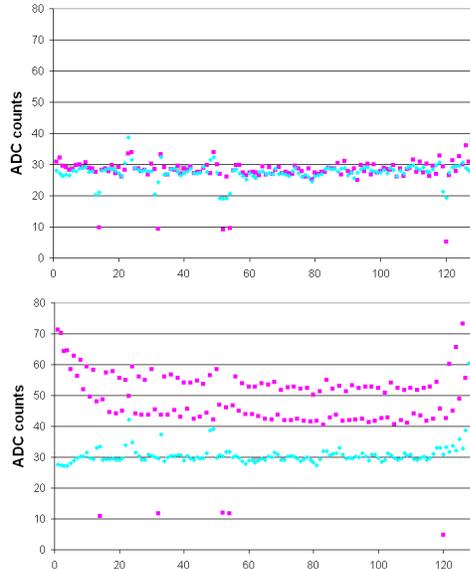


Fig. 3. Noise distribution (arbitrary scale) for single readout chip. The squares (diamonds) represent total (differential) noise. For the top (bottom), the cables are separated by 75 μm thick Kapton (plus 400 μm thick polypropylene mesh sheet) from the shielding metal.

trical properties of CF had to be mapped⁴. The main conclusion of our studies is that the CF is a good conductor for high frequency AC, such as 10MHz, which is relevant for us because the shaping time of the SVX4 chip is close to it. There are no distinctions among copper, stainless steel, and CF. This result implies that CF must be properly grounded, and will work as a shielding material, *IF* it is grounded.

In summary, we described the R&D of L0 Silicon Tracker for D0 Run2b with the special focus on the analog cable and the related noise issues. The baseline design has been fixed to resolve those noise problems.

⁴ B. Quinn, this workshop.