Studies of Pedestal Spliting

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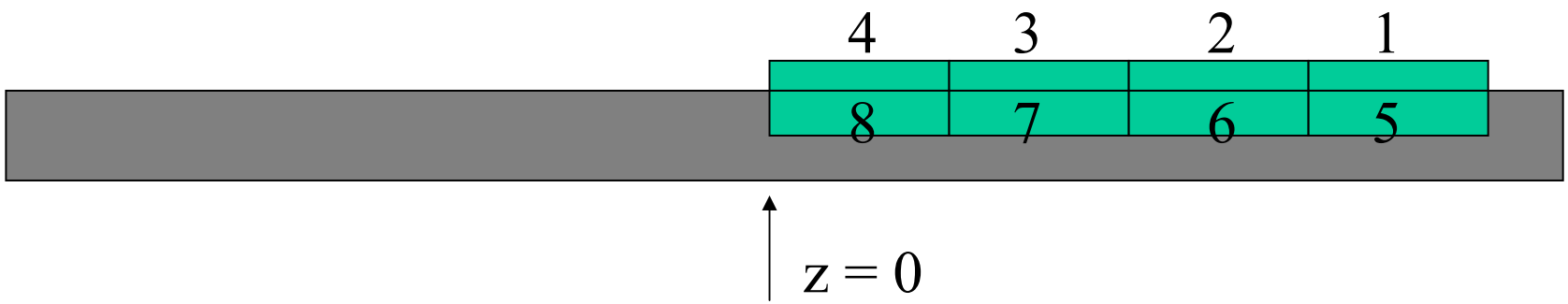
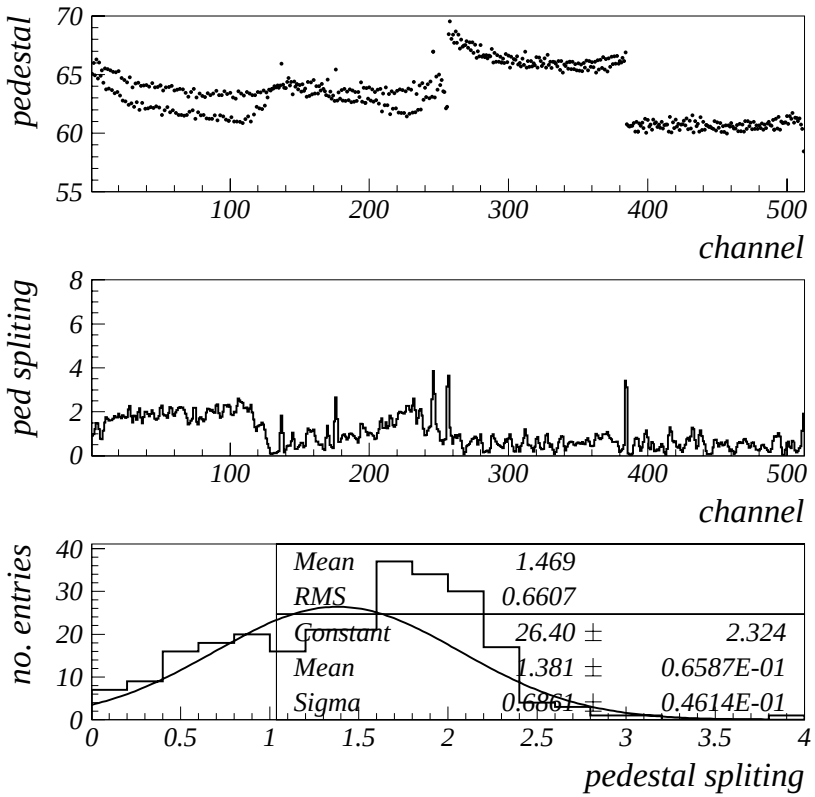
- 8 modules on the support structure



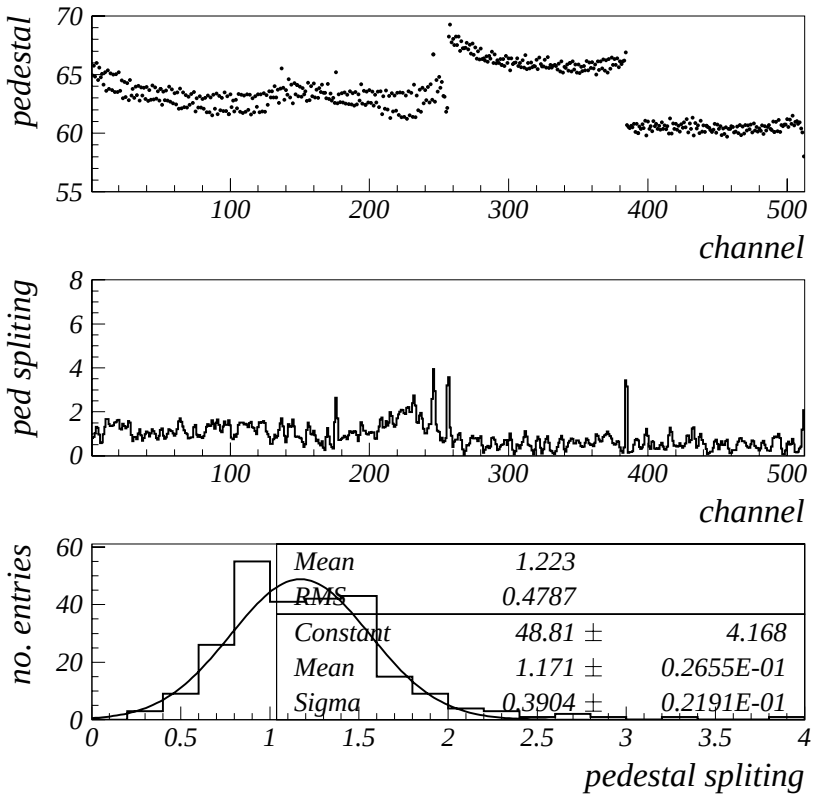
- Read out only 1 and 2 in this study
  - We know cal_sr in 2 has contribution to 1
  - Try to see the effect of clock
- HV = 50 V
- BW = 4 with 132 ns integration time

Starting point

pipeline depth same timing with cal_sr



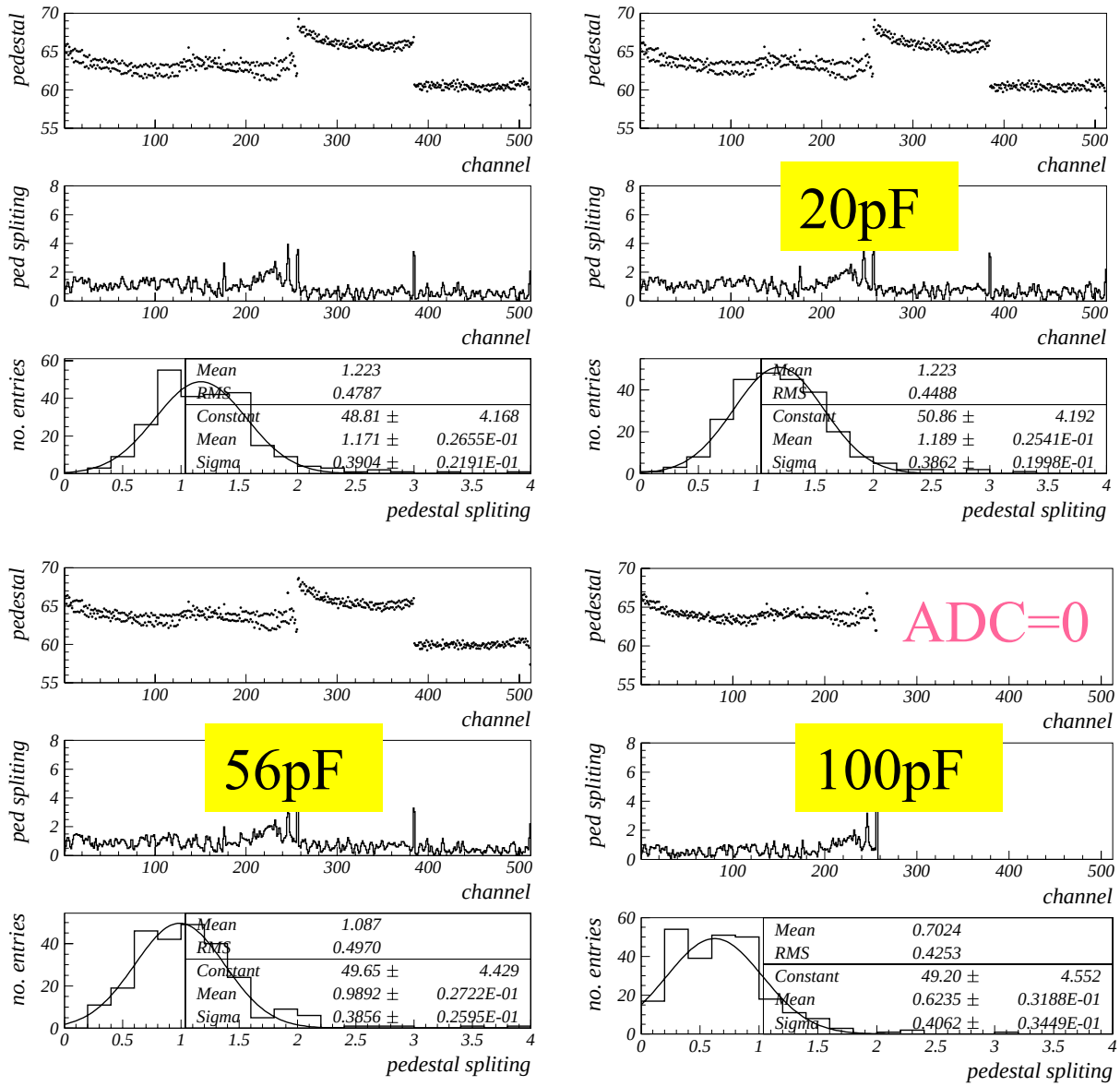
cal_sr away from sampling pipeline



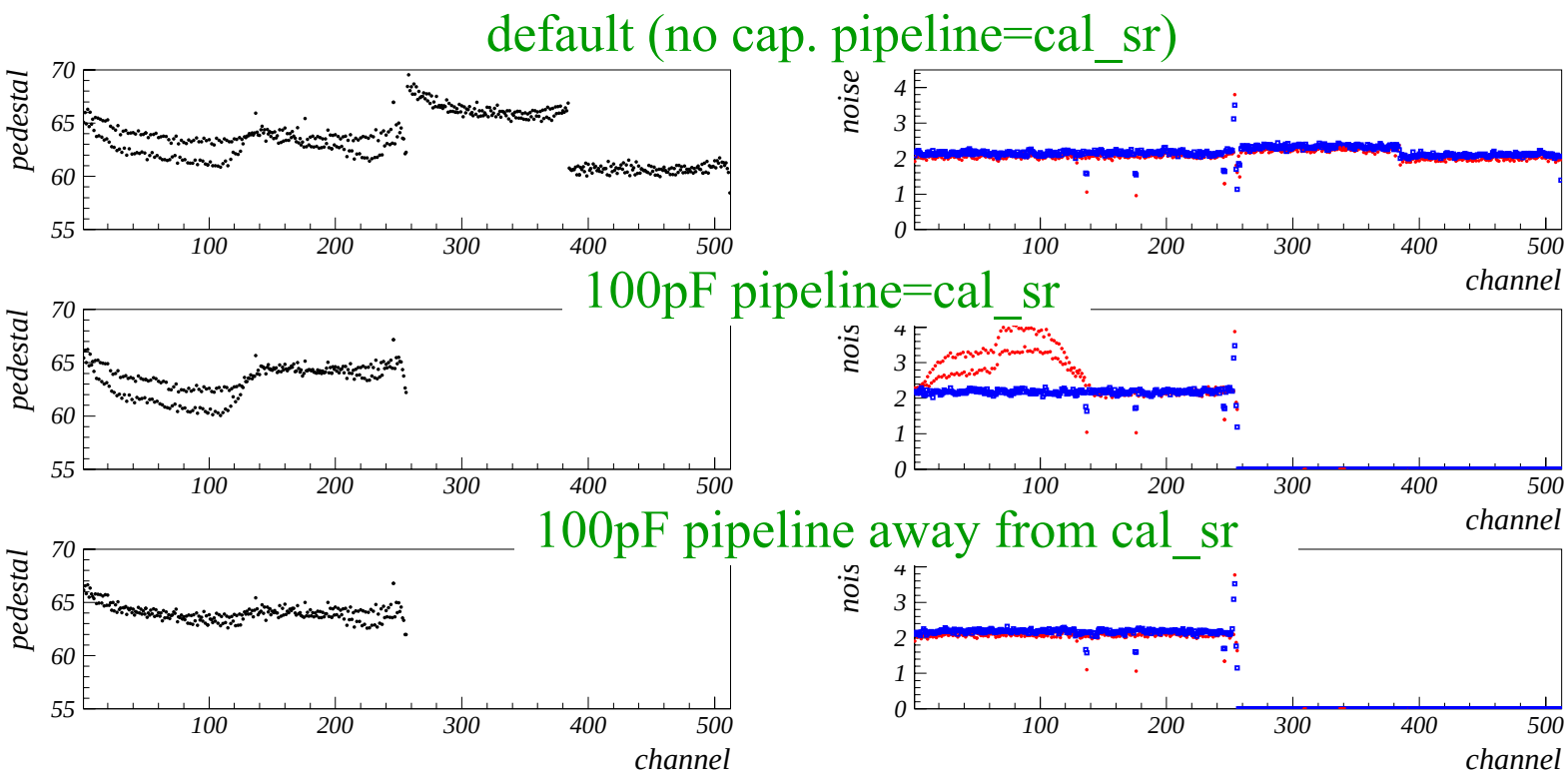
- Size of pedestal splitting is ~1.2 after eliminating cal_sr contribution (0.8-0.9 in single module)

Putting capacitor in parallel

- Failed to see the effect in the last report, but there was some mistake → repeated measurement
- capacitor is added on module 2
- sampling pipeline away from cal_sr
- some effect seen



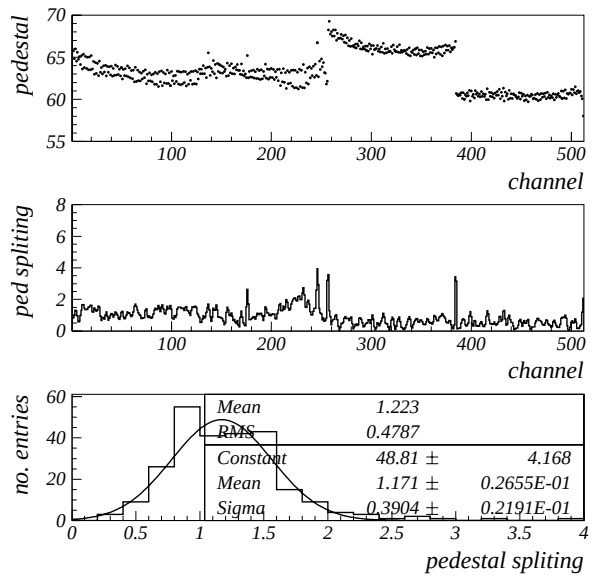
Noise level

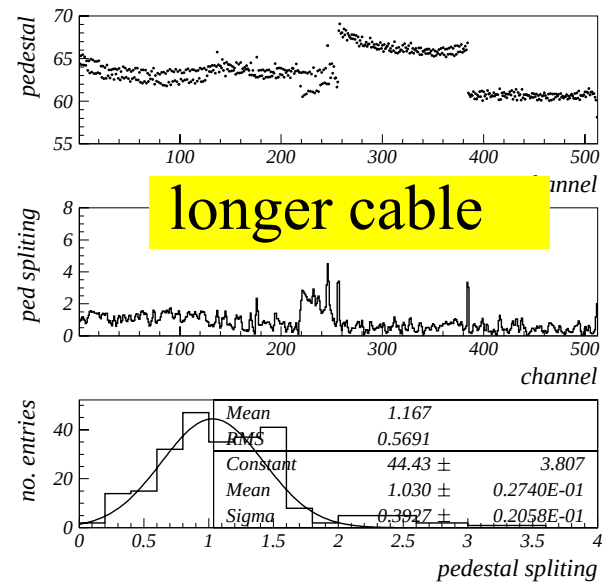


- We finally see not only the pedestal splitting but also pick-up noise, but why with this configuration?

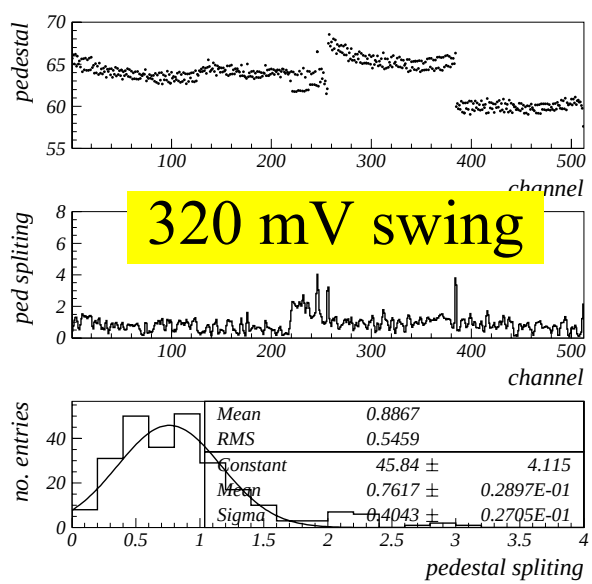
Reduced clock amplitude

- Again sampling pipeline away from cal_sr
- Pedestal splitting becomes smaller in module 1, but larger in 2 (?)

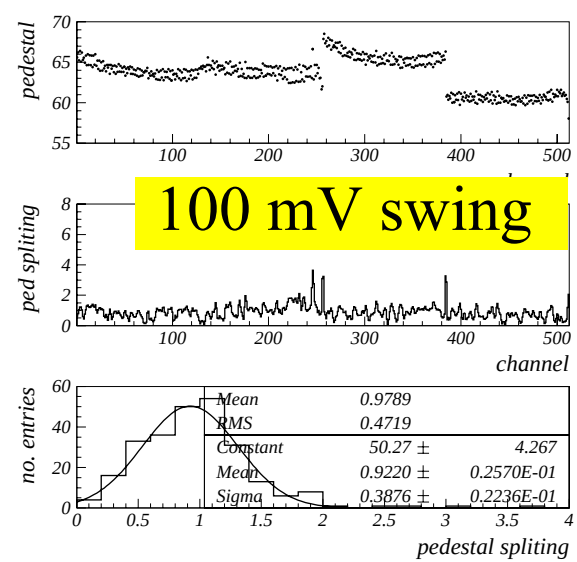




longer cable



320 mV swing

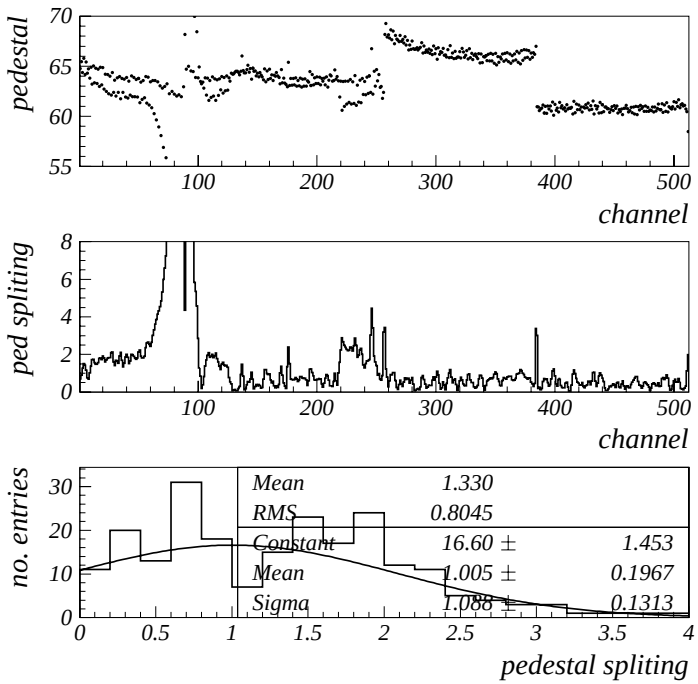


100 mV swing

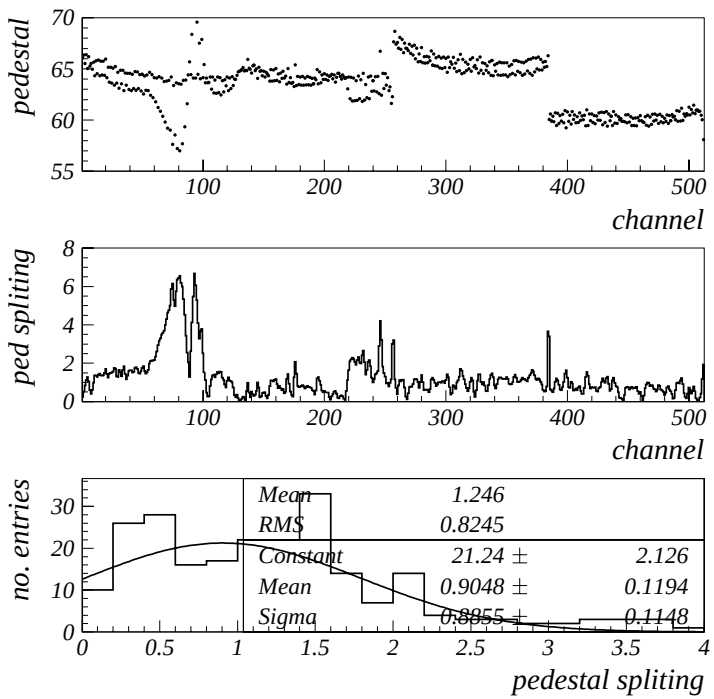
Other observation

- Local effect by cal_sr is enhanced after replacing the digital cable ← distance between digital cable to chip changed ???

normal clock



clock-clockbar 320mV



Summary

- We confirmed clock actually affects the size of pedestal splitting, on top of cal_sr
- Detailed mechanism is not clear
  - Reduced clock in module 2 helps to improve module 1, but makes module 2 worse
  - cal_sr effect is local or only for chip below the cal_sr trace, however, clock gives contribution to whole module