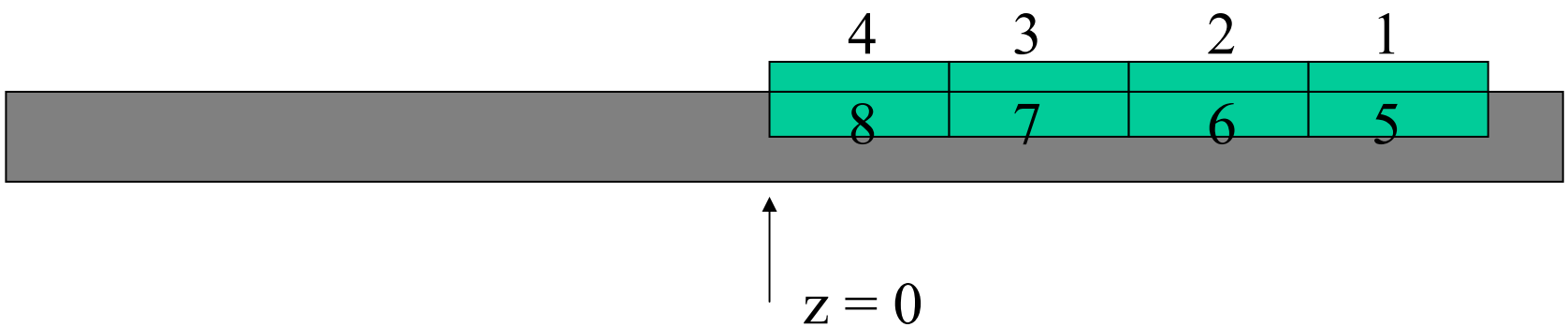
Test setup

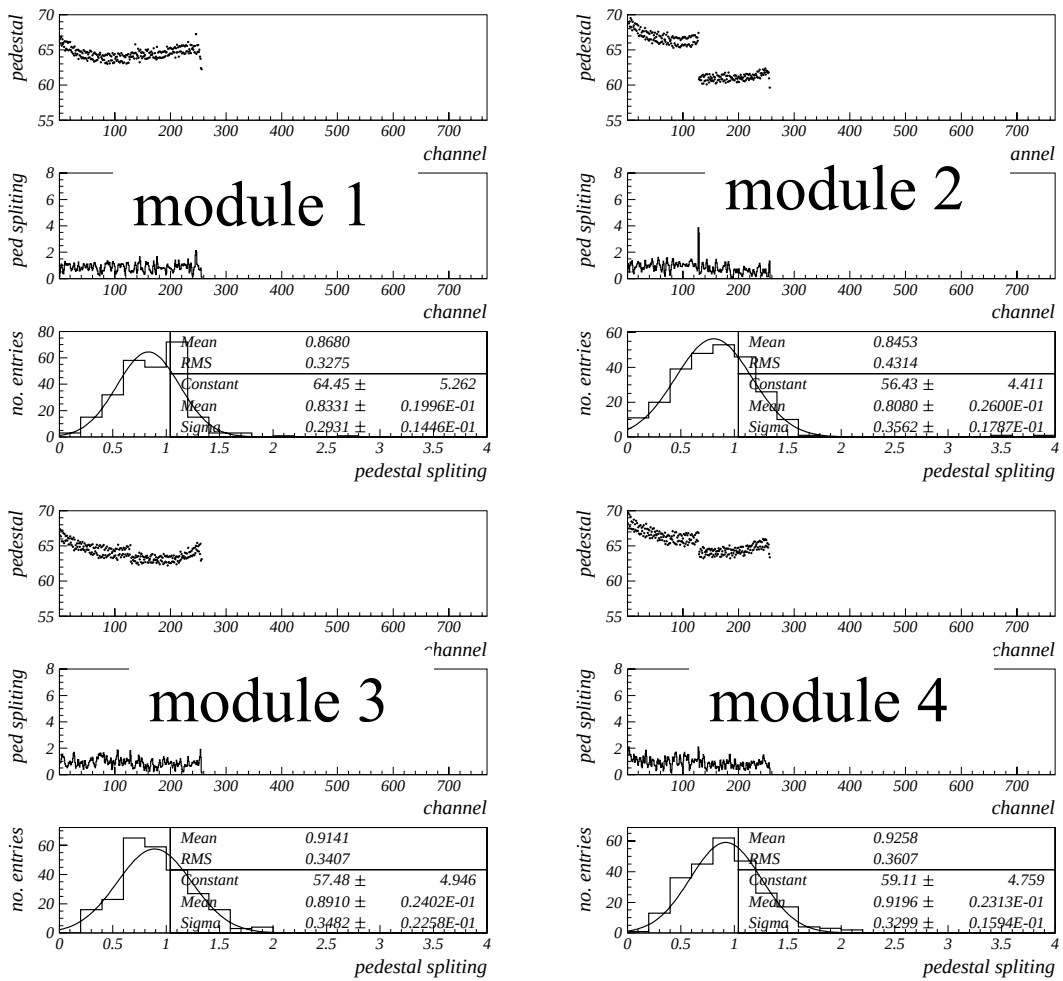
- 8 modules on the support structure



- module 1 (and 5) has the analog cable closest to the support structure
- 3 SASEQ → 6 modules simultaneously at maximum
- HV = 50 V otherwise mentioned
- BW = 4 with 132 ns integration time otherwise mentioned

Single module

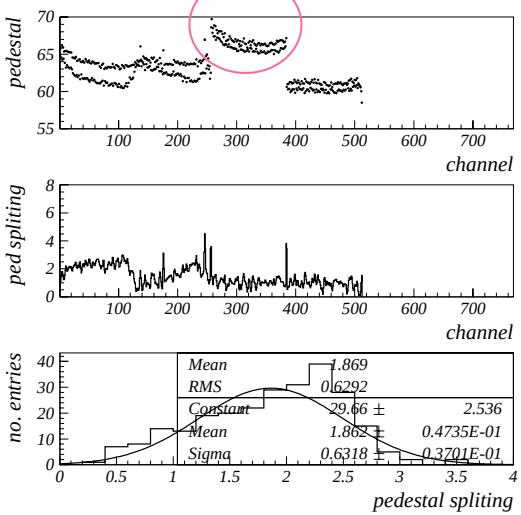
- Define the size of pedestal splitting as
  { |ped(i+1)-ped(i)| + |ped(i-1)-ped(i)| } / 2



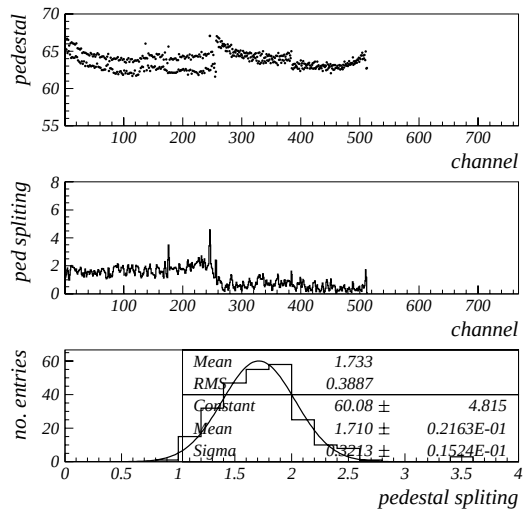
each has
0.8-0.9

Geometrical effect

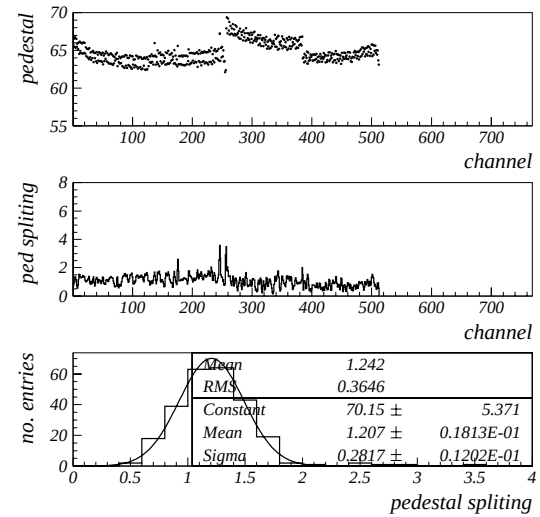
1-2



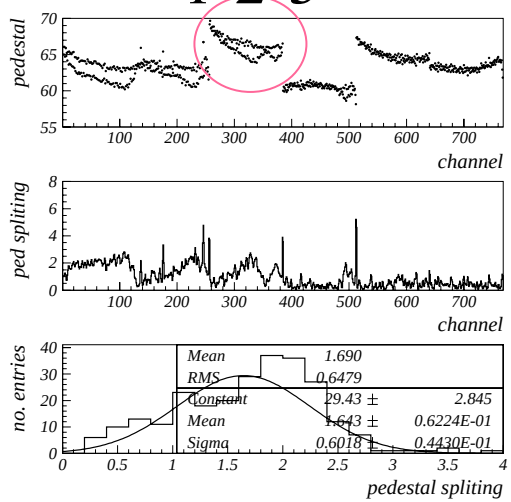
1-3



1-4

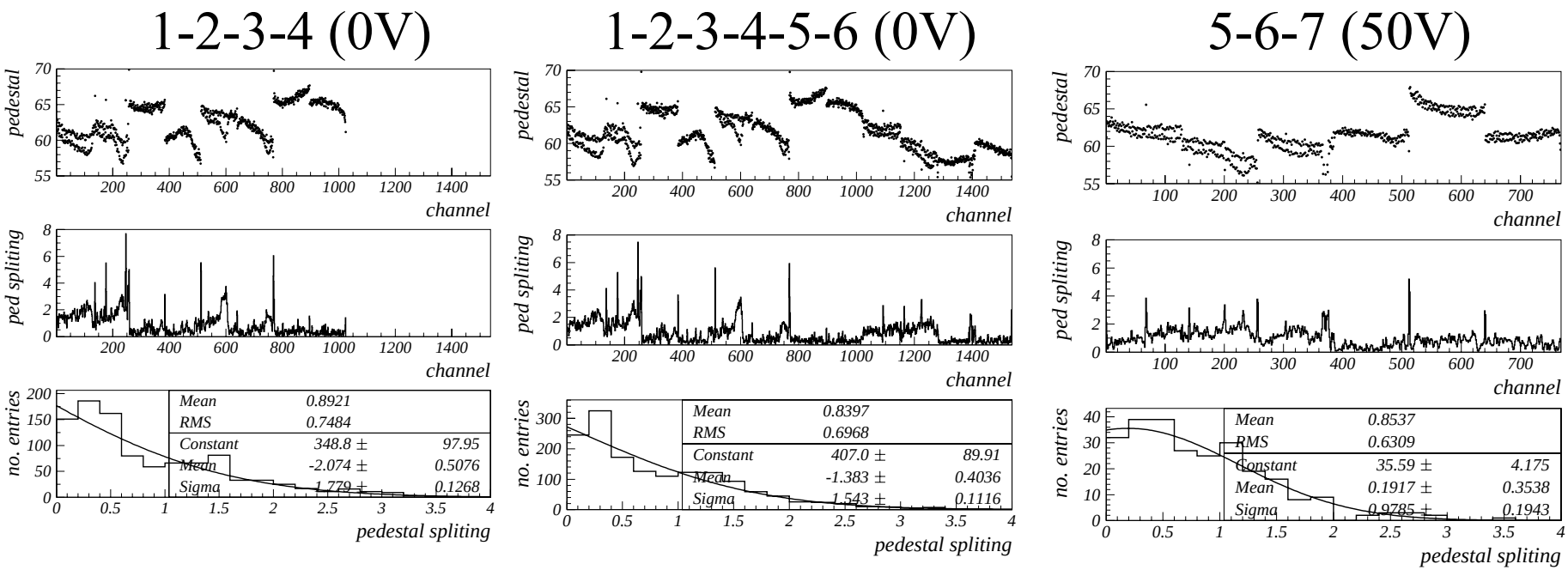


1-2-3



- ped splitting is enhanced by other modules, i.e. a module with digital jumper cable on top of the module of interest
- Looking at module 1, nearer module has more impact

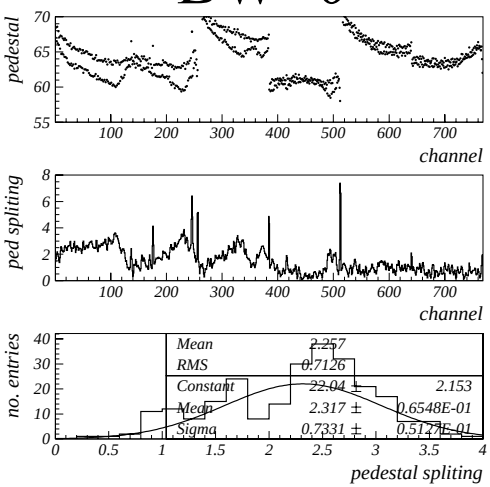
Geometrical effect – cont'd



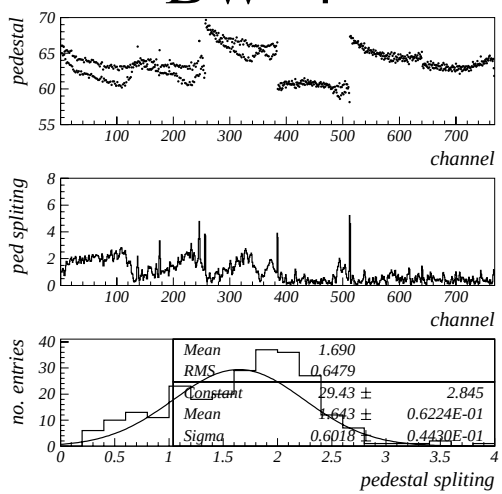
- module 1 has the most significant splitting
- also module 5

Risetime dependence (1-2-3 configuration)

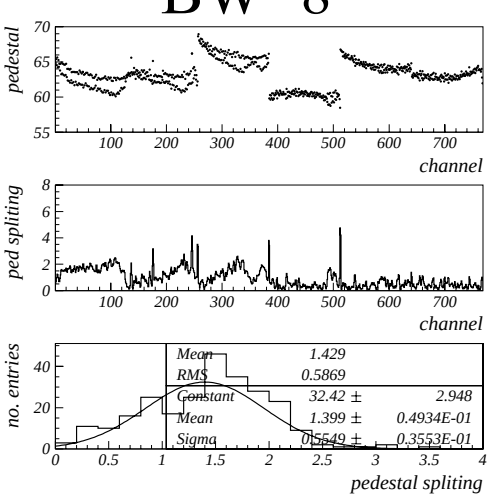
BW=0



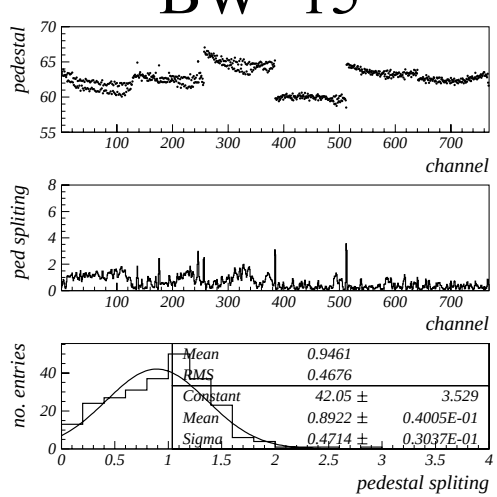
BW=4



BW=8



BW=15



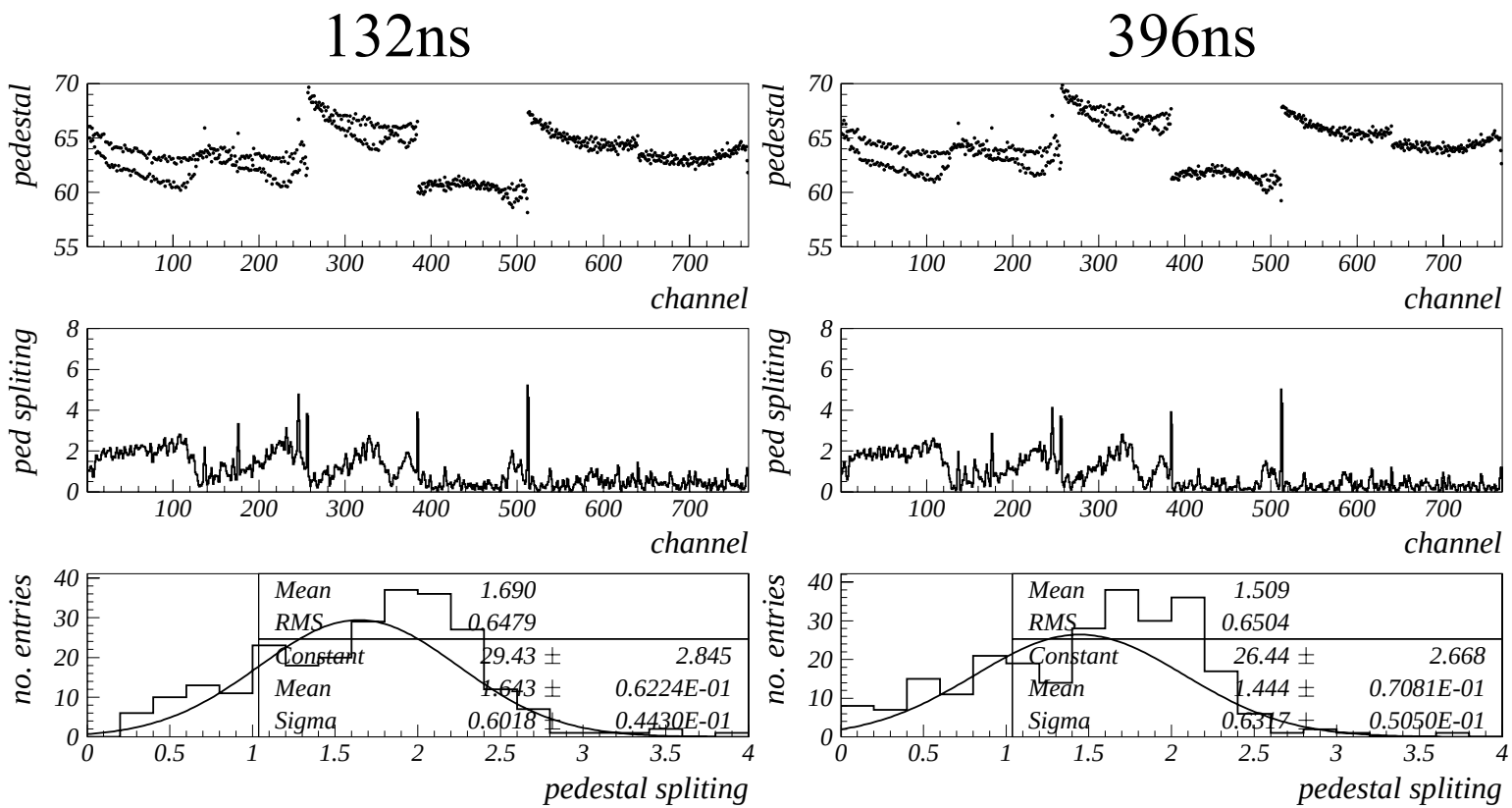
BW	PS	PS/Δ
4	1.64	0.0187
8	1.40	0.0163
15	0.89	0.0134

Δ is the response to cal_injet (cal-ped)

- also HV=0 reduces the splitting

➔ slower risetime reduces the splitting

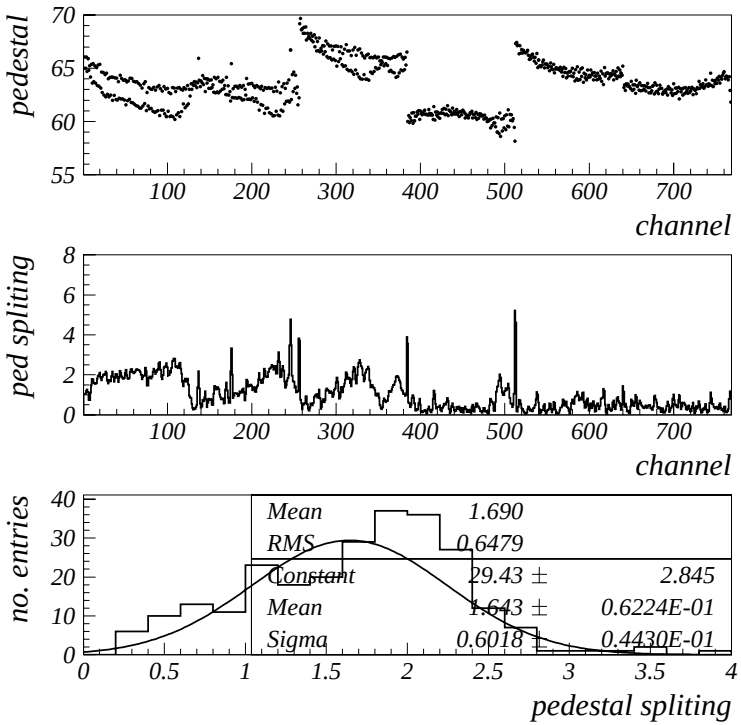
Integration time dependence (1-2-3)



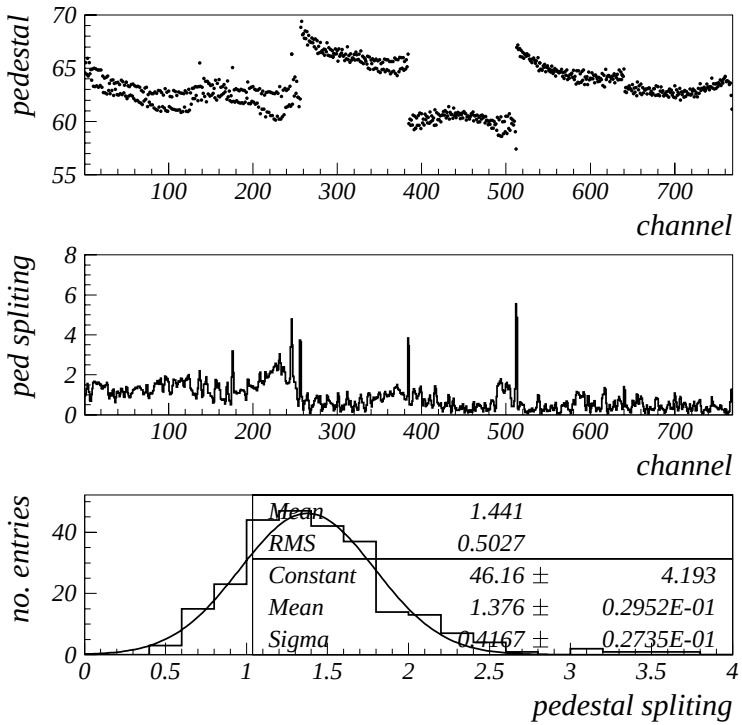
- Not so clear

Pipeline dependence (1-2-3)

depth=8



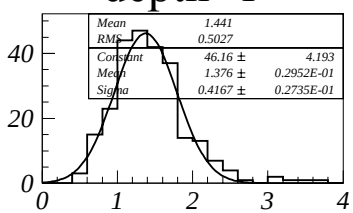
depth=1



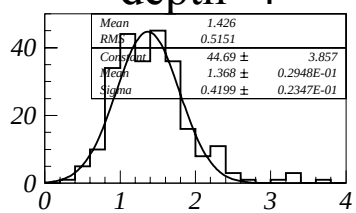
Pipeline dependence – cont'd

module 1

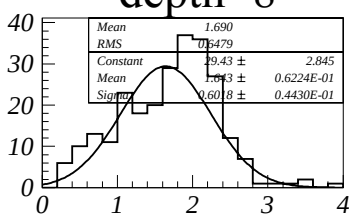
depth=1



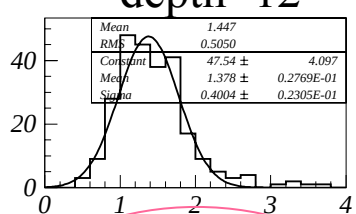
depth=4



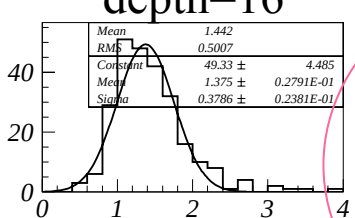
depth=8

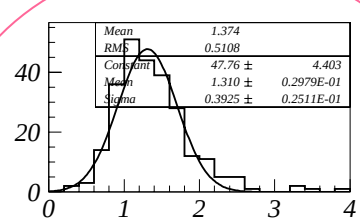


depth=12



depth=16

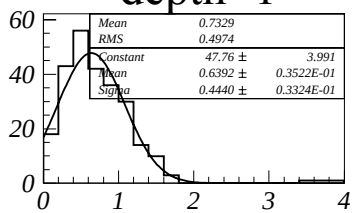




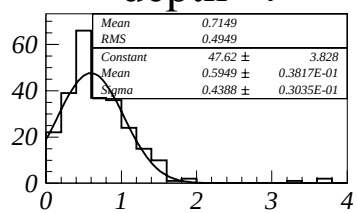
depth=8, but cal_sr timing moved to depth=4

module 2

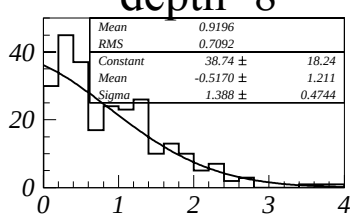
depth=1



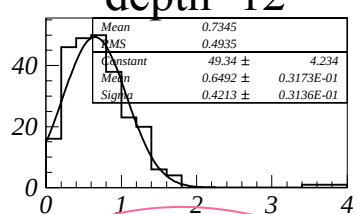
depth=4



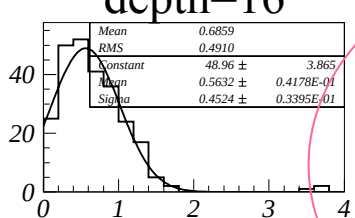
depth=8

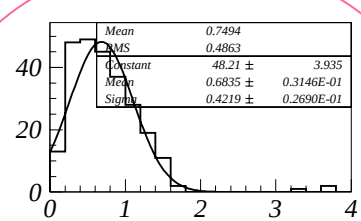


depth=12



depth=16





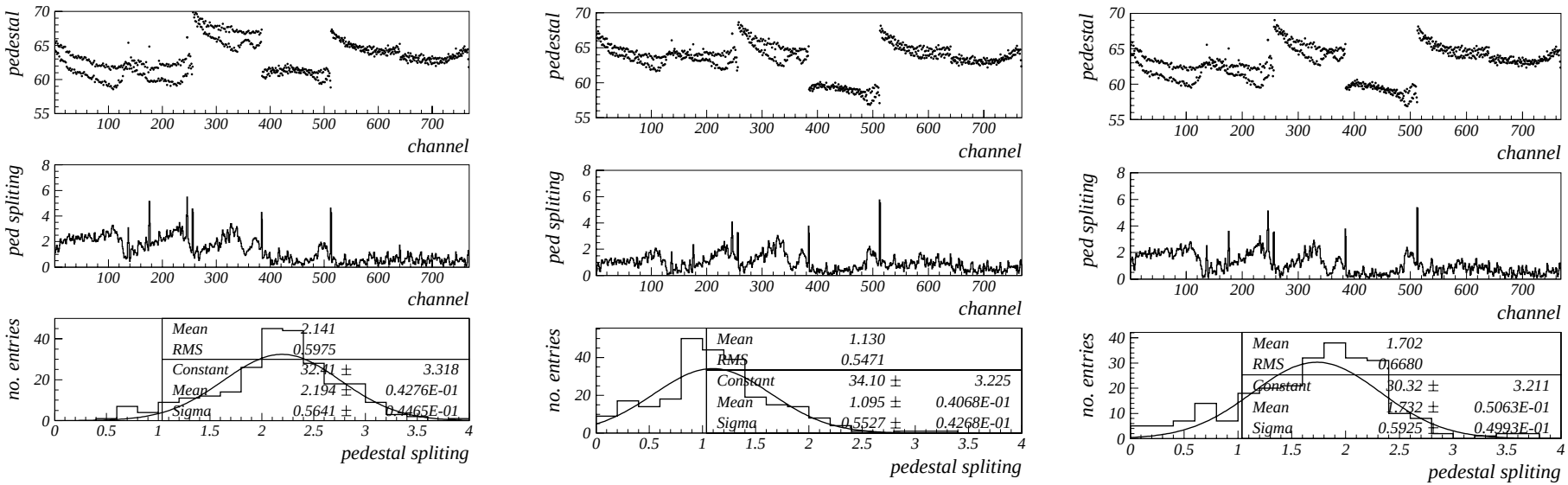
depth=8, but cal_sr timing moved to depth=4

- Cal_sr coincides with pipeline depth = 8
- Clear dependence ➔ cal_sr is one of the sources

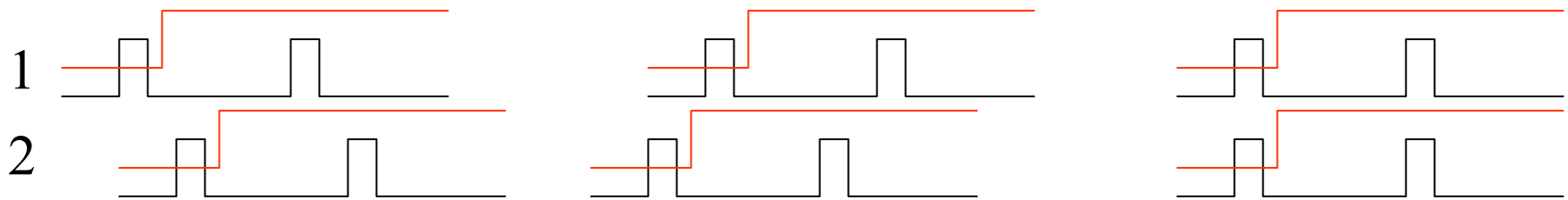
Longer jumper cables (1-2-3)

extra jumper cable (1m long) is added

to module1 | to module2 | to module1and 2

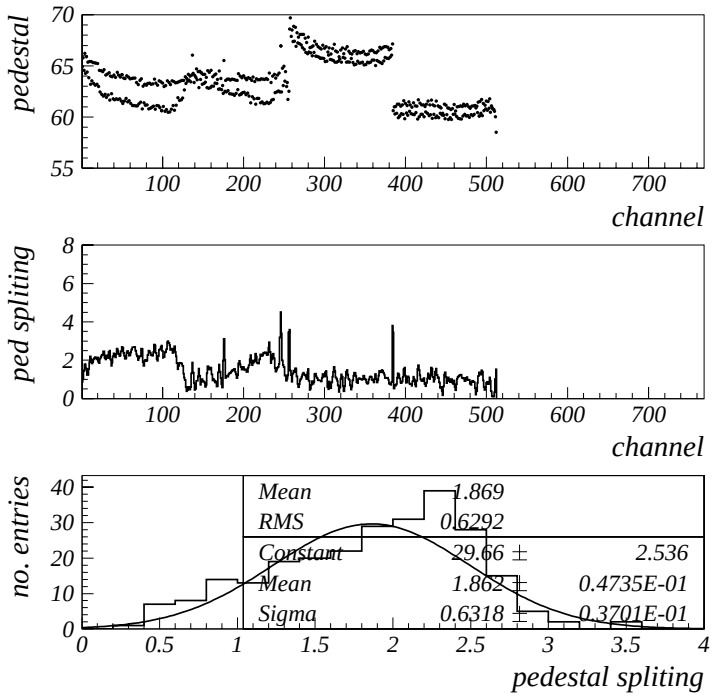


- no dependence on the clock amplitude
- confirmed cal_sr from neighbor is the culprit

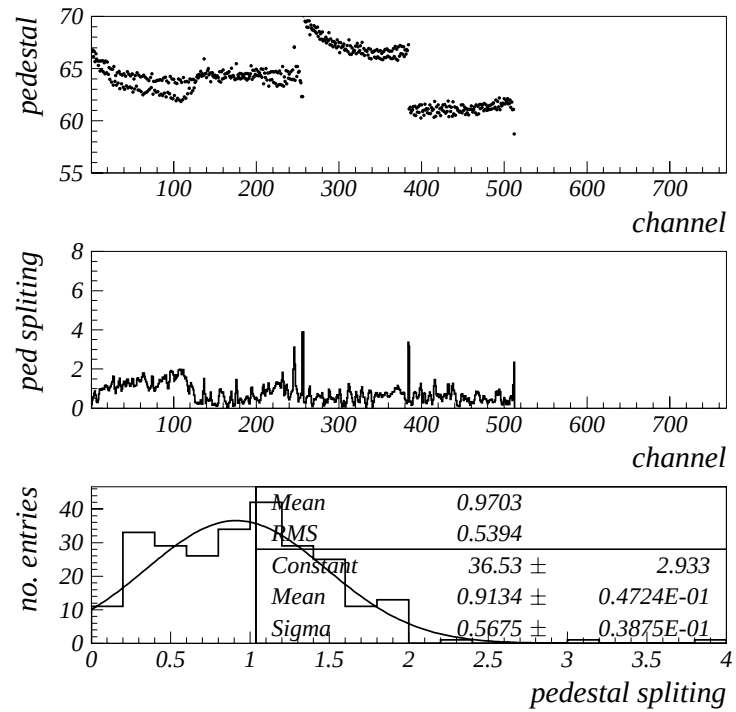


Another timing (?) effect (1-2)

module 1 and 2 read out by the same SASEQ



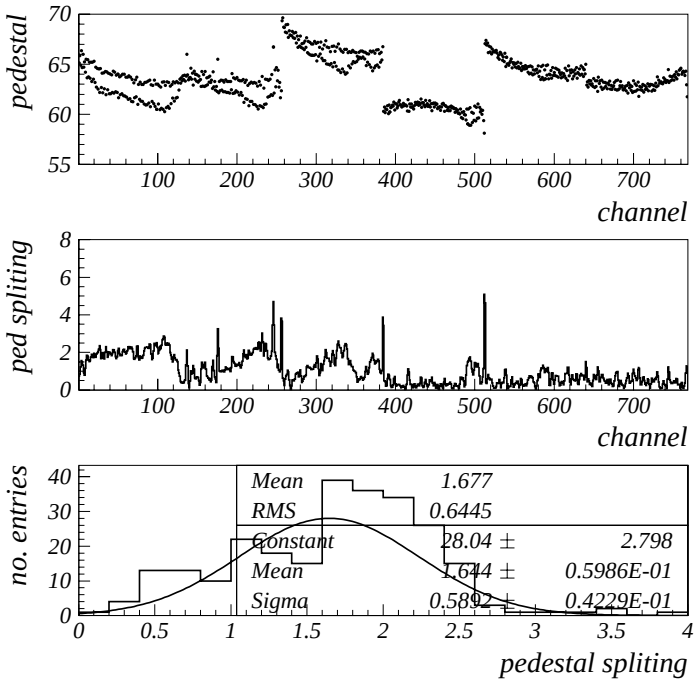
module 1 and 2 read out by the different SASEQ



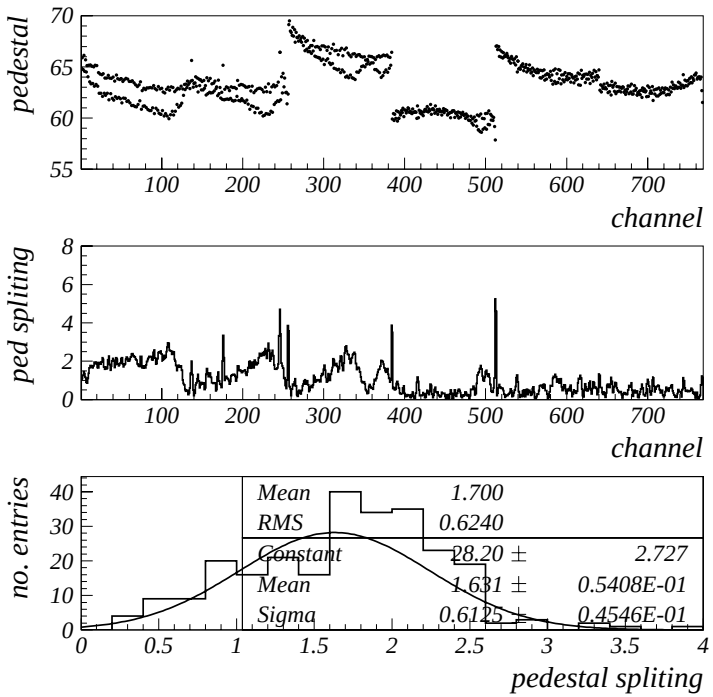
- Pedestal splitting is small when module 1 and 2 are read out by different SASEQ ➔ another evidence of contribution from neighbor's cal_sr (the size is consistent with the plot in prev page)

Clock ?

default



40nF capacitor



- Put 40nF (?) capacitor across clock and clock-bar, suggested by Andrei, to slow down the risetime of clock ← confirmed by scope
- Effect cannot be seen

Summary

- pedestal splitting originally ~0.8 or 0.9 ADC counts
  - enhanced by another module, resulting in 2 ADC counts of splitting
- cal_sr activity in the digital jumper cable running on top of the module (or chip) is one of the sources of pedestal splitting
  - module with the analog cable closer to the support structure has more contribution
  - slower risetime helps to reduce the splitting
  - splitting goes to ~1 ADC counts by reading out different SASEQ or using different timing
- Still another small effect
- Don't see the effect of clock so far