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Introduction

The AFE (Analog Front End) board uses numerous DAC channels to provide control voltages for the SIFT chip and control of the VLPC photodiodes. A large analog mux provides a feedback path by which the DAC outputs and other analog voltages may be monitored by the on-board microprocessor. Following reviews of the AFE design and using new information gleaned from tests on the MCM Test Board, the channel mapping and control interface has changed. This document describes the new setup.

Bus Structure and Control from 1553 bus

Each of the eight multi-chip modules (MCMs) on the AFE has an octal 8-bit DAC associated with it. Each DAC is controlled by a two-wire serial bus. Up to four octal DACs can coexist on a single serial bus. An analog switch is used with the microprocessor so that the serial bus lines are switched between serial bus 'A', which controls the DACs for MCMs 1 through 4, and serial bus 'B', which controls DACs 5-8. Firmware within the microprocessor takes demand values stored in a dual-port RAM from the experiment-wide 1553 bus, and upon command, downloads the demand values into the DACs.

Demand values for the DACs take the form of a sixteen bit data value which is bitmapped as shown in Figure 1.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
tag	N/A	Channel address						Demand Value							

Figure 1

The user's software loads a list of demand values into the dual-port RAM beginning at address 0. Sixty-four locations are reserved for DAC demand values, one per DAC output. Not all locations need be filled. Upon receipt of the command to update the DACs, the firmware starts processing demand values starting at address zero. Each value read is checked to determine if the tag bit (bit 15) is set. If bit 15 is '1', then the new demand value is stored in the channel address specified. If the tag bit is not set, the firmware interprets this as 'end of list' and goes back to normal command processing. The word with the tag bit cleared is not processed. Each new DAC value takes effect as the data values are processed, with a typical response time of 450 microseconds per value; this allows the entire board to be initialized in less than 30 milliseconds.

The channel address is linearly mapped into the board; bits 13,12 and 11 are interpreted as 'which MCM' and bits 10, 9 and 8 are the 'channel of that MCM'. The detailed breakdown for one MCM follows.

DAC Channel Map for one MCM.

Each MCM has eight DAC channels associated with it. The map of channels is as given in Table 1.

Channel Number	Function
0	VLPC Bias Drive Demand. An eight-bit value corresponding to 0-10 volts.
1	Heater Drive Demand. An eight-bit value corresponding to 0-10 volts.
2	VREF Demand. An eight-bit value corresponding to 0-5 volts.
3	QTHRESHA Demand. An eight-bit value corresponding to 0-5 volts. External op-amps create a 2.5V – 5V and a 2.5V – 0V voltage pair from this to set the threshold as a 0-5 volt differential centered around 2.5 volts.
4	QTHRESHB Demand. Same as QTHRESHA, but for the other 2 SIFTs in the MCM.
5	DRA Demand. Eight bits corresponding to 0-5 volts.
6	DRB Demand. Eight bits corresponding to 0-5 volts.
7	Spare. Brought out to a test point.

Table 1

ADC Channel Map for one MCM

Analogous to the DAC mapping, the internal slow A/D converter of the microprocessor may select one of sixty-four analog signals to read back. Some of the A/D values are direct readback of the DAC settings, whereas others are not directly connected to the DACs but instead read back signals affected by the DAC settings.

Channel Number	Function
0	Bias Readback. Reads the actual voltage driven to the VLPCs after the buffer amplifier in response to the VLPC Bias Drive Demand DAC setting.
1	Temperature Sense. Reads a voltage which is the voltage developed across the temperature sensor resistor in the cryostat as driven by a 10 uA constant current source. Since the voltage so developed is expected to be small, a buffer amplifier is inserted between the resistor and the A/D with a nominal gain of 19.297.
2	Direct readback of DAC VREF voltage.
3	Direct readback of DAC QTHRESHA output (0-5V, not the differential driven to the MCM)
4	Direct readback of DAC QTHRESHB output (0-5V, not the differential driven to the MCM)
5	Direct readback of DRA voltage.
6	Direct readback of DRB voltage
7	VLPC Bias Current readback. The current drawn in the VLPC bias supply, dropped across a 1.0K resistor, and buffered by an amplifier with a gain of 1000, for a nominal resolution of about 20 nA per count.

Serial Bus Control Protocol

Each half of the AFE board is one serial bus. The four octal DACs within a board half are allocated addresses 0x50, 0x52, 0x54 and 0x56. The four analog multiplexers are allocated addresses 0x90, 0x92, 0x94 and 0x96. Serial addressing of the analog multiplexers selects one signal from each of the eight MCM blocks on the AFE board; a different analog multiplexer is used to select which MCM's analog feedback signal is actually routed to the A/D converter.

Both the DACs and the first rank of analog muxes use the SMBus protocol in which two data lines – SDA and SCL – are used to transfer control information. When not being used, both lines are held high. Use of the serial bus down near the MCM's minimizes noise coupled from the microprocessor data bus.