**Fermilab**D0Note ##**The Central PreShower  
in the  
Axial CFT Trigger***by Fred Borcharding*

*This note addresses adding the Central Preshower, CPS, to the axial CFT L1 trigger. The present specification for the CFT trigger output calls for a six deep buffer containing the addresses for the highest Pt tracks found in each sector. The Upgrade trigger group has asked that a bit be added to each of these track words indicating when a corresponding CPS cluster is found. The first part of the note discusses how the preshower information might be combined with the CFT information to form an electron trigger. The second part discusses how two of the options described in the first part might be implemented in hardware. Included in this discussion are the results of simulations for the FPGA operation.*

**Introduction**

The CPS has 7680 total channels in 3 layers of triangular cross section scintillators. Two of the layers are stereo and the third is axial and all three layers are split at  $z = 0$ . Each of the layers has 2560 channels which are input into VLPC channels in the same cassettes used by the CFT. The output of the CPS is divided into the same 80 sectors as the CFT which gives 32 CPS channels per sector per layer. The single axial layer is input into the trigger by putting these 32 channels into the CFT trigger FE board for that sector. One of the stereo layers, 32 channels which are not used in the CPS trigger, are input into the stereo board for that sector. The other stereo layer is put into a separate group of VLPC cassettes that have FPS-FE boards. Each of these FPS-FE boards has 512 input channels that are each split into the two ranges. The resulting 1024 signals are input into 16 MCM's on each of 5 FPS-FE boards.

The extra 32 CPS stereo channels per FE board are in addition to the 480 channels per FE board for the stereo CFT, therefore, each stereo FE board has a total input channel count of 512. But, each of the CPS channels has its signal

divided on the FE board and input into two digitization channels for a x1 and x8 relative gain. Therefore, there are 544 electronics channels per FE board. Each MCM has 72 channels, so 7 are needed for the CFT. An 8<sup>th</sup> is used for the CPS. Each MCM has two threshold sets so that the x1 and x8 can have different thresholds.

The axial layer also has 32 inputs per FE board (sector) for an input channel count of 480 CFT + 32 CPS = 512 channels. Again the CPS inputs are split for dual gain which increases the digitization channel count to 544.

The CPS scintillators are triangular in cross section with a base of 7 mm. The mean radius of the CPS detector is 720 mm so each scintillator subtends about 7mm/720mm = 9.7 mrad. The outer CFT layer is about 1mm/550mm = 1.8 mrad. So a track through any given outer CFT layer bin points well inside one CPS bin. The CPS sector is 8 channels wide, and the CFT outer layer is 44 channels wide. MC results show that the CPS bin with the maximum pulse height is within 4.9 mrad RMS of the CFT track[1]. That width is about ½ of a CPS bin. Therefore we should be able to bin the CPS scintillators together into overlapping groups of 2 and define an electron as a CFT track in coincidence with a CPS bin above threshold:

$$EI = \{ \text{CFT Track} \} \text{ AND } \{ \text{CPS}[\text{bin}_k] \text{ OR } \text{CPS}[\text{bin}_{k+1}] \}$$

CFT inner bin offset	Pt	CPS Bin offset	OR Bins
1	21.0	0.2	0,1
2	10.5	0.5	0,1
3	7.0	0.7	0,1
4	5.3	1.0	1,2
5	4.2	1.2	1,2
6	3.5	1.5	1,2
7	3.0	1.7	1,2
8	2.6	2.0	2,3
9	2.3	2.2	2,3
10	2.1	2.5	2,3
11	1.9	2.7	2,3
12	1.8	3.0	3,4
13	1.6	3.2	3,4
14	1.5	3.5	3,4
15	1.4	3.7	3,4

This table calculates which CPS bin offset would be used with various CFT A layer bin offsets when the anchor layer is the H layer.

## Forming the CPS Trigger

### *Option 1*

There are several places in the calculation of the tracking trigger where the calculation of the PS trigger could be inserted. The first place, call this option

1, is right after the 8-fold equations are calculated. *Familiarity with D0 Note 3082 would be useful for understanding the following discussion*[2]. At that point we have terms of the form

$$T1013172227323945$$

but we have a large number of them. For a 1.5 GeV threshold we have over 12,000. At that point we could add terms of the form;

$$PS1013172227323945_{17} = \\ T1013172227323945 \text{ AND}(PS_{in}[17] \text{ OR } PS_{out}[17] )$$

where PS\_in and PS\_out are the channel numbers which are on the projected CFT track and the OR of the  $z > 0$  channel and the  $z < 0$  channel. This would give the most rejection of fake tracks, but it would also give the most extra terms. Only a detailed MC study could tell us if this is necessary.

### ***Option 2***

In the step after the equation finder in the CFT trigger algorithm the thousands of terms are OR'ed together into terms that share A layer and H layer bins. These terms are of the form;

$$T\_A10H45$$

We could form the CPS trigger here with terms of the form;

$$PS\_A10H45 = T\_A10H45 \text{ AND } ( PS_{in}[17] \text{ OR } PS_{out}[17] )$$

Call this option 2. For each sector there would be up to (44 in H x ~26 in A) 1144 of these terms. Forming the CPS trigger here in the form shown is mathematically identical to forming it in the previous step when there are no multiple tracks present. Therefore only MC studies could tell us what is gained by forming the trigger as in option 1 as opposed to option 2.

### ***Option 3***

There is a final place the CPS trigger could be formed, call this option 3. After the Pt versus phi terms in the above step are formed they are scanned in Pt order and the first 6 track candidates are loaded into a buffer. The information from this buffer could then be combined with the CPS information. Also the information could be combined within the hardware which created the buffer or in a following piece of hardware. This is in fact the method that muon will use to combine the CFT information with the muon hits. The information here is equivalent to that in option 2 above and therefore has the same weaknesses. It has the strong advantage however that it could use the least resources and, this is notable, it would be decoupled from the CFT algorithm. The CPS tracks could be found outside the hardware used for the CFT and thus

would be independent of changes in that algorithm or hardware. Also this option allows the sending of the track lists, sans the CPS information, at the earliest possible time.

## Hardware Designs

### *Option 2*

As was shown above for option 2 the set of CFT triggers from the base line design would be duplicated for a second set of CPS triggers. The effect is to more than double the resources needed to transform the results of the track finding equations into a list of tracks with Pt and Phi information. This is a doubling of a part of the problem that takes from 30% to 50% of the resources in the PLD's.

### *Option 3*

To explore this option we had to make several assumptions. The complexity of the track finder logic is very dependent upon the coarseness or road width of the information from the CFT track finder. We assumed one fiber wide road resolution from the CFT at both the inner and outer layers. Note that this fine of a road resolution is not available from the current base line CFT design. This fine of a road resolution in matching the CFT to the CPS gives an upper limit on the number of equations required and thus the complexity of the logic. About 700 CPS equations are needed to implement this road resolution. We had no MC information to guide us and suspect that with such information we may be able to relax the requirements on the CPS track finder. We do not think that MC studies will indicate that more stringent requirements are needed. Therefore the design described below is most likely a maximal design. How much it can be scaled back in hardware and cost can only be determined after specific MC studies.

Figure 1 shows a schematic of the hardware used and the flow of data for option 3. The CFT tracks come from the CFT track finder loaded into a six deep buffer formatted with the address for each track. First the CFT buffered tracks must be translated from an address to fiber bins. The phi address is de-multiplexed into the outer fiber layer bin and the Pt offset is de-multiplexed into the inner fiber layer offset. This information, up to 44 traces for the h layer, and 16 traces for the offset are then input into the CPS track finder. This number of bins corresponds to the maximum resolution likely to be available from the CFT track finder.

The CPS information comes directly from the data transfer registers where the trigger outputs for the CPS north and south ends have already been OR'ed together. The operation of these registers is described in a separate note[3]. The input information consists of the axial strips for the home sector, 8 for the inner and 8 for the outer, and two strips each for the inner next neighbor, the outer next neighbor, the inner previous neighbor, and the outer next neighbor. The total input count is 24. Restricting the neighbor strips to two limits the low Pt cut off to between 3 and 5 GeV.[3]

The CPS information must be matched separately to each of the six CFT tracks. One way to do this would be to use six sets of equations, one for each CFT track. Another would be to use the equations to match the CPS information to the first CFT track, output the results and then match the second, and so on for all six. The first parallel method requires six copies of the track equations in the FPGA, the second serial method requires that the time for each of the six operations be short enough so that all six can be finished within one crossing. Figures 1 and 2 show timing simulations of the logic. A new set of track inputs are given to each logic set every 50 nsec and the result is available on the output about 85ns later and remains stable for over 20ns. All six tracks can be processed by serially processing two tracks in each of 3 sets of parallel hardware. The logic is split into 3 parallel sections within which two tracks are matched in series for every crossing. As the CPS hit information for each CFT track is available the CPS hit bit is set. The new modified track buffer is then ready for transmission to the rest of the trigger system. The total latency for this method is 50ns, the second track waiting to be matched, plus 85ns, the latency of the second track matching, which is a total of 135ns.

At this time the track isolation calculation can be made. If there is a CFT or CFT/CPS track in the home sector the appropriate of two lines to each of two neighbors is set to 1. The home sector then samples its input isolation lines from each of its neighbors. If these lines are 0 the isolation bit on the track word is set to 1. The computation involved is very small and should require less than 100 LC's. Each sector has 4 input lines, CFT and CFT/CPS from two neighbors, and 4 output lines. The minimum time needed to set and sample the results over the back plane is 30ns. The total latency is thus up to 165ns.

For this design the CPS track finder logic requires just over 1600 logic cells for each of the three copies which is 4800 LC's. Decoding each track only requires 75 LC's which is 225 total. The 24 CPS input bits need to be pipelined for less than 6 crossings, that gives  $24 \times 6 = 144$  registers or 144 LC's. The six CFT track words must also be buffered for one crossing, that gives  $6 \times 16 = 96$  LC's. The isolation logic is about 150 LC's. Adding this up gives a grand total of 5,450 LC's. An Altera 10k130 has about 7000 LC's and is projected to cost about \$250 in '98.

This logic must be located on each FE trigger board. The amount of data for the CPS strips, 24 bits per sector, is small enough to be sent to a central location but such a transmission would require a second set of transmission hardware. The first set is the hardware to transmit the CFT track buffer. If it is located on the trigger board this logic can be inserted after the transmission of the CFT information to muon and before transmission to either the CFT L1 or any L2 preprocessor. Thus no hardware beyond that described above would be needed to add the CPS trigger to the CFT trigger.

## Summary

Several options were explored for adding the CPS information to the list of CFT found tracks. This addition in fact doubles the amount of information conveyed to the outside world so it is not surprising that it requires a significant

increase in resources. Adding the CPS information before the formation of the output buffer turned out to be very resource intensive and is not seen as feasible. Adding the CPS information after the CFT track buffer is formed is seen to be possible as far as the hardware needed. This note did not address the question of how much forming the trigger at this stage increases the number of fake electrons or its resulting utility.

Adding the CPS information to the CFT tracks after the CFT track buffer is formed is seen as having several advantages. First it is seen as doable. Second it de-couples the CPS from the CFT. Finally it can be added without delaying the CFT information to the muon system.

## References

- 1 - Brad Abbott, private communication.
- 2 - Fred Borcharding, 'L1 Axial CFT Trigger Hardware and Firmware Design for the Baseline Trigger Algorithm', *DONote 3082*, September 17, 1996.
- 3 - Manuel Martin, 'Routing of Signals for the 8 Layer Geometry SF Trigger and Preshower,' *DONote 3170*, January 20, 1997.

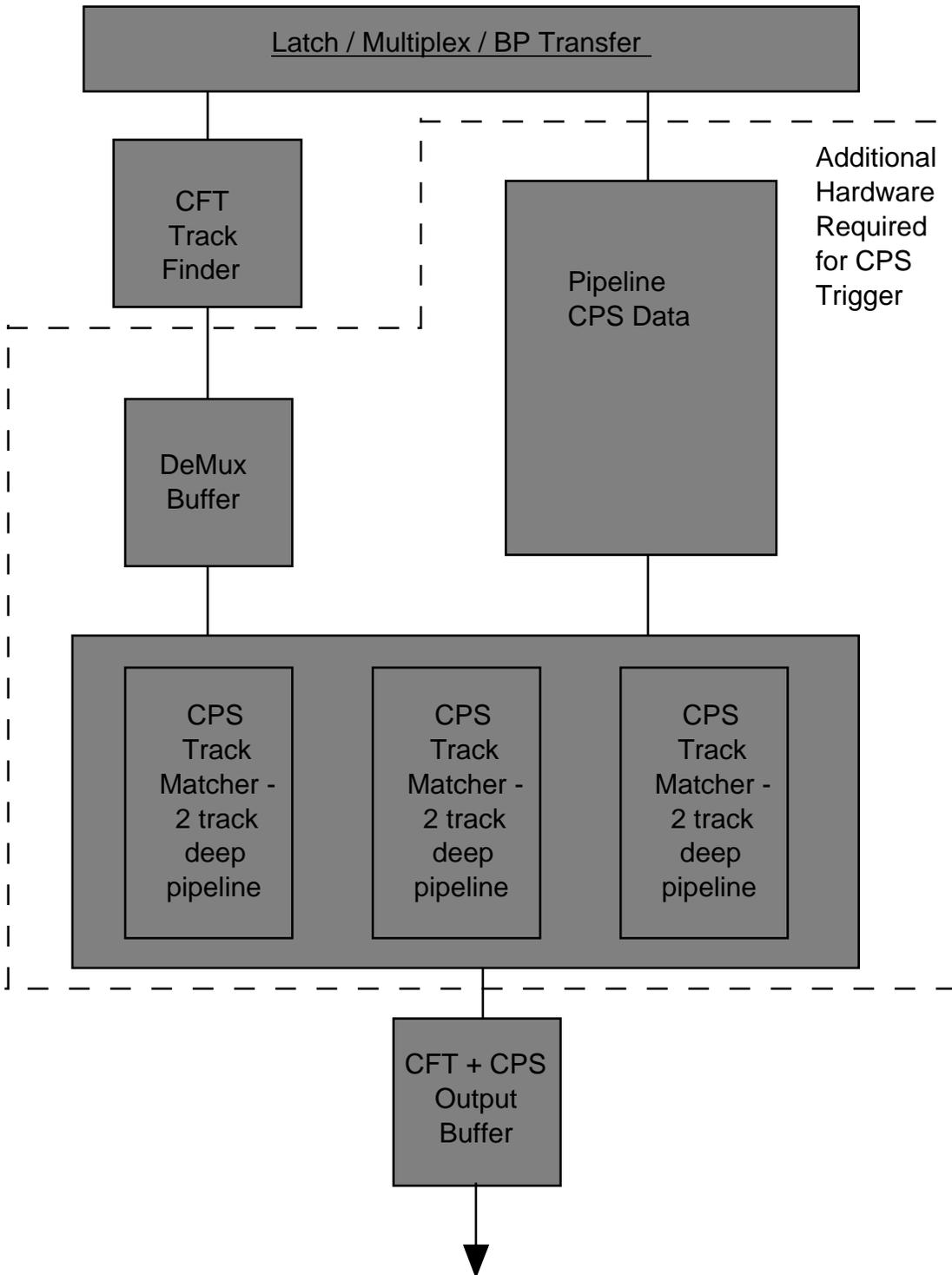


Figure 1 - Schematic of the data flow for the CPS trigger using Option 3. The raw north and south CPS data are OR'ed together in the Latch ... stage and then pipelined until the CFT information is available. The CFT track addresses are then de-muxed and combined with the CPS data. The output is the original CFT track address buffer with a bit set for each track which has a CPS match.

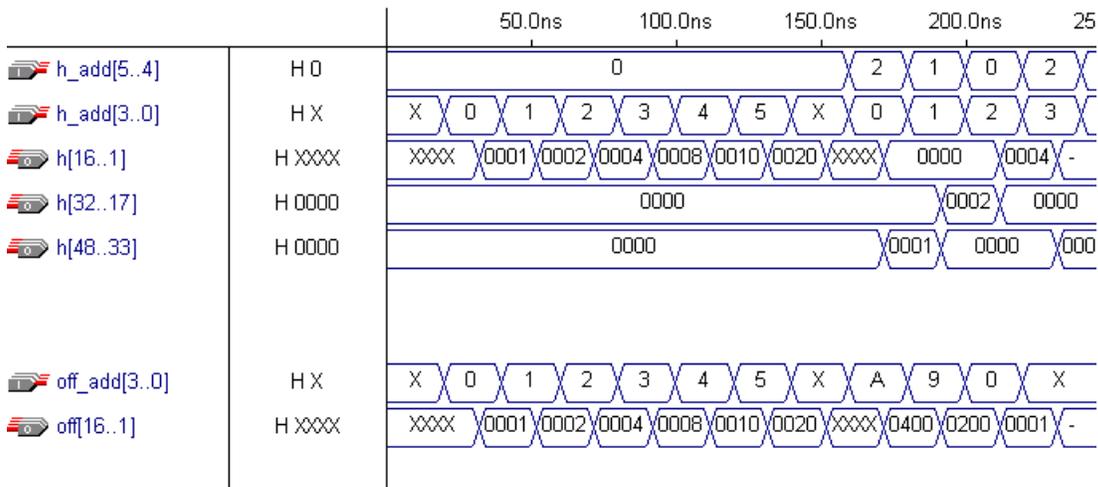


Figure 2 - Timing diagram from simulation for decoding the track word into outer fiber bin number and offset bin number. H\_add is the six bit phi address from the track word and h is the outer fiber bin array. Off\_add is the four bit Pt value from the track word and off is the Pt offset bin. In this simulation a new track word is input every 20ns and the decoded values are returned within 15ns. This design required 74 LC's.

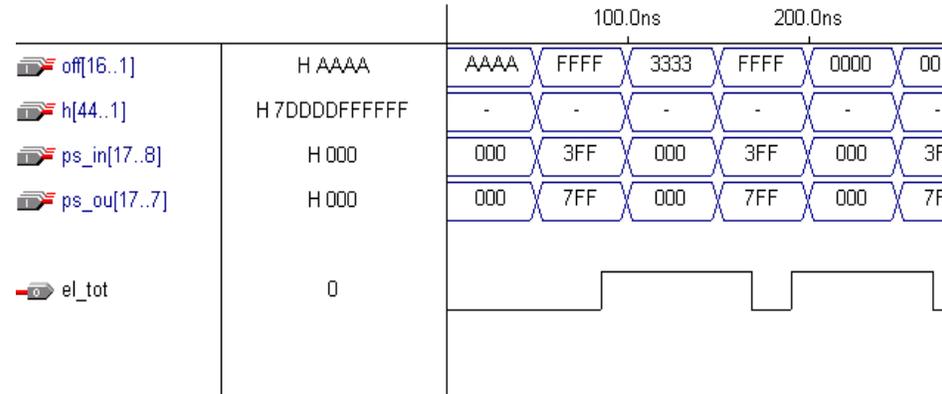


Figure 3 - Timing diagram from simulation for matching the CPS information to the CPS information. New data is presented every 50ns and the latency is 70ns. This design requires 1600 LC's.