

Fermilab

Testing the SIFT with the ADAPTER Board

by Fred Borcharding

We are testing the SIFT + SVX combination on a new test board. This board is based on the QPA-02 board which plugs into the 128 channel cryostat and was developed by the fiber group and used in the cosmic ray test. The new test board, called the ADAPTOR BOARD was developed by Mike Matulik. It holds two 16 channel SIFT chips for which all channels are bonded out. It also accepts an HDI containing two SVX chips. The HDI developed for the silicon tracker is glued onto the adapter board. The 16 SIFT analog output channels from each SIFT chip are bonded into 16 SVX channels. The 16 SVX channels are not in any particular order. The assembly of the test boards was supervised by Lynn Bagby and the testing has been done by Lynn and myself.

Figure 1 is an electronic drawing of the SIFT chip and the analog part of the SVC chip. The five switches on the SIFT chip are controlled by five clocks. CDS, S/H and READ are 3V levels, where high is closed and low is open. PRST and DRST are 5V signals, high is closed and low is open. V-Dr is the dynamic range adjustment of the preamp and was run at values from 2.5V to 3.5V. V-Th is the threshold voltage for the discriminator. V-Ref is the matching voltage for the SVX. Since the reference voltage of the SIFT is 0V and that of the SVX is about 1.95V an external reference voltage is required to avoid pumping unwanted charge into the SVX on each cycle. Figure 2 shows a drawing of the charge injection circuit that was used for these tests. A pulse from a voltage pulser was applied to a resistor pot which was adjust the range of the input signal. After the pot a resistor divider was used to greatly reduce the signal amplitude. The pulser typically supplied volts and the out of the divider as milivolts. After the divider the voltage input was coupled into the SIFT with a small capacitor. This change the voltage input into a charge input. This was done since the VLPC is a charge output device and the SIFT expects a charge input.

The operation of the clocks an hence the SIFT is shown in figure 3. The top drawing shows the clock signals for one 130 ns cycle the bottom for 4 cycles. The PRST and DRST are closed at the same time to reset both. The CDS switch is also closed as is the READ switch. The READ switch is closed to

transfer charge from the SIFT output capacitor into the SVX. Since the S/H switch is open this capacitor is isolated and drains into the SVX with some RC constant. This constant was measured in pace to be less than 10ns and is expected to be much less than 1 ns. The PRST is released first and the front end is allowed to settle. After the preamp has settled the closed CDS switch allows the external V-Ref to charge the 560ff capacitor to the reference voltage of the SVX. This switch is then closed. The DRST switch is also released some time after the PRST switch. The SIFT is now ready to accept and input charge. At the end of the cycle the S/H switch is closed to transfer the integrated charge from the preamp onto the output capacitor. This switch is then opened at the very end of one cycle which is also the start of the next. The nominal times for these clocks are given in figures 3 and 4. For some of the tests these times were varied and the text below or the figures should state which were varied.

We were able to get a discriminator threshold measurement. Figure 1 shows a threshold measurement made at 130ns cycle time and standard input values. Table 1 lists the standard values while figures xx-xx show the set up and figure xx shows the clock table set up. For the measurement shown in figure 1 we were able to measure the threshold behavior down to 5 fC of input charge. Figure 2 shows a blow up of the low input end. Input signals of 5 fC or less were turned off by a V-Th of 0.0V while a V-Th of 0.05V shut off inputs below 12 fC. The V-Th vs. Input curve becomes linear at about 45 fC and remains so until the V-Th approaches its rail of 4.75V. In this case the maximum Input signal which can be shut off is about 110 fC. The fit shown is for those points in the linear region. This fit shows an apparent negative pedestal on the threshold voltage.

When we went to a longer cycle time of 390ns we saw the threshold behavior change. Figure 3 shows a threshold scan at 390ns where the 130ns clock table was modified by inserting 260ns of all signals=0 after DRST and before SH. The threshold voltage for this case is a linear function of the input but has a large positive pedestal. This high pedestal results in a maximum threshold range of only 25 fC. But by lengthening the resets the pedestal can be reduced. Figure 4 shows a scan at 390ns but with the clock table shown in figure xx. Here the resets and other clock signals are increased to about twice their previous values. As a result the maximum threshold is 55 fC and the pedestal is consistent with 0V. Figure 5 shows a time scan of the threshold voltage for this clock table. The threshold is stable from shortly after the end of the DRST to within 60ns of the end of the cycle.

How reproducible are these results? Figures 6 and 7 show results taken on two different days. Figure 6 is a threshold scan at 130ns cycle time. The results are similar but not the same. Figure 7, however, which plots the analog input vs. the analog output to the SVX is very consistent.

In summary these results look very positive. It appears that we can operate the SIFT at a threshold range of 5 to 100 fC at both the 130 and 390ns cycle times. But the threshold behavior is still not completely understood. The results vary from day to day and measurement to measurement in a manner which is not understood. Noise is still a problem, and grounding still needs improvement.

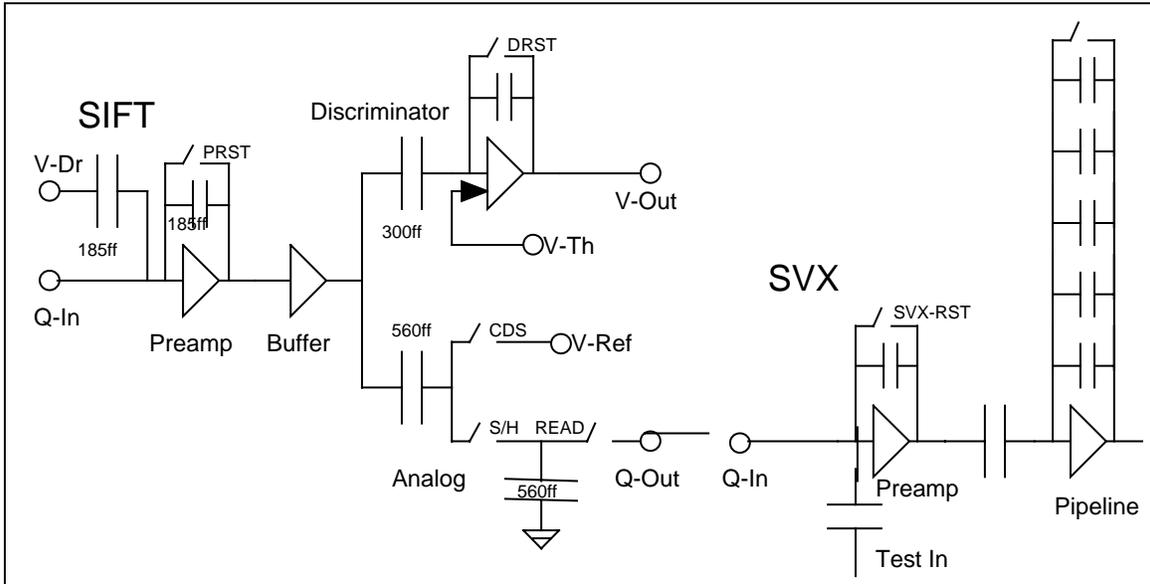


Figure xx. Schematic of SIFT chip connected to the SVX chip.

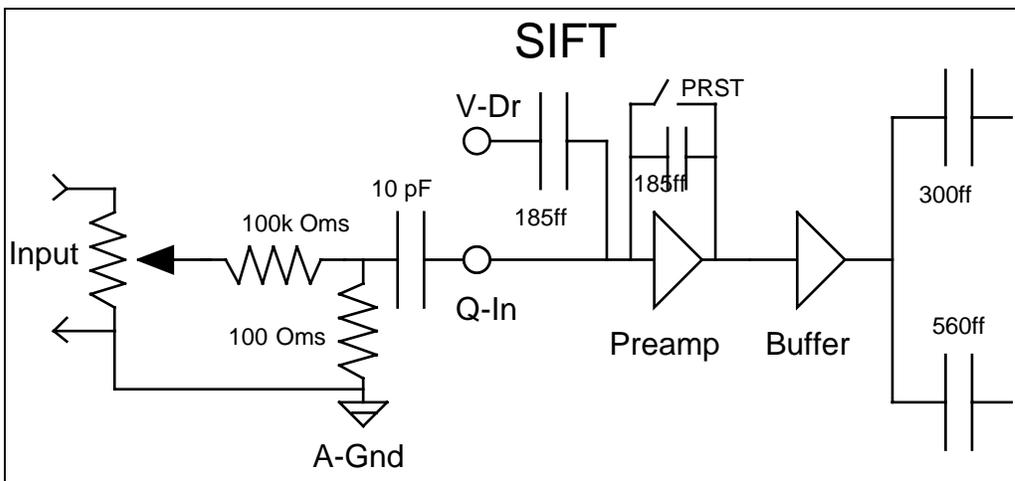


Figure xx. Pulse Input circuit for testing of SIFT chip.

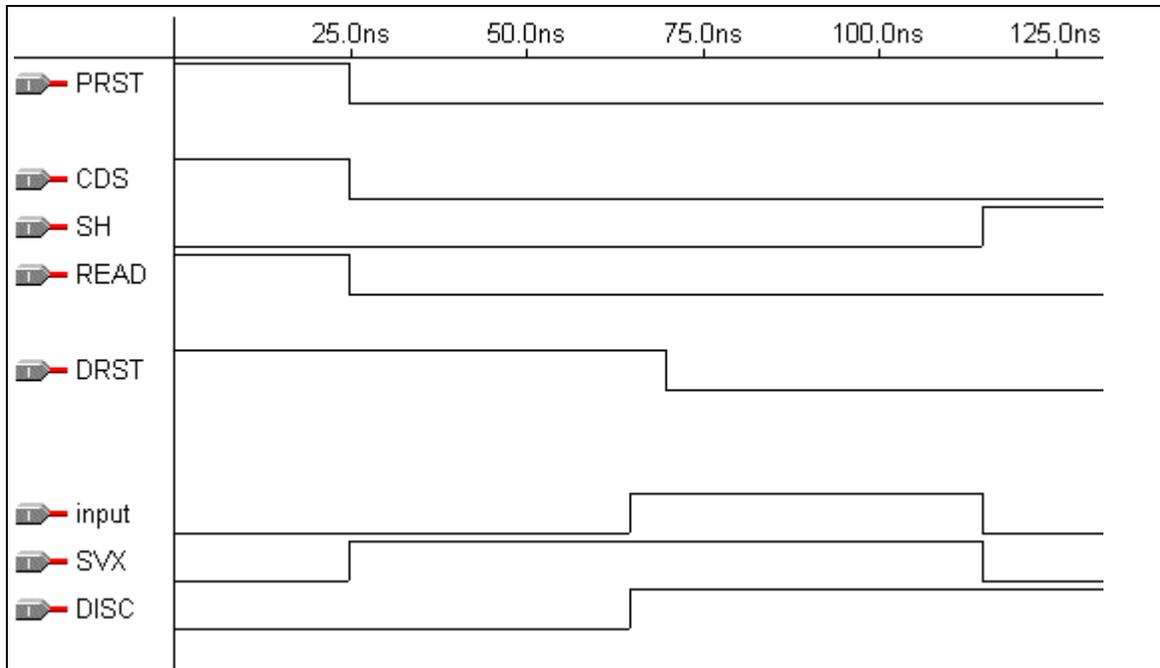


Figure xx: Clock table for 130ns cycle time.

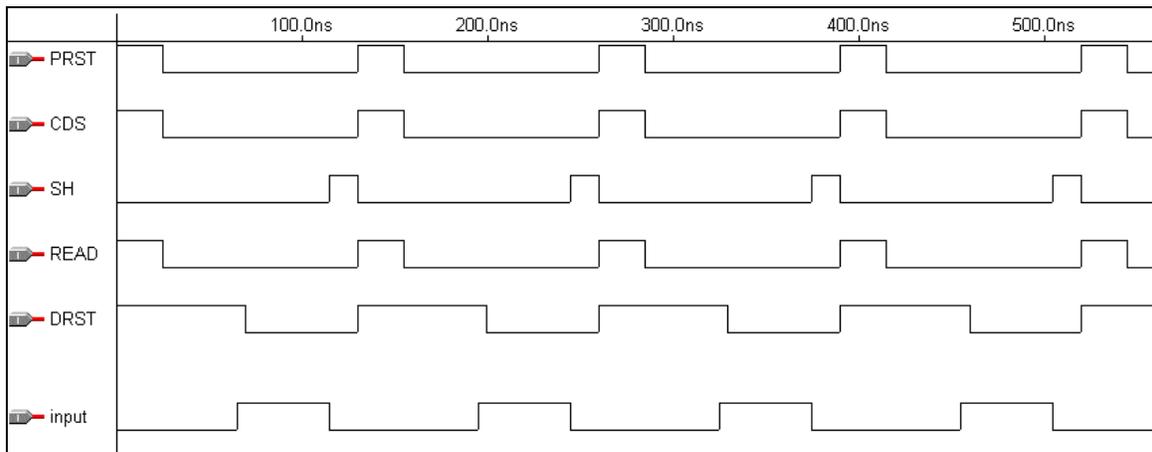


Figure xx: Clock table for 130ns cycle time showing 4 cycles.

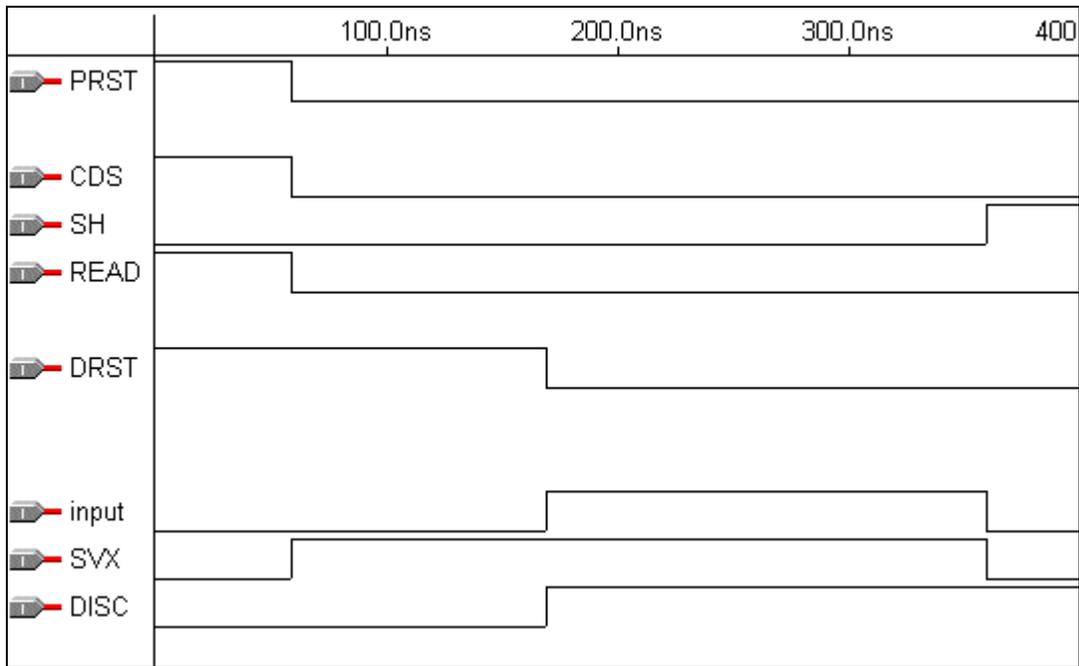


Figure 5: Clock table for 390 cycle time.

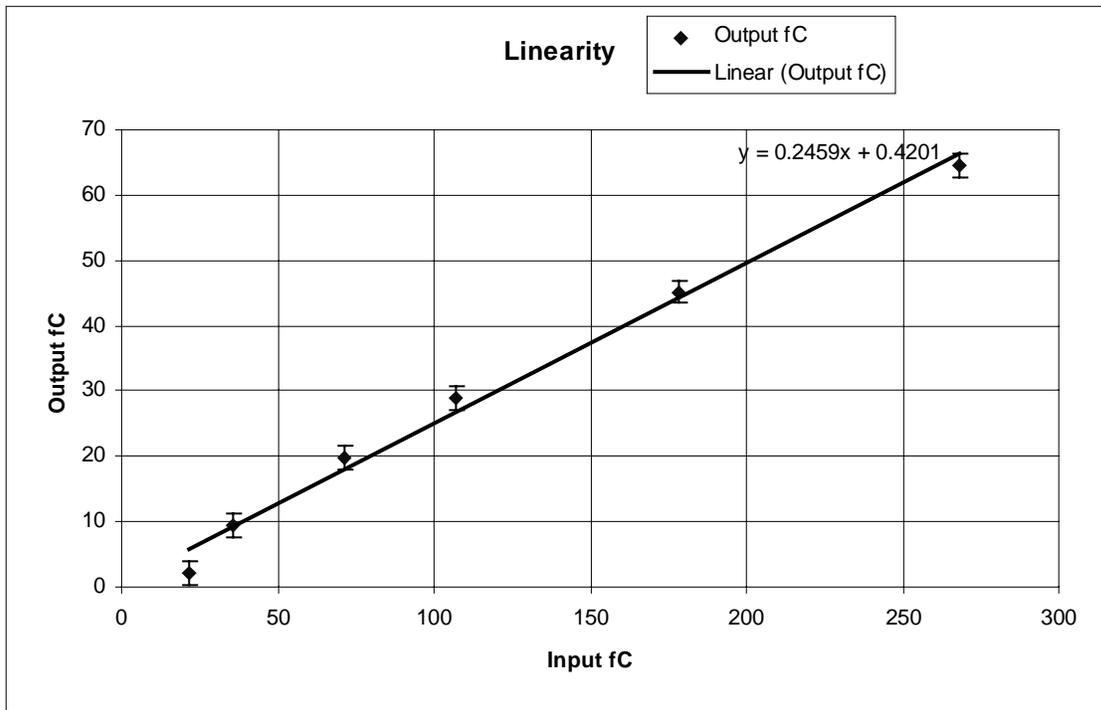


Figure xx. Data taken on August 20. This is our golden data. In the top plot the horizontal axis is the input charge in fC. The charge was calculated using the values of the input capacitance and resistance and by measuring the input voltage. The vertical axis is the charge in fC seen by the SVX. The calibration of the SVX output counts to fC input is used to establish this axis. The slope of this line gives the measured value of the SIFT gain. Here it is 0.25.

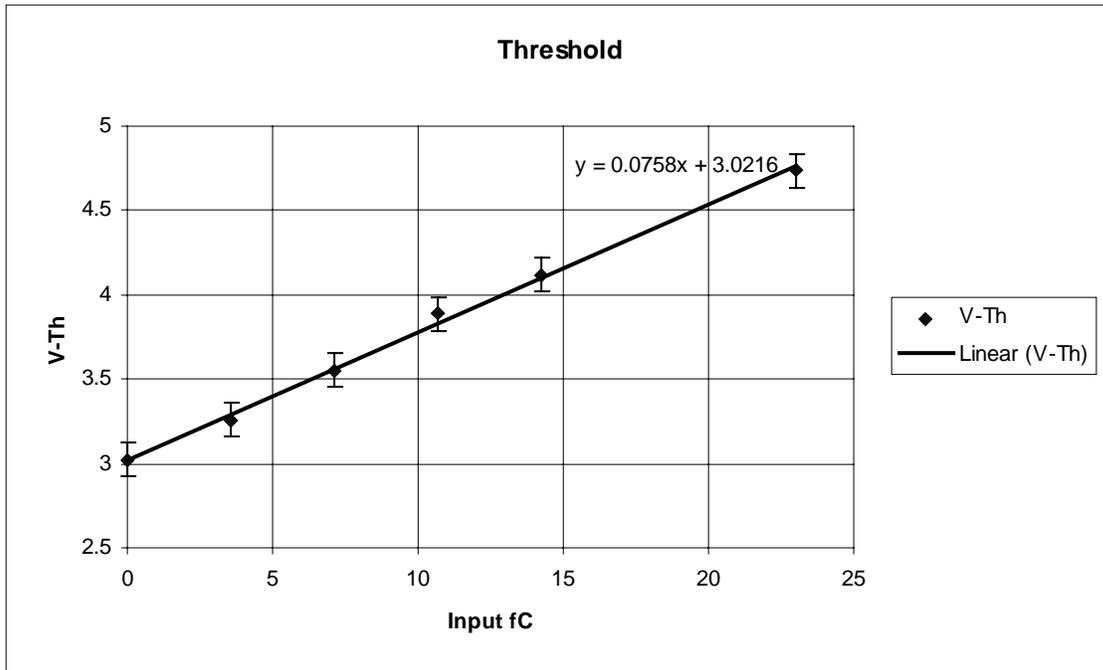


Figure xx. Data taken on August 20. The horizontal axis is the input charge determined as above. The vertical axis is the threshold voltage at which an output voltage pulse is present at full amplitude (3V). The width of the pulse is about 5ns and the efficiency discriminator is not determined but could be as low as 50%. A threshold voltage setting of 3V is required to turn off the discriminator with zero input charge. At the maximum possible value of the threshold voltage the discriminator level is about 23 fC. The slope is 0.076 fC per volt.