

# Links from CFT (CPS) Concentrators to L2pp

This document covers the transmission of data over the fast serial links from the Broadcast Crates to the L2pp for three(four) systems:

CFT/CPS axial trigger	to	STTpp & CFTpp
CFT/CPS axial trigger	to	PSpp
FPS & CPS axial	to	PSpp
(FPD)	to	(FPDpp)

and applies equally to all three (four) links except where noted.

### **Link Activity**

The states of the links are:

Idle.... DATA-for-one-event.... Idle....DATA-for-one-event....

where Idle is a link defined state in which no information is sent and fills in the entire time between data transmissions.

### **Data Block Format**

The data block format for each event consists of two frames of header followed by N frames of Data, and ending with an End-of-Record frame:

Header Frame 1
Header Frame 2
Data Frame 1
Data Frame 2
.....
Data Frame N
End-of-Record Frame

where N changes from event to event but has a maximum value set for each link. Each link has two lines (bits) which are members of the link control set, are not seen as part of the data, and control the data block transmission. The transmitter for the link must set these lines(bits) and the receiver must interpret them. The first is the FLAG line (bit). A FLAG = 0 value indicates that the information in the data block is header or data frame, while a FLAG = 1 value indicates that the transmitted frame is the End-of-Record frame.

The second is the CONTROL line (bit). A CONTROL =1 vaule indicates that the frame being transmitted is a control frame.

The CONTROL frames are reserved for use in either of two purposes. Either they can be used by the sender/receiver pair to indicate a diagnostic frame is being sent. Or they can be used by the pair to indicate that a second type of data is being transmitted when two different types of data are sent over the same link to multiple recievers. For example if CPS clusters are appended at the end of CFT tracks then the control line could be used to indicate the CPS data frames. As another example if the STTpp only wanted 32 tracks and CFTpp in parellel wanted 64 then the CONTROL line could be used to indicate the frames for tracks 33 through 64.

**FRAME**

Each frame is  
 16 or 20 bits wide per 53MHz clock tick, and  
 the width is set by a command from the HOST for each link.

**Each Frame**

The format of each frame is as shown below. The bit order is from left to right, that is the msb is on the left, the lsb is on the right, and each box represents 4 bits. Five boxes are shown representing 20 bit mode, for 16 bit mode the left hand box is absent.

**Header Frames**

Frame 1

Spare	Link ID	Status	Crossing	Crossing
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The link ID is used to identify the link, and the status is used to pass informaion about the formation of this data block on to the preprocessor. The crossing is the 8 bit crossing number generated at the FE and is for use within the preprocessor.

Frame 2

Spare	Turn Number	Turn Number	Turn Number	Turn Number
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The turn number is the 16 bit turn number generated in the FE and is for use within the preprocessor.

**DATA Frames**

Frames 3 through N+2 are data and are composed as below. In 16bit mode the Spare/Data nibble is absent.

Frame 3 through N+2

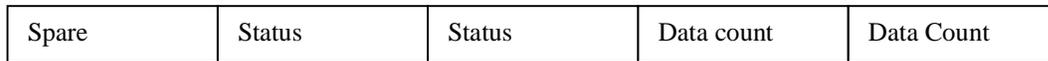
Spare / Data	Data	Data	Data	Data
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For the CFT/CPS axial trigger system the data bits include 15 bits for the combined phi and Pt values and up to 5 bits for flags. The flags include whether the CFT track is matched to a CPS cluster, whether it is isolated and so on. For the FPS the data bits will include the eta and phi values for each found track.

**End of Record Frame**

The End of Record Frame is inserted after the last valid data frame. As discussed above this frame is indicated to the receiver by the presence of the FLAG bit. The data count is an eight bit counter of the number of data frames transmitted, N. This count is intended for use by the preprocessor. However, this count could be used by the receiver for comparison to a counter of its own to recognize a transmission problem. The eight bits of Status can contain information about this event for use by the preprocessors.

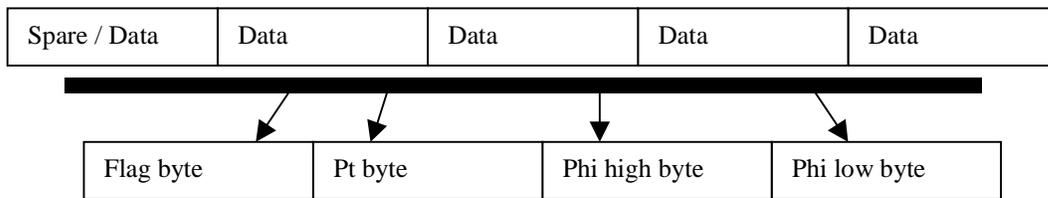
**End of Record Frame**



For the CFT/CPS axial trigger system the data count would be the number of tracks sent.

**FIC Functionality**

The 20(16) bits of DATA are mixed and matched within a PLD on the FIC from a bit-wise orientation to a byte-wise orientation. The 20 (or 16) bit input DATA frame is expanded into a 4 byte ( 32 bit word) output frame. In the output frame physics elements such as Pt, phi or eta are each integral bytes. The solid bar in the figure below represents the PLD function. The four output bytes, shown here for the CFT/CPS axial trigger system, are two for the phi value and one for the Pt value and one for the flag bits.



The orientation is most-significant-byte on the left to lsbyte on the right. The bits within each byte are arranged according to the bit-within-each-byte format of the ALPHA processor, whatever that may be.

A PLD is utilized to make the shift from bits to bytes so the each link can have its own bit pattern and/or byte pattern. A PLD does this very quickly and economically, plus a PLD can be programmed differently for the needs of different link types. The FIC could be manufactured with the footprint for a family of PLD's so that a small/inexpensive one could be mounted where little translation is needed or a larger/more-costly one could be mounted if a lot of translation is needed. If even more translation is foreseen a mezzanine board could replace the idea of a single PLD on the FIC.

