

Fermilab

Central Fiber Tracker Trigger

by Fred Borcharding

What must the fiber trigger do?

Identify real tracks within several Pt bins

Nominal thresholds of 10, 5, 3 & 1.5 GeV

Not be fooled in a high multiplicity environment into finding fake tracks

Do this for every crossing at both 396ns or 132 ns per crossing

Package the result and distribute on 500ns time scale

Muon results are needed in 500 to 700 ns

L1 concentrator needs results on same time scale

What does the fiber trigger output?

6 Highest Pt tracks from each of 80 Sectors

These are sent to Muon for L1 Muon + CFT Trigger

They are also sent to CFT L1 'Concentrator'

20 Highest Pt tracks globally

Used in L2 global

Found from 6 per sector in L1 Concentrator

List of tracks to SVT - 'still under study'

SVT needs CFT tracks as 'filter' as data arrives

SVT needs CFT tracks as seeds & lever arm as it finds tracks in the silicon tracker

Does this come from 80 FE sectors or concentrator?

What is the input to the fiber trigger?

480 'axial' fibers from the 'home' sector

The fiber tracker cylinders are divided into 80 Phi wedges called sectors

The electronics for each sector is on ONE FE board

368 axial fibers from 'next' and 'previous' sectors

For a 'seamless' trigger fibers from neighbor sectors are shared

32 axial scintillator strips from the CPS

Each CFT track is flagged if it has a corresponding CPS cluster

How does the CFT find tracks?

It is loaded with the 'equations' for all possible real tracks in the sector in the Pt range

44 Phi bins X 24 Pt bins X ~12 different routes = 12K equations

These equations are an 8 fold AND of all the fibers a particular real track would intercept

Has the flexibility to switch to 7 of 8

After it has found which equations are TRUE it;

SORTS to find the 6 highest Pt tracks

Assigns an address for the Phi 'bin' and Pt 'bin' for each track

What Hardware does the CFT Trigger use?

It uses FPGA's (Field Programmable Gate Arrays)

Can implement AND / OR logic with > 5K Logic Units

FE board hardware is as 'general' as possible

Algorithms and other details of the design are in the FPGA programming

High level languages available for programming

Can re-download different triggers for each run

Trigger can evolve with run

FPGAs are very fast

Problems are solved in parallel versus serial

Logic level latency is about 3-5 ns

Can operate with 53MHz clock

Commercial market is pushing the size up and the cost down

Proven 40% to 60% price reduction per year (same size chip)

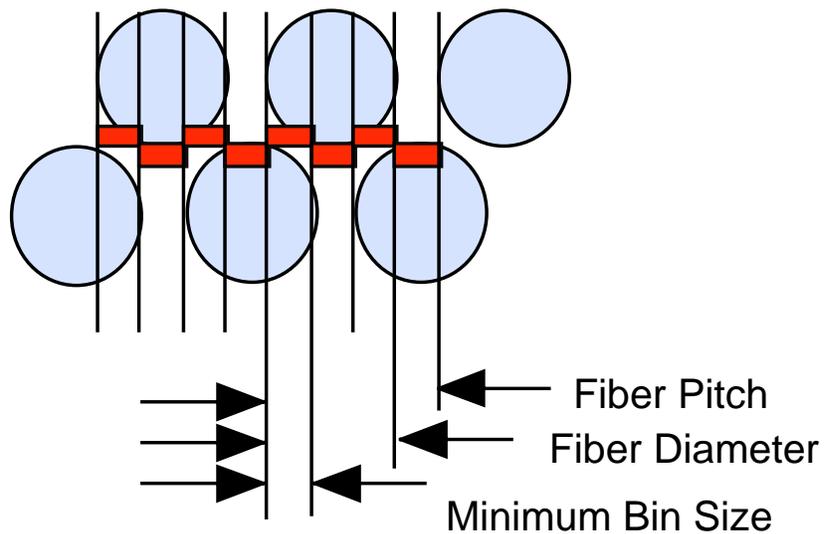
Metal process now at 0.5u soon 0.35u and then 0.25u ...

Tracker Geometry

Fibers Arranged in Doublet Layers

8 Doublet Layers are parallel to the beam - Axial Doublets

8 Doublet Layers are at stereo angles to beam - U & V Stereo

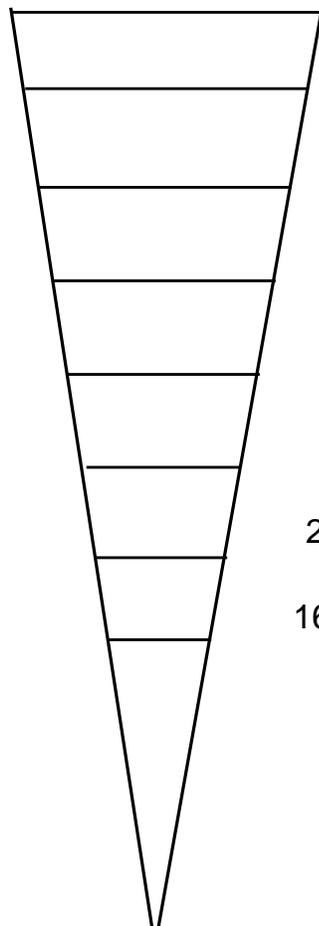
DL { doublet layer }**D0 β**

- Fiber Pitch \sim 1 mm

■ Fine Binning = Sum of 4 Minimum bins

Baseline Detector Fiber Arrangements for Trigger

H
G
F
E
D
C
B
A



44 = 11 x 4 @ ~55cm
 40 = 10 x 4 @ ~50cm
 36 = 9 x 4 @ ~45cm
 32 = 8 x 4 @ ~40cm
 28 = 7 x 4 @ ~35cm
 24 = 6 x 4 @ ~30cm
 20 = 5 x 4 @ ~25cm
 16 = 4 x 4 @ ~20cm

480 Fibers
 Total
 per sector
 into each board

One Sector
 80 sectors
 ea. 4.5 degrees

XU-XV 8 layer Base Line Detector with Equal Spacing between Axial Layers

775.0	60.0	835.0 um		Fiber active diameter, cladding diameter, Total diameter
128 fibers				Width of ribbons
80 sectors				Number of Sectors
0.0750 mm				Thickness of layer between Axial Doublet and Stereo C
1.5281 mm				Doublet thickness
190.000 mm		9.525	0.381 mm	Inside Stay Clear / End Ring / Cylinder Thickness
520.000 mm		2.54 mm		Outside Stay Clear / Connector Highth
0.250 mm				Gap between ribbons / Measured from fiber edge to fib

Layer	Radius mm	Number of Fibers per sector	Ribbons per layer	pitch microns	pit/active- diameter	number	Active Length meters	
A	199.9	16	1280	10.0	979.3	1.264	4	1.660
A-U	201.5	16	1280	10.0	987.2	1.274	4	1.660
B	249.0	20	1600	12.5	975.8	1.259	5	1.660
B-V	250.6	20	1600	12.5	982.1	1.267	5	1.660
C	298.0	24	1920	15.0	973.4	1.256	6	2.520
C-U	299.7	24	1920	15.0	978.6	1.263	6	2.520
D	347.1	28	2240	17.5	971.7	1.254	7	2.520
D-V	348.7	28	2240	17.5	976.2	1.260	7	2.520
E	396.2	32	2560	20.0	970.4	1.252	8	2.520
E-U	397.8	32	2560	20.0	974.4	1.257	8	2.520
F	445.3	36	2880	22.5	969.5	1.251	9	2.520
FV	446.9	36	2880	22.5	972.9	1.255	9	2.520
G	494.3	40	3200	25.0	968.7	1.250	10	2.520
G-U	495.9	40	3200	25.0	971.8	1.254	10	2.520
H	514.3	44	3520	27.5	916.1	1.182	11	2.520
H-V	515.9	44	3520	27.5	919.0	1.186	11	2.520
		960	76800	600.0				

FILE: Fiber
Last Modifi

The outer layer H/H-V is placed at the maximum radius possible.
 The next to outer layer G/G-U is placed as close to layer H as possible.
 The inner layer A/A-U is placed at the smallest radius possible.
 The other layers are placed to give equal separation between layers from A to G.
 An extra gap between fibers of a singlet layer is added between ribbons (see above).
 The fiber Pitch = (circumference) / (number of fibers per layer). The circumference = 2piR - (the num

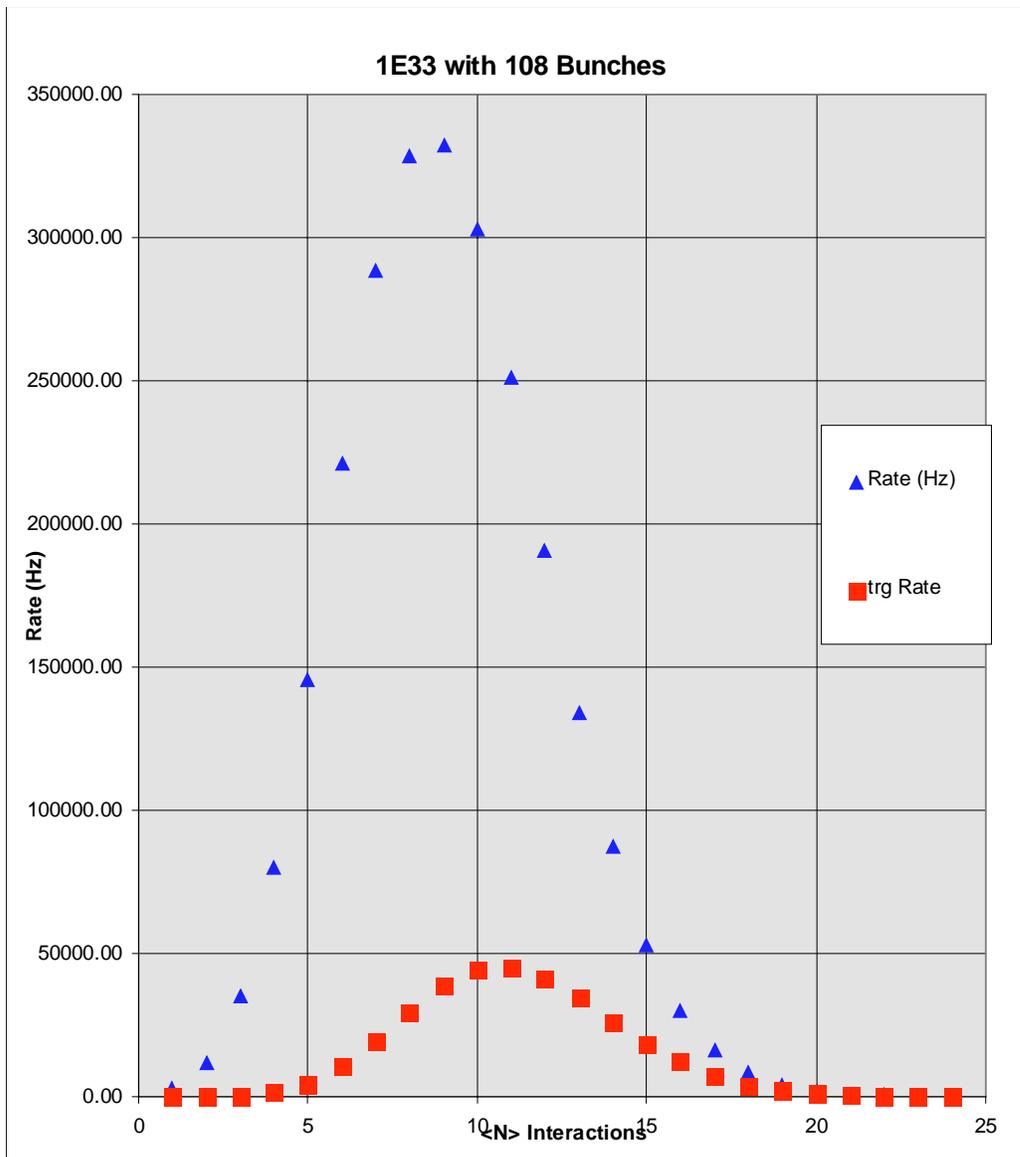
Occupancy

Luminosity	crossings	<int>/cross	<occ>/cross	Inner Layer	Outer Layer
8.00E+31	6	13.12		52.50%	19.69%
2.00E+32	6	32.81		100.00%	49.22%
1.00E+33	6	164.06		100.00%	100.00%
2.00E+33	6	328.12		100.00%	100.00%
8.00E+31	36	2.19		8.75%	3.28%
2.00E+32	36	5.47		21.87%	5.47%
1.00E+33	36	27.34		100.00%	27.34%
2.00E+33	36	54.69		100.00%	54.69%
8.00E+31	108	0.73		2.92%	1.09%
2.00E+32	108	1.82		7.29%	1.82%
1.00E+33	108	9.11		36.46%	9.11%
2.00E+33	108	18.23		72.92%	18.23%
8.00E+31	252	0.31		1.25%	0.47%
2.00E+32	252	0.78		3.12%	0.78%
1.00E+33	252	3.91		15.62%	3.91%
2.00E+33	252	7.81		31.25%	7.81%

Geant MC for minimum bias events generated using di-jet s.

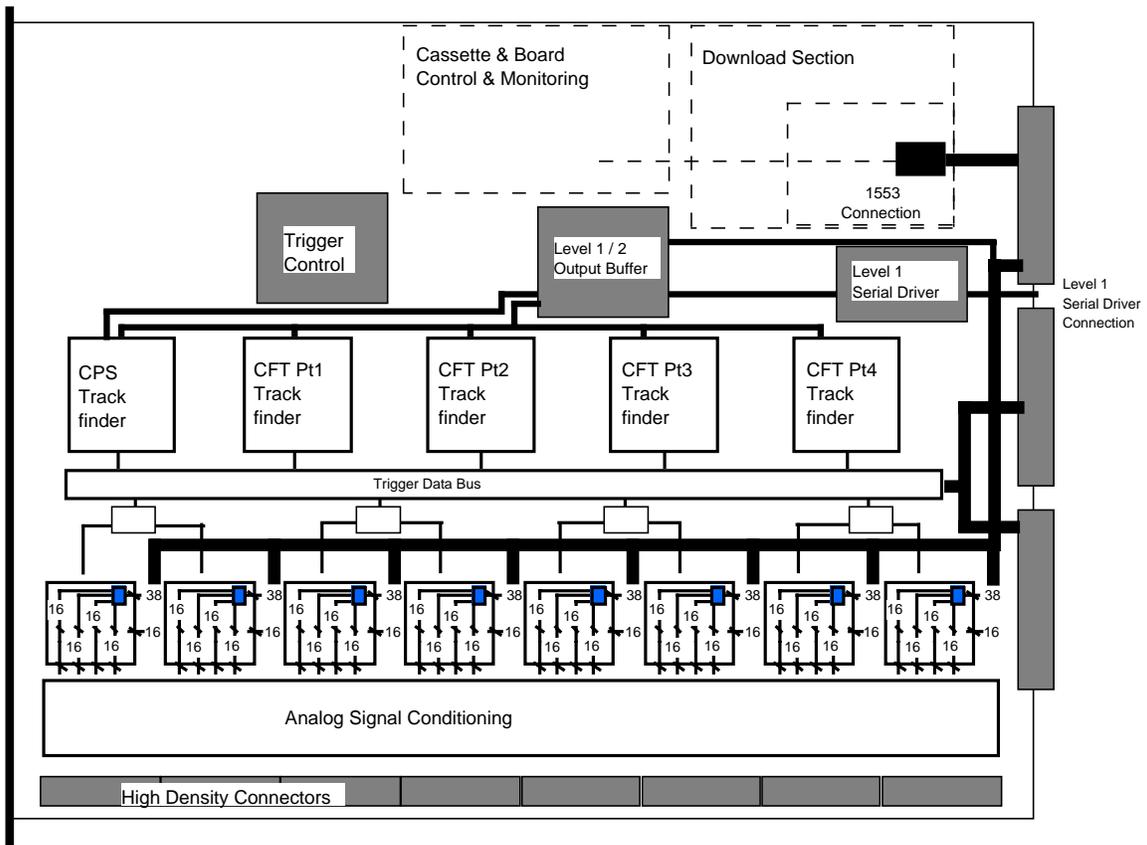
4% Occupancy / Interaction for Inner layer

1.5% Occupancy / Interaction for Outer layer



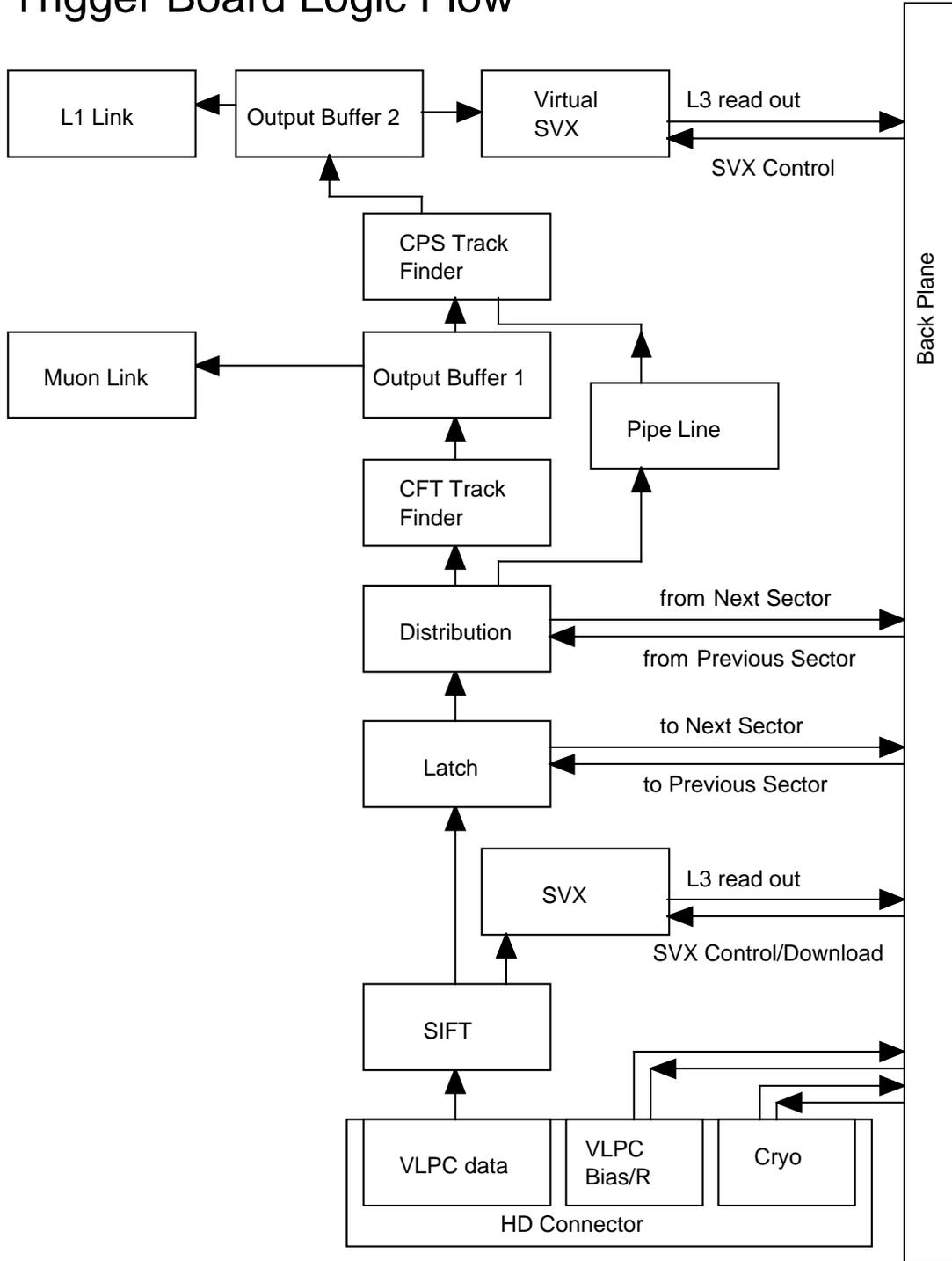
When we use the fit to the MC data to extrapolate to n interactions per crossing we can plot the trigger rate for any luminosity and number of crossings.

Here we plot to the 10 GeV fine binned trigger for 1E33 with 108 bunches.



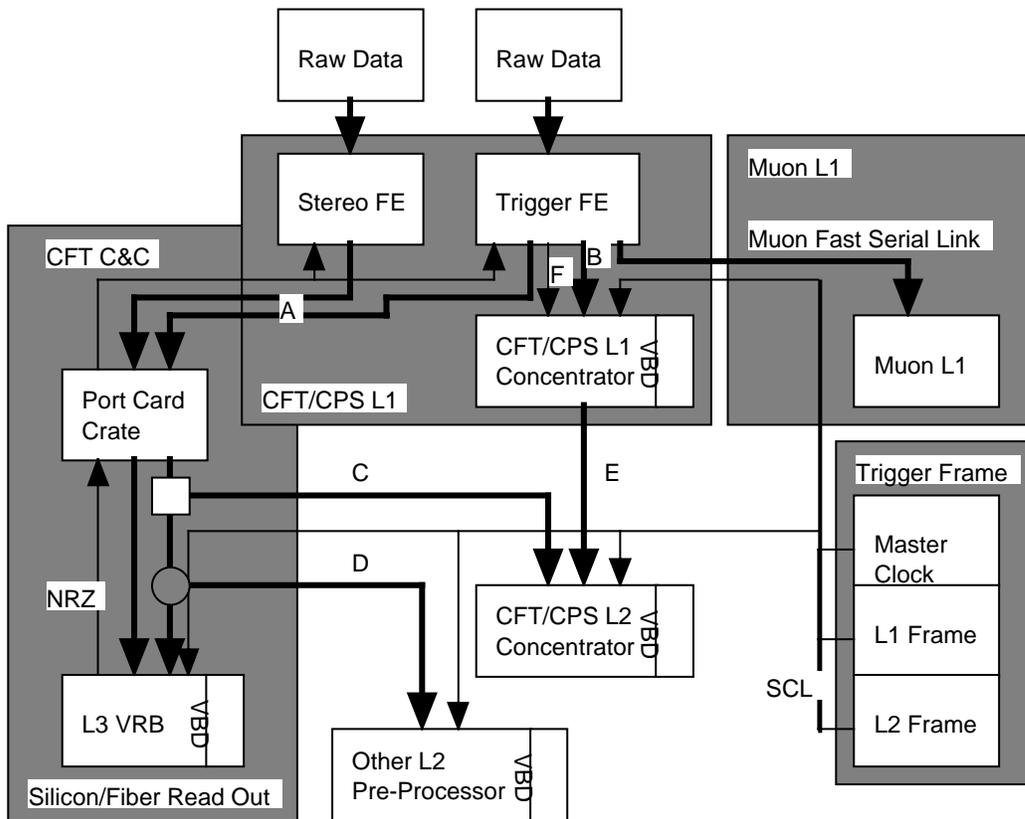
CFT/CPS FE Trigger Board Logic Flow

DATA_FLO.cdd
01-Oct-97
Fred B.



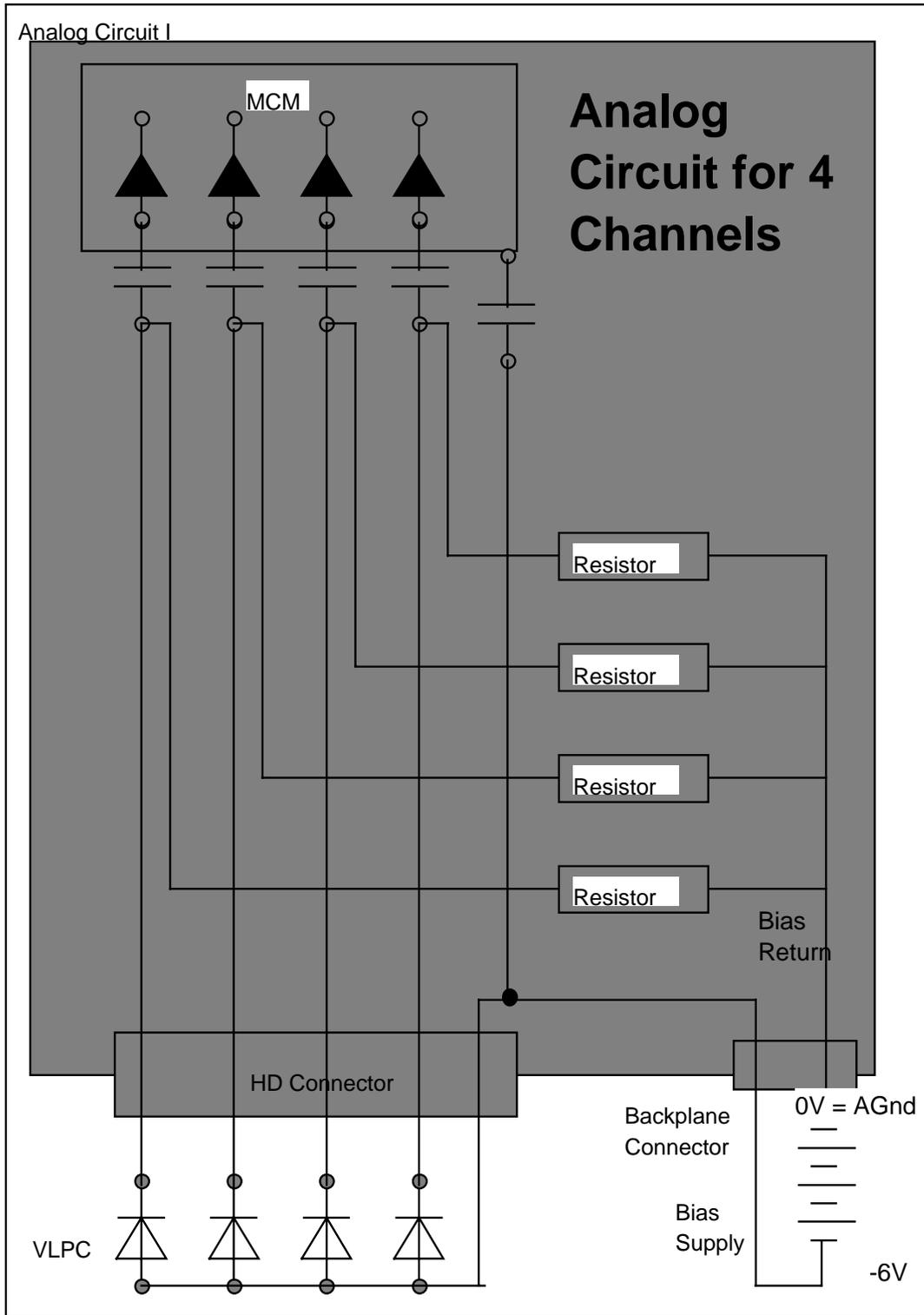
CFT_L1_Trigger
 15-July-97
 Fred Borcharding

Data and Command Flow for CFT/CPS FE & Triggers



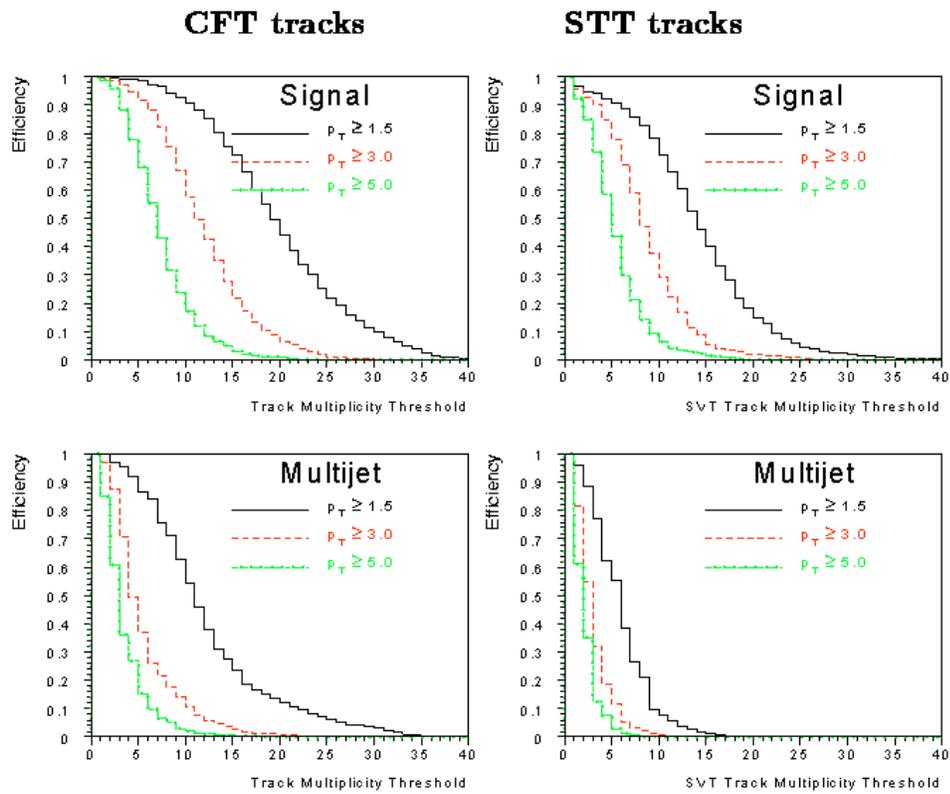
- A - Copper Ribbon
- B - Copper Ribbon
- C - FPGA Peek to Copper
- D - Passive Optical Splitter
- E - Fast Serial Optical ??
- F - Busy & Error from FE

18-April-1995
Fred Borcharding



Track multiplicity

Track multiplicity for signal and background for various track p_T thresholds



Plots by John Hobbs from Meenakshi Narain's Oct 2, 1997 SVT talk.