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Project: Dzero High Voltage
Doc. No: A1050803

Subject: Modifying HV Pods for higher gain in current readout

Introduction

The Layer 0 Silicon Detector upgrade for Dzero uses the modular high voltage system common throughout the experiment. They use a set of the Type 4 high voltage pods (2kV, 3mA maximum output). The Layer 0 system runs these pods at very low output, typically less than 100 volts, to bias the silicon strip detector elements. At that voltage the current is near zero. This causes problems because small variations in the current are below the resolution of the high voltage system and because a correspondingly low AC current trip setting causes nuisance trips. A request has been put forward to modify some of the type 4 pods to achieve higher resolution current readings. This document details the changes and the effects those changes will have.

Circuit Description and Modification Analysis

The high voltage pod schematic is available as Fermilab engineering drawing number 3740-124-ED-295564. Current draw from each pod in the Dzero high voltage system is accomplished by use of an operational amplifier (U3) that provides a virtual ground point at its inverting input. The non-inverting input is tied to analog ground. The output current of the high voltage pod returning from the load returns through resistor R19 to AGND. The return current must then be provided by operational amplifier U3 at its output flowing through feedback resistor R9 and resistor R8 in such a way that the inverting input of the operational amplifier stays at the AGND potential. This develops a voltage on the output of the opamp that is nominally equal to the output current multiplied by R9.

For the type 4 pod this works out to 1.54 volts per mA of output current, since R9 is 1.54K ohms. This output voltage is connected to a 15-bit ADC with an input span of 5V, for a presumed resolution of 152uV per count. Division says that the current readback resolution should be about 98.7 nA/count. In actuality the resolution is likely about four times worse due to noise and ADC limitations, so a working number would be 0.4uA/count. This reasonably matches with practical experience, where the software displays numbers jumping around between 0.1 uA and 0.7 uA of current for a pod with no load. This relates to an input voltage noise at a perfect ADC of about 600uV, which is common.

Changing resistor R9 from 1.54K to 15.0K will increase the gain such that the ADC will now read about 40nA per count, with an expected noise of ± 200 nA. The input noise of the ADC will not change (contributing about four counts, or ± 80 nA at our new scale) and the noise passed through the amplifier should be multiplied by nearly ten just like the current signal itself is. Of course all this gain does not come for free. Increasing the gain of the amplifier will cause it to saturate the ADC at a current of approximately 325uA. The op-amp is capable of generating output voltages in excess of +5V (the limit of the ADC) so this means that under *normal and acceptable output current levels the pod can generate voltages in excess of that which the ADC chip can withstand*. Normally we shouldn't have to worry about this because the current trip should scale along with the current readback; that is, the DAC value that would have set the trip point to, say, 100uA in an unmodified pod will now cause the pod to trip at 10uA.

To protect the ADC in the case where the current trip doesn't work, resistor R17 needs to be sufficiently large. The original schematic for the Type 4 pod shows a 15 ohm resistor for R17. Later documentation indicates that this was changed by Rick Hance to 100K ohms, presumably to add another pole to the filter response to make the current readback less noisy. Unfortunately, a resistor that big will introduce bias current errors in the ADC at low current levels. The CS5016 ADC specifications are based upon an analog source with a source impedance of 200 ohms. The OPA404 opamp at U3 has a maximum output current of 10mA. With a presumed maximum output voltage of +12V, this sets the lower bound for resistor R17 at 500 ohms. Thus, R17 should be set to the practical EIA value of 510 ohms.

In order to insure that software realizes these are “special” pods, one pin of header H2 (pin 7) has been cut so that the ID value read from the pod is changed from 4 (decimal) to 12 (decimal). The list of changes made is summarized in Table 1.

Change #	Component Affected	Details of Change	Rationale
1	R9	Change from 1.54K to 15.0K	Increase gain of current readback by factor of 9.74.
2	R17	Change from 100K (or 15) to 510 ohms	Protect ADC and insure impedance match to ADC
3	H2	Clip pin 7	Change pod ID from 4 to 12

Table 1

External Markings for Visual Identification

Type 12 pods have a sticker placed on them that clearly states “TYPE 12 POD”. This sticker is placed on the yellow metal can encasing the pod at the time the pod is modified.

Testing Modifications

These pods are tested just like any other high voltage pods. At Dzero, the test stand uses the old DOS “HVD” program. The D0HVPODS.DAT file has been modified so that the entry for pod ID #12 (0x0C hex) is set to match the expected performance of the newly modified pods. One takes the information for a type 4 pod and copies it to the type 12 line in the file, leaving everything the same except for the maximum current. This is set to the value for the type 4 pod, divided by 9.74.

Because the current readback gain is greater, these pods trip easily and thus need be tested at relatively low output voltage or with a relatively large load resistance. Since the noise of the HV pod design does not scale significantly with the actual output voltage, I recommend the testing procedure be modified as follows for these pods:

- Verify output voltage and output noise using a load resistance no less than 10 megohms. At an output voltage of 2000V, such a load will draw 200uA of current. The 15.0K gain resistor will then develop a voltage of 3V at the input to the ADC, within operational limits.