

L1_Cal Int/Comm Team Toolbox

September 19 -September 23, 2005

Mon, Sept. 19	<p>ADF→tape (Nayeem/Sabine) Defining ADF data pattern with unique data in each TT and event for debugging BC mismatch.</p> <p>TAB (Cory/Jaro) Captured signal tap data Jaro requested.</p> <p>Simulation/Algo (Sabine/Cory) Thresholds adjusted. Possible overflow/saturation/boundary issues. Investigating.</p> <p>TRANS_SYS(Johnny) ATC FP due today. PP expected Wed/Thurs. 50 ATCs expected this week. After visual inspection delivering to assembly house.</p> <p>Infra(Lyn) Defining operating parameters for Wiener load testing.</p>
Tues, Sept. 20	<p>ADF→tape (Nayeem/Sabine/Cory/Mike) Investigating TAB signal tap double L1_accepts, verifying timing.</p> <p>Simulation/Algo (Sabine/Cory) Checking firmware for overflow bit, generating test bit pattern to exercise same, comparing results w/Nevis.</p> <p>TRANS_SYS(Johnny) ATC FP in house.</p> <p>Infra(Lyn) Defining operating parameters for Wiener load testing.</p>
Wed, Sept. 21	<p>ADF→tape (Nayeem/Sabine/Cory/Mike) Folded back one iteration of Global chip firmware on TAB. Ran offline w/no no errors. Checking BC # match. Physics run sometime today. Trying to catch pesky crazy 8s.</p> <p>Simulation/Algo (Sabine/Cory) Simulation software bug found and corrected. Running test.</p> <p>GAB (Mike) Setting up timing.</p> <p>TRANS_SYS(Jorge) Installing FP on ATCs.</p>
Thurs, Sept. 22	<p>ADF→tape (Nayeem/Sabine/Cory/Mike) 2 physics runs planned w/global firmware versions. Signal tap indicates BC mismatch between ADF and TFW. Appears SCL/VME begins counting with 0 instead of 1. Jaro modifying firmware.</p> <p>Simulation/Algo (Sabine/Cory) Investigating overflow bit assertion.</p> <p>GAB (Mike) Setting up timing.</p> <p>TRANS_SYS(Johnny G) Visiting vendor to understand discoloration, masking flaws on 2nd batch (26) ATCs. Appear to be cosmetic but checking before committing parts. PP due today.</p>
Fri, Sept. 23	<p>TRANS: 47 ATC boards sent out to be stuffed. Expecting 65 working boards by end. of next week. Patch panel boards: received 100, looked 25 inspected-ok. Sending 75 out of 100 out for assembly today. Jorge installing front panels.</p> <p>ADF->tape: 8s linked to chip 10 firmware and chip 2.</p> <p>Sim/Firmware comparison: Cory sent an example event of where firmware and simulation don't agree—sent to Chad for comparison.</p>