

L1_Cal Int/Comm Team Toolbox

August 15-19, 2005

<p>Mon, Aug 15</p>	<p>TAB→Cal_Track (Cory/Sabine/Jorge) Setting up data file to send expected 159 events to Cal_Track. TAB→L3 BER (Mike/Mark/Lyn) Setting up sequential pattern in TAB to debug event glitches as seen by VRB firmware. BLS→tape (Sabine/Mike/Nayeem/Todd) Ila/Ilb/Prec. comparison data will be shown at Int/Comm meeting today. TRANS_SYS (Johnny/) Glenair test card ready. Jorge working w/Rahmi to establish test procedure. ORC (Lyn) Finishing documentation.</p>
<p>Tues, Aug 16</p>	<p>TAB→Cal_Track (Cory/Dan/Mike) ADF file ready. Planning to run when Dan arrives. TAB→L3 BER (Mike/Mark/Lyn) Resolving some firmware bugs. Obtained 2 VTMs from PREP. BLS→tape (Sabine/Mike/Nayeem/Todd) Found channel mismatch. Plots indicate stuck bit. TRANS_SYS Jorge working w/Rahmi to establish test procedure. ORC (Lyn) Sense line backplane fusing info finally arrived.</p>
<p>Wed, Aug 17</p>	<p>TAB→Cal_Track (Cory/Dan/Mike) ADF file ready to troubleshoot even/odd rate problem. TAB→L3 BER (Mike/Mark/Lyn) New firmware and TAB seq data file available to debug extra words. BLS→tape (Sabine/Mike/Nayeem/Todd) Replaced VRB and VTM for stuck bit problem. Todd looking at new data, generating plot. Requesting physics run. TRANS_SYS (Lyn) Successfully tested continuity/shorts on LVDS cable. ORC (Lyn) Documentation submitted today.</p>
<p>Thurs, Aug 18</p>	<p>TAB→Cal_Track (Cory/Dan/Mike) ADF file ready to troubleshoot even/odd rate problem. TAB→L3 BER (Mike/Mark/Lyn) New firmware and TAB seq data file available to verify global to VRB transmission. BLS→tape (Sabine/Mike/Nayeem/Todd) Stuck bit gone. TRANS_SYS (Lyn) Assisting in calibration of Glenair. ORC (Lyn) Documentation forwarded to review committee.</p>
<p>Fri, Aug 19</p>	<p>TAB→Cal_Track (Cory/Dan/Mike) Even/odd rate problem due to last event word (parity) shift to next event. KJ developing trig file to troubleshoot early next week. TAB→L3 BER (Mike/Mark/John) Modified VTM cap in ppl circuit. Ran 250M events from TAB global chip to VRB—no errors. Trying from TAB SW to VRB today. ADF→tape (Sabine/Mike/Nayeem/Todd/Dan) Using ADF to tape configuration to check mapping and BX if TAB SW→VRB clean. TRANS_SYS (Alan/Dan/John) Disconnected from TAB and secured extra LVDS cables in ADF rack, installed ½ crate ADFs, cabling up 1 full TAB, installed rack doors, making front panel covers. ORC (Lyn) Test stand ready for review.</p>