

**D0 Upgrade** *Electronics*

**Technical Design  
Report**  
for the  
**Upgrade L1/L2 Tracking  
Trigger**  
Including  
**Central Fiber Tracker,  
Central Preshower Detector,  
Forward Preshower Detector,  
Forward Proton Detector**

**Version 2**

by D0 Electronics Group\*

D0 Electronics Group: (preliminary)

Fred Borcharding, Stefan Gruenendahl, Marvin Johnson, Manuel  
Martin, Kin Yip.- *Fermi National Accelerator Laboratory*

Mario Vaz - CBPF/LAFEX DEL/UFRJ

yyyy

test

## 1. Introduction

### 1.1 Scope of the Document

This document is the technical design report for the front end electronics and trigger for four of the upgrade detectors, the Central Fiber Tracker, CFT, the Central Preshower, CPS, the Forward Preshower, FPS, and the Forward Proton Detector, FPD. Three of these detectors share the same Front End, FE, location the VLPC cassettes and all share the same hardware. The electronics for the four detectors are grouped into four systems that are not arranged along detector boundaries.

The FE and trigger systems included in this document are:

- |                        |  |
|------------------------|--|
| <u>CFT/CPS Trigger</u> | The detector inputs for this system are the Central Fiber Tracker, CFT, Axial fibers and the Central Preshower, CPS, Axial strips. This system forms the L1 Fiber Tracker Trigger and supports the L2 Central Fiber Tracker preprocessor, CFTpp, the Silicon Tracking Trigger preprocessor, STTpp, and the Preshower preprocessor, PSpp. <u>As of this writing the STTpp and PSpp are not approved projects.</u> |
| <u>CFT Stereo</u>      | The detector inputs for this system are the Central Fiber Tracker Stereo fibers. This is a FE system only and does not support any trigger.  |
| <u>PS Trigger</u>      | The detector inputs for this system are all of the Forward Preshower detector strips and the Central Preshower Stereo strips. The FPS strips are used to form the L1 Forward Preshower Trigger. The FPS and CPS stereo strips are used for the L2 Preshower Trigger preprocessor, PSpp. <u>As of this writing neither the FPS nor CPS trigger beyond the FE are approved.</u>                                    |
| <u>FPD Trigger</u>     | The detector inputs for this system are the Forward Proton Detector. These inputs are used to form the L1 Forward Proton Detector Trigger and supports the L2 Forward Proton Detector preprocessor, FPDpp. <u>As of this writing no FPD trigger beyond the FE are approved.</u>  |

The first of these systems, the CFT/CPS Trigger, is the largest system and has the most mature design. This document will describe that system first and in detail. For the other systems this document will point out the shared features and describe in detail only the unique features of each system.

Note that, for some of the systems, parts of the design presented in this document are not approved projects. For the purposes of this document they are treated as if approved and the complete system designs are presented. It is expected that those parts not approved can later be omitted with minimal impact on the overall operation of the as-built system.

## **1.2 Structure of the Document**

This document has three major roles to fulfill:

- 1) It supplies a functional description of each of the five systems and its interaction with other elements of the upgrade detector.
- 2) It supplies a complete as possible description of the hardware and/or firmware already designed.
- 3) It supplies a complete as possible design criteria to follow in the design of elements not yet fully designed

This document is divided into five sections. The first addresses the environment and features shared by all the systems and the next sections each describe one of the above four systems. Each system is at the '0.' level of the document headings. Within each system one or more sub-systems are described, which are at the '0.0' level of the headings. For each of these subsystems a brief functional description and detailed system architecture description are given, which is at the '0.0.0' level of the headings. The functional description is intended to give the major functionality of each part with a general audience in mind. The system architecture description is intended to detail the system at the expert level. This part of the document is aimed at those designing and building the not yet finished parts of the system. And by those who install and maintain the systems as a basic reference document.

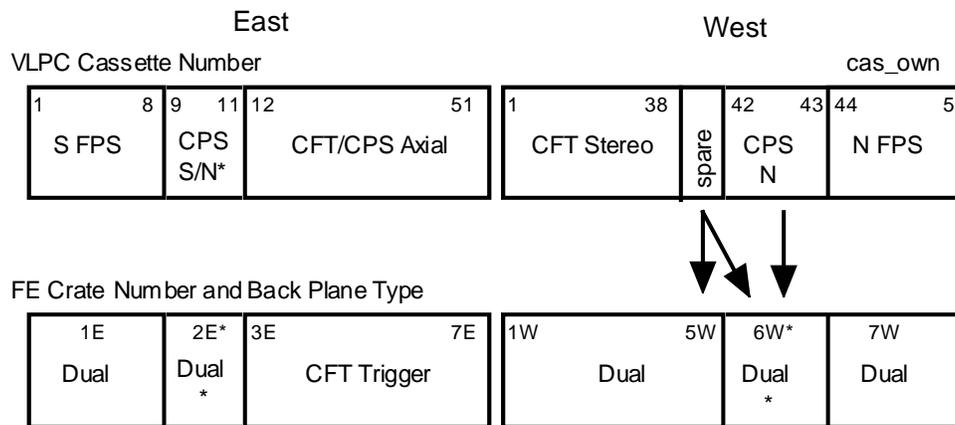
This document also points which part of the described systems are, at the time of the writing, either built, designed, or simply specified. The document is followed by several appendixes, which give design details on specific aspects of the systems.

### 1.3 Features Common to all systems

Three of the systems in this document have their FE boards mounted on VLPC cassettes located in the center row of the center platform. Several of the systems have a L1 trigger and several of the systems support a read out for input into a L2 preprocessor. But most importantly for this document, since they share so many common attributes, they are designed to share most the same hardware.

#### 1.3.1 Cassette Ownership

The different detectors are arranged in the VLPC cassettes and FE crates as shown in figure 2. The VLPC cassettes are numbered from east to west with numbers 1 through 51 for both the east and west cryostats. The CFT/CPS Axial fibers are in the 40 cassettes numbered from 12E through 51E. These cassettes are arranged into groups of 8 that share the same back planes and form a single FE crate. Each cassette holds two FE boards and therefore each crate holds 16. There is no room in any crate for any boards other than FE boards. Therefore



other boards which might normally be located in a FE crate have to be located in a remote Utility crate. These five crates belong to the CFT/CPS Trigger System.

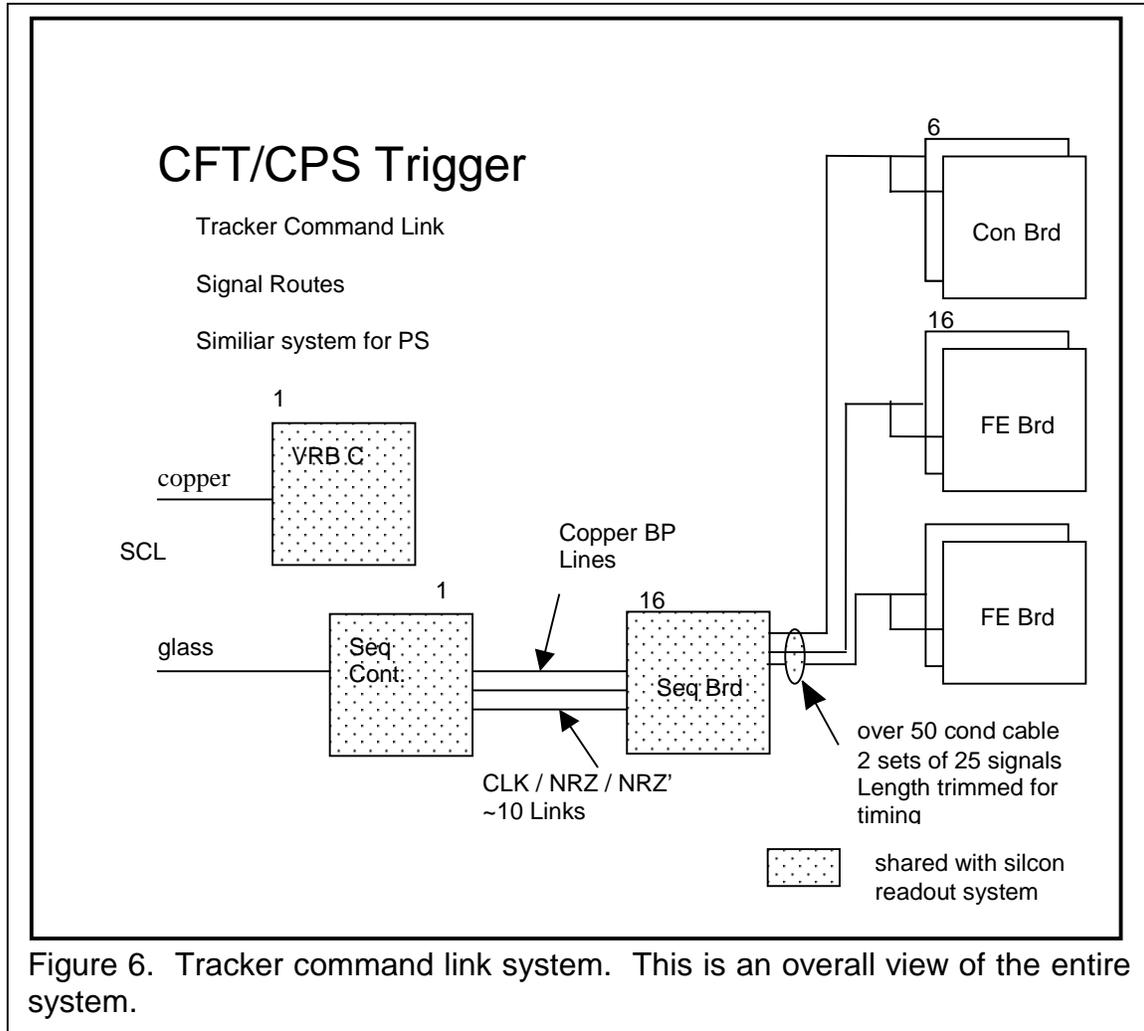
The CFT stereo fibers are in 38 cassettes numbered 1W through 38W and populate most of 5 crates. The FPS South (North) is in 8(8) cassettes numbered 1E(44W) through 8E(51W), which are at either ends of the row of cassettes and occupies one crate at each end. The CPS stereo is divided with part in the east cryostat and part in the west. The CPS stereo south and some of north are in cassettes 9E through 11E and the remainder of CPS north is in cassettes 42W and 43W. Cassettes 40W and 41W are spares. All of the crates are 16 FE boards or 8 cassettes wide except the two holding the CPS stereo. These are short crates, each of which is 6 FE boards or 3 cassettes wide. These short crates are in the center of the cassette string so that all the spare cassettes are grouped together.

The location of the FPD FE boards is has not yet been determined but for strong reasons will probably be located on the West platform.

### 1.3.2 Tracker Command Link, TCL

#### 1.3.2.1 System Overview

The D0 detector uses a set of Serial Command Links, SCL, to maintain coordination and synchronization between the various detector parts. Each SCL serves a single Geographical Sector, GS, of the detector. The CFT Trigger FE, is one GS. The CFT Stereo FE is another and the Preshower, which includes



the Forward and Central Stereo, is a third. The command information and timing must be translated from the SCL to the FE hardware and the status information returned. The Silicon Detector readout constitutes several GS and also uses this same command system. This section describes the system command links for the tracking system called the Tracker Command Link, TCL.

The major features of the TCL from the SCL to the FE and back are:

- A single SCL is sent to the Sequencer Crate on the platform. This is a slave of a duplicate link sent to the corresponding VRB crate.
- The SCL is landed in the Sequencer Controller Board. This is a dual board, it lands two SCL links and serves two GS.
- The Controller board actively fans out selected SCL signals over the Sequencer crate back plane. Which of 20 slots receives each output is remotely selectable. Trace lengths on the controller board and back plane fix the phase delays between the 20 slots.
- Each Sequencer board receives the signals from the controller and translates them into signals to control the SVX chip strings, the SIFT chips associated with each string, and the operations on the FE boards containing the strings.
- Each FE board may generate status information, which is sent back to the SCL. The information from each FE board is put onto a crate wide bus.
- The information from each crate is returned to the Controller board which OR's the result to a single set of information.
- The information from the Sequencer Controller board is returned to the VRB Controller board.
- The VRB Controller board records for host computer retrieval whether the status information it received came from the link to the Sequencer or from within its own crate. It then sends the combined information back over the SCL. The passing of information back from the Sequencer at the VRB controller can be remotely disabled with a command from the host.

The TCL not only tells the system what to do but also when to do it. The 'absolute' timing of some commands relative to the beam crossing is critical, as is the relative timing within several groups of signals. The origin of the SCL is expected to be timed relative to beam crossing to fewer than 5ns and to maintain that accuracy over the course of the run period. This system is designed to control the timings at the FE boards at 2.5ns.

The overall timing of the GS is controlled remotely by delaying the SCL at its source. Controlling the relative path lengths to each FE board closely controls the timing within each GS. At each of the FE boards the start and duration of each of the many local clocks are controlled independently.

### **1.3.2.2 Sequencer Controller Board**

The Sequencer Controller Board is a single wide 9U VME style board mounted in the first slot of a Sequencer Crate. This board has two SCL receivers, 20 channels of timing and control output to the sequencer boards, 16 channels of status input from the FE crates, and 2 channels of status output for the VRB Controller.

Each board serves two GS by interfacing with two SCL links. These links are realized in optical fiber and the receivers are located on plug in daughter boards. After the daughter board has landed the SCL signals, several are routed to the mother board where they are translated to the NRZ protocol described below and transmitted over each of the 20 output channels. Each of these 20 channels is independent and can receive SCL commands from either of the two SCL inputs. Which of the 20 channels is linked to each of the two SCL is set

Line	Bit Number	Name	Description
1	1	Framing Bit	Start of 7.6 MHz Crossing Cycle
1	2	Crossing	This is a beam crossing*
1	3	D1	Data
1	4	D2	Data
1	5	D3	Data
1	6	D4	Data
1	7	Parity bit	Parity of preceeding 6 bits
2	1	Framing Bit	Start of 7.6 MHz Crossing Cycle
2	2	Spare	
2	3	Reset	Start/Continue RESET
2	4	Sync. Gap.	Start/Continue SYNC_GP
2	5	1st Crossing	Start/Continue 1ST_CRS
2	6	L1 Accept	Start/Continue L1_ACC
2	7	Parity bit	Parity of preceeding 6 bits

Table 1 Definition of the NRZ protocol bits. The first line carries information used by the SVX chips exclusively. The second line carries additional information used by the FE boards.

and sensed remotely. At the back plane interface of the board are 20 sets of 4 traces. Each set of four traces is routed over the crate back plane to a single sequencer board slot.

For each channel, the 53 Mhz signal is converted into a signal pair, clock and clockbar, and sent over two of the four back plane lines. Other command signals are extracted from the SCL and coded into two separate protocols using a non-return-to-zero format. Each of these signals is sent over the back plane on the remaining two lines. The phase delay for all channels is controlled to be equal to better then 1ns from controller board to sequencer board with controlled path lengths on the controller board.

The 16 channels of status return are each 3 signals plus ground. Eight channels are wire OR'ed together and sent over each of the two status output channels. The grouping of the 16 channels down to 2 is built into the board.

### 1.3.2.3 Signals on the NRZ Back Plane Links

Four traces from the controller card to each pair of sequencer boards carry the differential 53 Mhz clock on two lines and a separate NRZ protocol bit sequence on each of the other two lines. Each of the NRZ protocol signals consists of a bit string of 7 bits. The first bit, the framing bit, must always be present, equal to 1, and is used to keep the decoding hardware in synchronization with the encoder. The next 5 bits carry information and the 7<sup>th</sup> and final bit encodes the parity of the preceding 6 bits. The signals on both lines use a non-return-to-zero protocol, NRZ. That is if two or more successive bits are all high, the signal stays high. The definitions of these 7 bits are listed in table 1. The details of this may be modified during the sequencer board design. The bits carried in each line are extracted in coincidence with the 53 MHz clock, stored, and executed at the start of the next framing bit.

Line 1 encodes the information for the SVX chip strings and is necessary for the silicon system readout as well. Line 1, bit 2 is the crossing bit and marks this crossing as having beam. In 132ns mode this bit is always present. During 396 running this bit is present only for every 3<sup>rd</sup> Framing bit and marks a crossing with beam. Line 1, bits 3 through 6 are used to encode 16 possible commands. This packing of commands into 4 bits maximizes the amount of information that can be sent. But only one of those commands can be sent each crossing. The bit coding for these 16 commands are defined elsewhere. Line 1 is sufficient for controlling the SVX chip strings.

Line 2 encodes the signals for the SIFT chips and the trigger and is necessary only for this system. It is not transmitted across the back plane for those systems where it is not needed. Line 2, bit 2 is a spare bit and Line 2, bit 3 marks a GS reset. Line 2, bit 4 marks the one gap each turn that is used as the synchronization gap. Crossing number 1 occurs within this gap. Line 2, bit 5 marks the first crossing of a turn. Line 2, bit 6 marks that a L1 accept has occurred.

### 1.3.2.4 Sequencer Card

Each sequencer board receives the NRZ signals and decodes them. It translates the information coded on line 1 into the command format expected by the SVX chip strings and the information coded on line 2 into the command format expected by the FE boards. If the line 2 signals are not present the sequencer board does not generate the signals in block type.

Each sequencer board has 4 output 50-conductor cables. Each of these cables is used to read out two strings of SVX chips.

### 1.3.2.5 Signals on 50-conductor Cables

The signals carried on the 50-conductor cable are shown in table xx. The FE uses the signals shown in block print exclusively. The SVX chip strings use the signals shown in italic print. Twenty-one signals connect to SVX chip string A and twenty-one to string B. The FE board uses the other 8.

### 1.3.2.6 FE Boards

Each 50-conductor cable is connected to the FE back plane and the signal routed to two FE boards. Therefore each FE crate has 8 cables which

Net no.	Net Name	Connector no.		Description
1	CROSS	1	38	53/7 (53/21) always present
2	/CROSS	26	14	53/7 (53/21)
3	GND	2	39	Connect pin to GND Shield
4	CLK_A	27	15	SVX clock -
5	/CLK_A	3	40	frequency varies
6	SYNC_GAP	28	16	Synchronization Gap
7	1ST_CROSS	4	41	First crossing of turn indicator
8	PRIORITY_IN_A	29	17	Top Neighbor
9	CHANGE_MODE_A	5	42	Mode control
10	MODE1_A	30	18	Mode control
11	MODE0_A	6	43	Mode control
12	D7_A	31	19	Data Buss
13	D6_A	7	44	Data Buss
14	D5_A	32	20	Data Buss
15	D4_A	8	45	Data Buss
16	D3_A	33	21	Data Buss
17	D2_A	9	46	Data Buss
18	GND	34	22	Connect pin to Gnd Shield
19	D1_A	10	47	Data Buss
20	D0_A	35	23	Data Buss
21	HDI_ENABLE_A	11	48	Enable String
22	DVALID_A	36	24	Data Strobe
23	PRIORITY_OUT_A	12	49	Bottom Neighbor
24	DIR_A	37	25	Transceiver direction
25	VCAL_A	13	50	Cal Voltage - DC level
26	L1_ACCEPT			L1 Accept indicator
27	CLAMP			Clamp the SIFT to SVX
28	GND			Connect pin to GND Shield
29	CLK_B			SVX clock -
30	/CLK_B			frequency varies
31	RESET			Reset the FE board systems
32	Spare			

come from two adjacent sequencer boards. The 21 signals for SVX chip string A are routed to the LH board and those for string B to the RH board for each cassette. The 8 shared signals are bussed to the same pair of FE boards.

Listed below are the eight timing and command lines to each FE and concentrator board, along with a short explanation of their use and meaning.

#### Signals received by the FE boards

CROSS	is the crossing signal, which is 53/7 MHz in 132ns mode and is 53/21 in 396ns mode.
/CROSS	is the inverse of the CROSS signal.
SYNC_GAP	is the Synchronization Gap marker. This signal goes high at the start of the synchronization gap and goes low at its end and is used to maintain synchronization of the fast serial links off the FE boards. In coincidence with the start of the SYNC_GP and the local 53 MHz clock, the fast links start sending control sequences. In coincidence with the end of the sync-gap and the clock they resume sending data.
1ST_CROSS	is the first crossing of a turn marker. Each FE board keeps a count of the present crossing, 8 bits, and turn, 16 bits. The crossing count is reset with each 1 <sup>ST</sup> _CROSS and the turn count is incremented. The turn number is reset after a reset flag and if not reset within about 1.38 sec wraps around.
L1_ACCEPT	is the L1 accept indicator. When this signal is received the FE switches from L1 process mode to L2 readout mode.
RESET	is the Global Sector reset signal and is used to reset all parts of a GS at the same time. When it goes high each FE resets, when it returns to low each FE waits for the next 1st_cross marker and then resumes.

#### 1.3.2.6.1 FE board Clocks

At each FE board the control signals are received and translated into local clocks. One set of clocks called the analog clocks are used by the SIFT chips and are time locked to the SVX clocks which come directly from the Sequencer. The other set of clocks called the digital clocks are used to control the flow of digital information on each FE board and the flow of information off each Fe board.

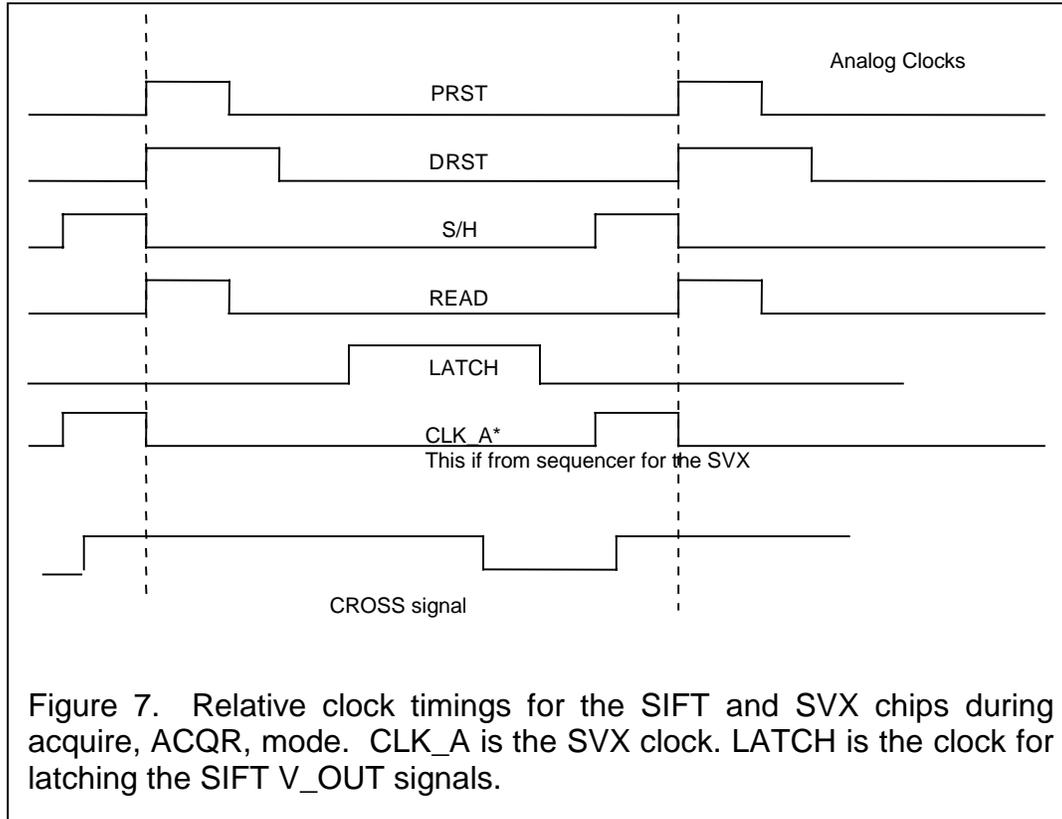
Each of the FE boards has 8 multiple-chip-modules, MCM, each of which contains one SVX chip and four SIFT chips. The clock and the control signals for the SVX chips are all generated in the sequencer board and transmitted to the FE board. Hardware on the FE board must generate the start time and duration of each of the SIFT clocks. This hardware generates two sets of analog clocks at the middle of the FE board. One set is routed to the rear of the board and the other to the front. This arrangement minimizes the on board trace length for any of these clock signals.

The SIFT can cycle at 132ns or 396ns depending on the beam crossing frequency. Which cycle time is used is set at each FE board by the clock generation hardware. At either of these cycle lengths it operates in three possible modes.

RESET a special cycle(s) with longer preamp and discriminator reset times,

- CLAMP a special cycle executed in coincidence with an SVX preamp reset, which is used to match the SIFT output level with the SVX input level,
- ACQR the normal or acquire mode used for data taking.

The five SIFT clocks are;



- PRST reset the SIFT preamp,
- DRST reset the discriminator,
- S/H switch the analog signal onto the output capacitor,
- READ switch the output capacitor onto the output line for the SVX to sample, and
- PCLMP clamp the baseline of the analog output to the input level of the SVX channel.
- LATCH Latch V-Out within the SIFTs

Each SIFT cycle starts with the CROSS signal. If the RESET signal is high a SIFT RESET cycle is executed. If the CLAMP signal is high a SIFT CLAMP cycle is executed. For all other cases an ACQR cycle is executed with each Crossing signal.

The nine digital clocks are;

- D\_READ Latch the V-Outs from the SIFTs into the PLD's

SEND(4) Send data across the BP and out of home PLD's  
STORE(4) Store data from across BP and other sources into PLD's

These nine digital clocks are in phase between the FE crates as well as within each crate.

### 1.3.2.7 Return Signals

The signals returned from the FE are;

BUSY indicates that the FE is busy and unable to generate the information for a L1 Trigger.  
ERROR indicates that an error condition exists that keeps the FE from generating the information for a L1 Trigger.  
INIT\_ACK indicates that the FE has received a RESET but has not yet finished resetting itself.

The three returned signals are the L1 busy status, the L1 error flag and the initialize acknowledge flag. Each FE board generates its own L1 busy bit if it is unable to process L1 events, and a L1 error if some error has occurred on the board. Each FE board raises the INIT\_ACK when it receives the reset signal and lowers it when it is finished with its reset and is ready to resume processing.

The signals returned from each FE board are connected to a bus in the back plane shared by all 16 FE boards in a crate. Therefore only at the FE is it possible to determine which FE is busy or has an error. This information is latched at significant event times and stored in each FE board for access via the host computer, a process that is detailed elsewhere in this document.

## 2. Central Fiber Tracker and Central Preshower Axial Trigger, CFT/CPS

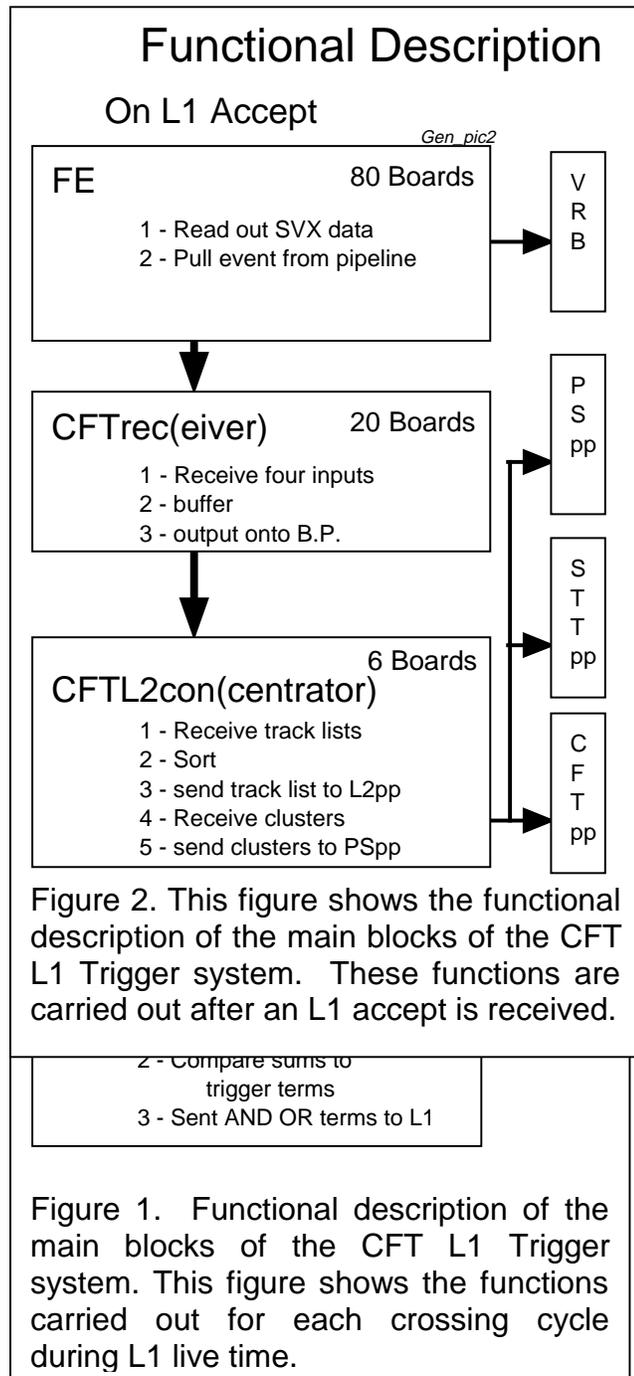
### 2.1 CFT/CPS Axial Trigger System Overview

The CFT/CPS Axial trigger system provides the means for triggering at level 1 on the information from the CFT and CPS axial channels, forms counts for a L1 multiple interaction veto, sends seed information to the muon level 1 trigger, and supplies information for level 2 trigger preprocessors. It also supplies, from the FE boards, the raw data from the VLPC channels for the level 3 read out.

For the L1 CFT/CPS Trigger it counts the number of tracks found in sixteen categories from all the FE boards and allows for a L1 trigger if any of these counts exceed a required minimum. For the L1 multiple interaction veto it counts the number of fibers hit in each sector and compares this number to a minimum. It then looks at how many sector exceeded this minimum to decide the most probable number is interactions for this crossing. For the level L1 muon system it supplies from each FE a list of tracks indexed by  $P_t$  and  $\phi$ . For the L2 preprocessors the system pipelines track and cluster information indexed by  $P_t$  and  $\phi$ , and upon the receipt of a L1 accept compresses, sorts and forwards this information.

#### 2.1.1 Functional Description

During normal running the operation of the system can be separated into four function blocks as shown in figure 1. In the FE the raw hit data is shared across the back planes between neighboring boards to form a seamless trigger. The raw hit data is then formed into bins for the fibers and clusters for the preshower. The bins are then compared to possible track roads and track candidates identified. The



track candidates are then converted into lists of tracks indexed by  $P_t$  and  $\phi$ . At this point the six track candidates with the highest  $P_t$  are formed into a sorted list and passed to the muon L1. Concurrently with the above the number of fibers hit in the sector is found and that sum compared to a minimum. When that minimum is exceeded the multiple interaction flag is set to TRUE. Next the tracks are matched with CPS clusters and possible electron candidates identified. Then the result of the track searches in the two adjacent neighbor sectors is queried and those tracks, which are the only track in three adjacent sectors, are identified. At this time the track and cluster candidates are loaded into pipelines for transfer to L2 and the count of the track candidates found and the value of the multiple interaction flag are forwarded to the CFT Receiver boards for the L1 trigger.

The CFT receiver boards, the second box in figure 1, are located in the Broadcaster Crates. Each receives information from several FE boards over a 1-bit wide fast serial link and translates it onto 16-bit wide parallel links for transmission through the crate back plane to the CFT L1 Concentrator boards. These boards which are the third box in figure 1, receive the individual counts and sum them into a single set per board, count the number of multiple interaction flags set, and send all this information out over another serial link to the CFT Trigger Manager, the bottom box. The trigger manager sums the several sets it receives into a single global set over the entire CFT/CPS detectors. At this point the individual sums are compared to cuts set by the host and are used to set bits in the AND/OR cable to the trigger manager.

Whenever a L1 accept for the system is issued it stops normal processing and shifts to L2 readout mode. The functional description for this can be divided into three blocks as shown in figure 2. First in each FE the data for the correct crossing is pulled out of the pipeline and sent to the CFT receiver boards. Also at each FE the raw data is pulled out of each SVX pipeline, digitized and read out for the L3. Most of the L3 readout system is shared with the silicon system and is not detailed in this document.

The CFT receiver boards operate in the same manner as for normal readout but now a different board, the CFT L2 concentrator board pulls the data off the back plane busses. The L2 concentrator board sorts the tracks from several front ends into a single list, sorts by  $P_t$  and sends a truncated list to the L2 preprocessors. It also sorts the clusters by  $\phi$ , forms them into a single list and sends the list to the PSpp.

#### **2.1.1.1 Geometry and Definitions**

To ensure consistent results between the FE trigger, the online, the offline and the Monte Carlo processing a unified coordinate system and system of definitions must be adopted. This section describes the coordinate system and definitions. A detailed geometry of the detector is given elsewhere.

The  $D\emptyset$  standard coordinate system is used. In this system the  $+z$ -axis is along the proton direction, which is south. The  $x$ -axis is horizontal with the  $+x$  direction pointing towards the outside of the Tevatron ring ( i.e., east). Figure 3 shows the South face of the detector. The  $y$ -axis is vertical with the  $+y$  orientation pointing towards the zenith. Azimuthal angles,  $\phi$ , are measured with respect to the  $+x$ -axis such that  $\phi = 0$  coincides with the  $+x$ -axis,  $\phi = \pi/2$  coincides with  $+y$  and  $\phi = \pi$  coincides with the  $-x$ -axis. The range of  $\phi$  is  $[0, 2\pi)$ . Polar angles,  $\theta$ , take values in the range  $[0, \pi]$  and are measured from the  $+z$ -axis.

The CFT consists of 32 concentric layers of scintillating fibers, each layer at the same radial distance from the  $z$ -axis. That is on imaginary cylinders concentric with the  $z$ -axis. The 32 layers are arranged in 16 'doublet' layers. Half of the layers have fibers parallel to the  $z$ -axis (axial layers) and the other half are at an angle to the  $z$ -axis (stereo layers). For the CFT trigger system, only the 8 axial doublet layers are used and are referred to as layer A through H with A the innermost layer.

In the  $r\phi$  plane, the CFT is divided into 80 trigger sectors with sector 1 subtending angles from  $0$  to  $2\pi/80$ . The number of fibers inside each sector in each of the 8 axial doublet layers is given by  $[16 + 4(j-1)]$ , where  $j$  is the  $j$ -th layer and the 1st layer is the one at the smallest radii. Each doublet layer consists of one inner and one outer "singlet" layer and the

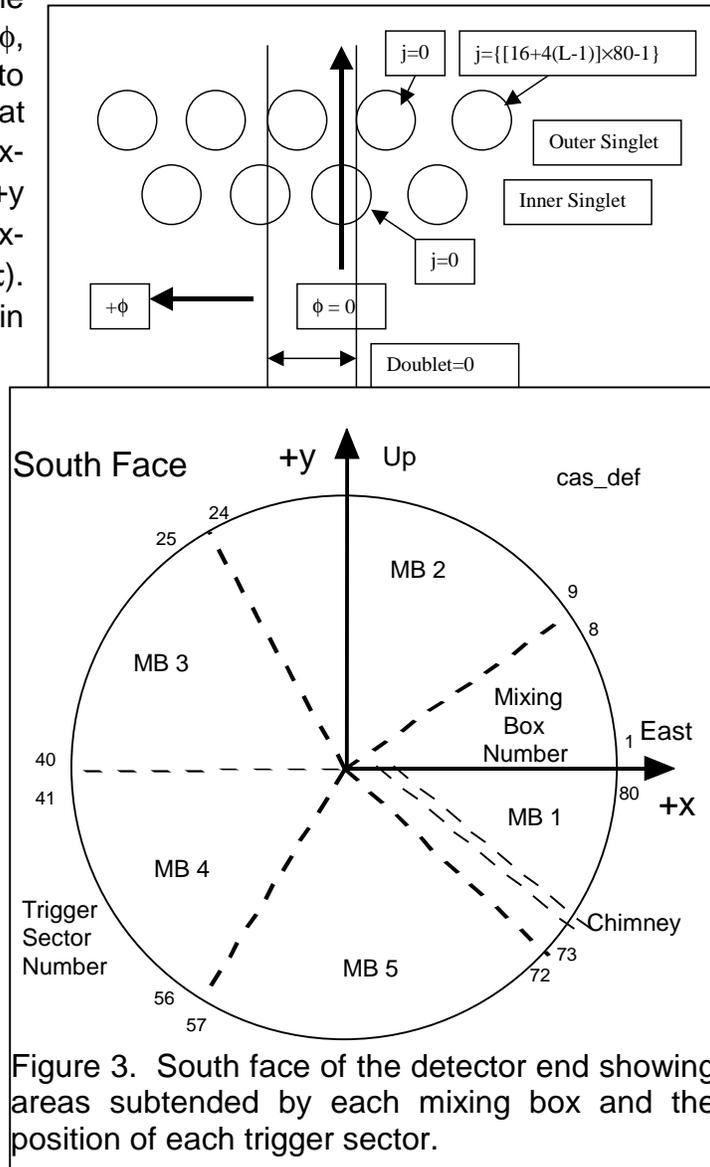


Figure 3. South face of the detector end showing areas subtended by each mixing box and the position of each trigger sector.

numbers of fibers in these two singlet layers are the same. There is an offset between the inner and outer layers in  $\phi$  by one-half of a fiber pitch. The exact geometry is detailed elsewhere.

The indices of the fibers are counted in the counter-clockwise direction if one stands at the south end of the  $D\emptyset$  detector. For each layer  $j$ , the fiber indices range from 0 to  $\{[16 + 4(j-1)]*80 - 1\}$ . The center of inner layer fiber 0 is at  $\phi = 0$ . Figure 4 shows an expanded view of a doublet layer. Note that 'up' for figure 4 corresponds to 'to-the-right' for figure 3.

A doublet bin is a logical combination of inner and outer fibers.  $DOUBLET[k]$  is defined logically as follows:

$$DOUBLET[k] = \{ NOT( OUTER[k] ) .AND. INNER[k] \} .OR. OUTER[k+1],$$

where  $OUTER[k]$  and  $INNER[k]$  correspond to the outer and inner singlet fiber indices respectively. Note that is important that exactly the above equation and the exact meaning of the indexes be used in the FE Trigger software, the M. C. simulation software, and the online and offline analysis software.

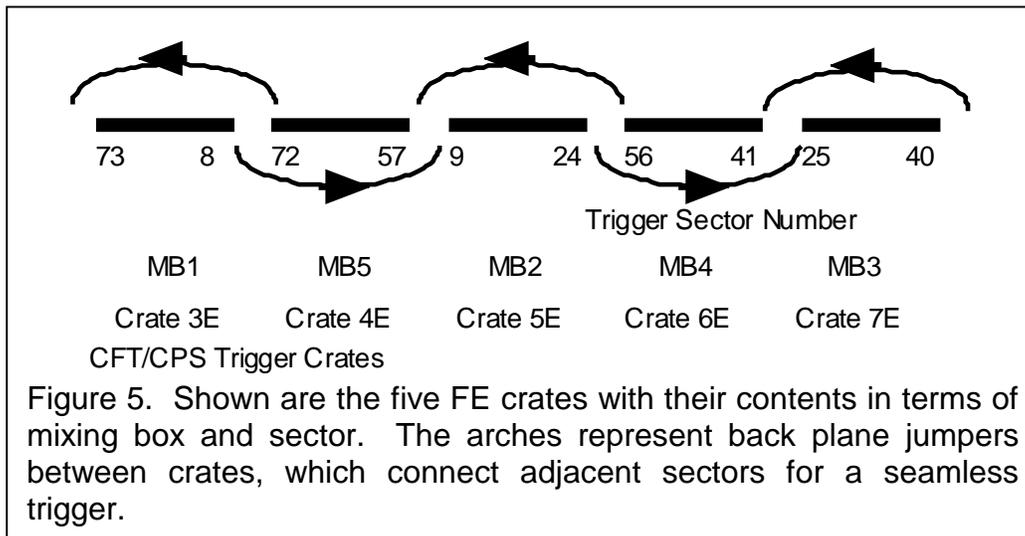
In the above definition, the width of a doublet bin depends on the diameter of the relevant singlet fibers and the gap between them, which is slightly different from layer to layer. Also the exact  $\phi$  position of the bin boundaries depends on the 'active' diameter of the fibers. The total diameter of a fiber is 0.835 mm in which 0.060 mm is occupied by two layers of cladding to make sure that the light is internally reflected and 0.775 mm is the scintillator. A charged particle, which passes through the fiber center with normal incidence, generates about 12 photoelectrons on average. The average number of photoelectrons generated by a traversing particle is linearly proportional to the length of the track inside the scintillating fiber. The CFT is likely to operate at a threshold that corresponds to about 1 photoelectron. Then by simple geometric calculations, the thickness of the area of a fiber which on average generates more than 1 photo-electron in terms of the fraction of the fiber diameter is for this case  $(1 - (1/12)^2)^{1/2}$  or 99.7% of the diameter. Therefore, under the above assumption, it is reasonable to claim that the "active" diameter of a fiber is equal to  $(0.775-0.060)$ mm or 0.715mm. Therefore the bin boundaries are approximately defined by the fiber geometry but can vary as the threshold used for the trigger or the light output from the fibers varies.

The CFT trigger system is inside a solenoid magnet, which bends all charged tracks in the  $r\phi$  plane. A charged track is said to have positive momentum if its  $\phi$  coordinate increases in value when its  $r$  coordinate increases in value. Whether this track is that of a positively or negatively charged particle depends on the sign of the magnetic field. If the positive magnetic field is orientated along the  $+z$ -axis, a positive momentum would correspond to a positively charged track, and vice versa.

### 2.1.1.2 Trigger Sectors

The level 1 trigger must accept a new event every 132ns (396ns) and send found tracks to the Muon L1 within 500ns. Therefore it is necessary to have all the data needed to make a trigger decision concentrated at one location. The trigger achieves this by dividing the global trigger into a series of local triggers each of which are independent of one another. The trigger finds tracks that propagate through all eight layers in small sectors or  $\phi$  wedges of the detector. Each of these sectors contains all or most of the fibers transited by a track. The detector is divided into eighty trigger sectors each of which has 480 axial fiber channels and 32 axial central preshower strips for a total of 512 channels per FE board. Eighty trigger sectors result in a sector size which can contain a track below 1.5GeV and at most requires fiber information sharing between two sectors to reconstruct all possible tracks.

The trigger sectors are numbered in a counter-clockwise direction when viewed on the South face of the detector with sector 1 just above the positive x-axis. Since the fibers are built in ribbons, which extend over the  $\phi$  direction, and



the trigger sectors extend in the  $r$  direction, five mixing boxes, MB, are used to map from the ribbons to trigger sectors. Each MB contains 16 trigger sectors, with the first, MB-1, containing sectors 73 through 80 and 1 through 8. Figure 3 shows the South face of the detector with the sector and mixing box numbering.

The sectors are arranged in 5 FE crates in a special order to meet two requirements. First the channels in a mixer box must all go to the same crate. Second, data is passed between FE boards so that the trigger does not have any cracks. If all the sectors were placed in one line starting with 1 and ending with 80, then passing data from sector 1 back to sector 80 would require that the signals be passed over a cable of about 8 feet. But the signal propagation time for this, about 12ns, is too long. If the sectors are packed into the five crates as shown in figure 3, then there are 5 jumpers between back planes, but now each of is about the same 16" length.

## 2.1.2 System Architecture

### 2.1.2.1 Hardware Inventory

The CFT/CPS Trigger system has;

1	GS with SCL
1	VRB Crate
1/2	Sequencer Crate
5	Front End Crates
80	FE Boards, 40 RHB & 40 LHB
2	Broadcaster Crates
1*	MTM Crate

Each VRB crates has;

1	VRB Controller board with SCL receiver
10	VRB Boards
10	VEPA Boards
40	Optical link receivers (from Seq)

Each ½ Sequencer crate has;

½	Sequencer Controller Board with SCL receiver
10	Sequencer boards
40	Optical link transmitters (to VRB), 4 per board
40	50-Conductor Cables, 4 per board

Each FE crates has;

8	Right Hand FE Trigger Boards
8	Left Hand FE Trigger Boards
8	BP Connectors for 50-Conductor Cables
8	BP Connectors for Cryo I/O

Each FE board has;

1(2)	Serial link transmitters to Muon L1
1	Serial link to broadcaster crate
1	1553 Node to receive download
1	SVX String
½	50-Conductor Cable from Sequencer
1	Analog and Serial Clock generator
8	MCM, each with 1 SVX and 4 SIFT chips

Each Broadcaster crate has;

1	Controller board
3	L1 Concentrator Board
6	L2 Concentrator Boards, 3 for STT/CFTpp & 3 for CPSpp
10	Receiver Boards
40	Copper Serial link receivers (from FE)
6	Optical Serial link transmitters to STT/CFTpp

- 6 Optical Serial link transmitters to PSpp
- 3 Copper Serial link transmitters to L1

Each Controller Board has;

- 1 50-conductor cable receiver
- 1 1553 Node

Each Receiver Board has;

- 4 Copper Serial link receivers

Each L1 Concentrator Board has;

- 1 Copper Serial link transmitter

Each L2 Concentrator Board has;

- 2 Optical Serial link transmitter

#### **2.1.2.2 Hardware description**

Figure 1 shows the overall data flow of the system. It could also be considered a crate level diagram of the system since each box corresponds to one or more crates.

The data starts in each of the 80 FE boards located on the VLPC cryostat in the center platform. During L1 live time each FE continuously transmits information for each crossing, within the time of one crossing, to two different

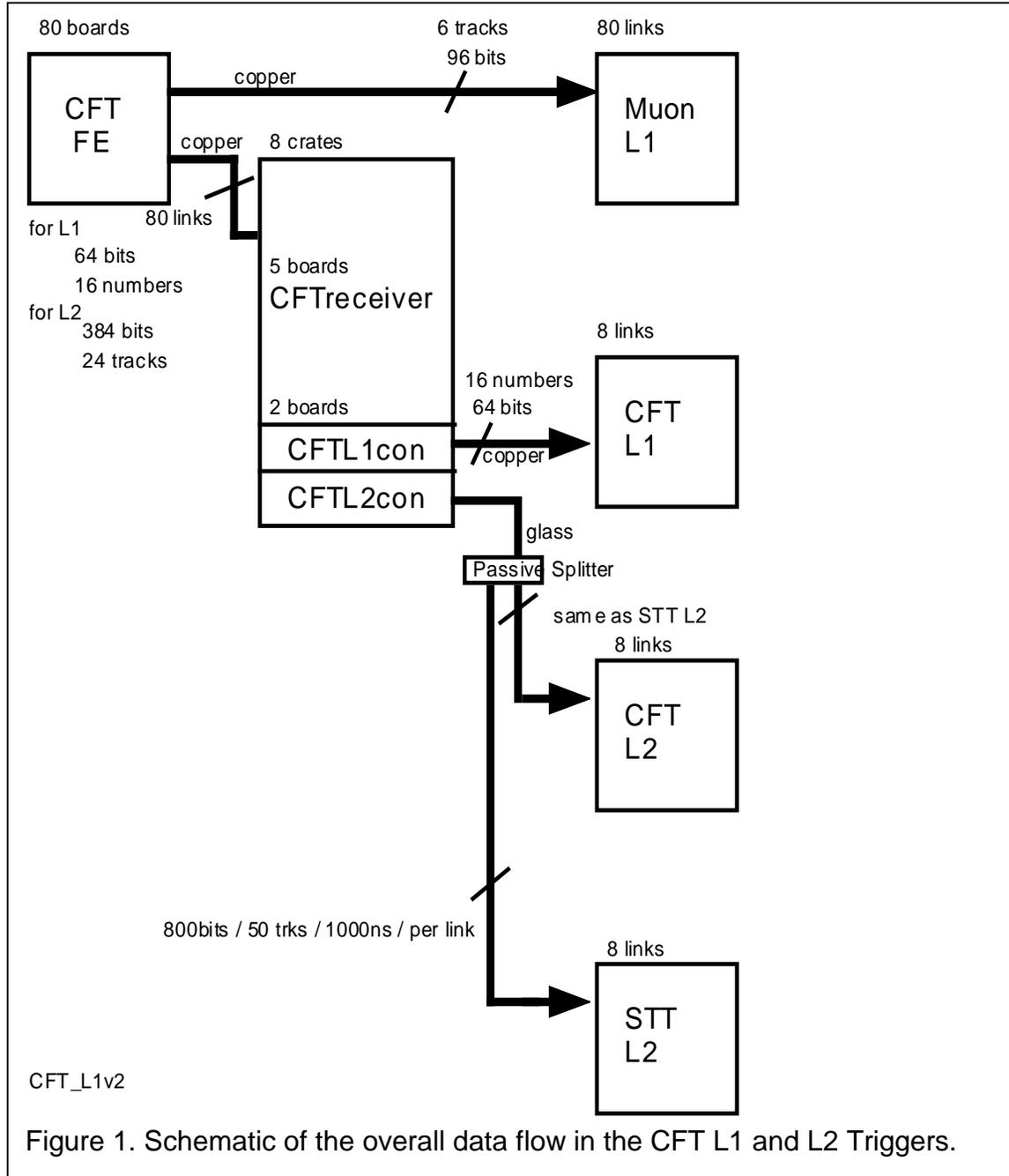


Figure 1. Schematic of the overall data flow in the CFT L1 and L2 Triggers.

destinations. One link is to the muon L1 located on the east platform and consists of 80 fast serial copper links. The other link, which serves a dual function, uses the same type of hardware and goes to eight crates on the west

platform. During L1 live time this second link carries track counts from the CFT FE. And from each of these crates fast serial links transmit data to the CFT Trigger Manager, CFTTM, in the same crate as the Muon Trigger Manager on the east platform. When a L1 accept is received this link transmits track lists from each FE to the same four crates. And from there the track lists are transported to L2 preprocessors located in the mobile counting house over a fast optical serial link. Figure 3 is a functional diagram of the system during L1 times and figure 4 is a functional diagram of the system upon a L1 accept.

## **2.2 CFT/CPS Axial Trigger Front End, CFT FE**

### **2.2.1 Functional Description**

The CFT/CPS Axial Trigger Front End boards are mounted on the VLPC cassettes which are in turn inserted into the top of two VLPC cryostats located in the center aisle of the detector platform.

Each of the 80 FE boards has several functions. The principle functions are supporting the VLPCs, VLPC signal processing and producing a fast logic signal within the MCM, finding the track, and reporting out the trigger information. Figure 2 is a schematic of the data flow on each FE.

#### **2.2.1.1 VLPC Support**

Visible Light Photon Counters, VLPC, are used to convert the light produced in both the scintillating fibers of the CFT and the scintillating strips of the CPS to electronic signals. Each VLPC chip contains a two by four array of 1mm diameter photo sensitive areas and operates at from 6 to 14 degrees Kelvin and at a bias voltage of 6.5 volts. The VLPC chips are mounted in 1024 channel cassettes that are inserted from the top into a special cryostat. The tops of the cassette assemblies when placed in the cryostat form an electronics crate. This crate contains special back planes and holds the front end electronics boards, CFT FE. For space reasons 1/2 of the FE boards must have their components mounted on the left hand side of the boards when viewed from the front of the crate while the other half are the VME standard right hand side. Therefore each type of FE board has two handedness versions.

The bias voltage is routed from the crate back plane to the VLPCs over the FE boards. Each VLPC chip has a single bias supply line but each of its eight pixels has a bias return line. The bias supply is -6.5V and the return is at 0V. A dominate failure mode of a VLPC pixel is for the output to latch up and draw a large current. This excess current can warm the entire chip and cause the entire chip to fail. To guard against this a current restricting resistor is placed in series with the bias return. After this resistor all the bias returns are tied together. All the VLPCs in a single cassette share a common bias supply and return.

The VLPC output signal is superimposed on the bias return. Therefore the input into the MCMs must be AC coupled to the bias return. This isolation capacitor is located just before the protection resistor on the FE board. Each FE board receives 512 VLPC signals and therefore has 512 sets of capacitors and resistors. To keep the space required down the capacitors are small surface mount types and the resistors are in surface mount packages.

The monitoring of the cassette temperature and the power for heaters for each group of 64 channels is routed over the FE boards also. These services are only routed on the right hand boards.

### 2.2.1.2 Analog signal processing

The expected mean signal level from the VLPC is 30,000 electrons per photoelectron and the longest charge collection time is about 70ns. The number of photoelectrons varies widely from roughly 10 at the center of the fiber tracker to 1500 for the preshower detectors. The signal needs to be both digitized and discriminated. The fiber tracker needs only a few bit ADC while the pre shower detectors need 11 bits because of their larger dynamic range and the discriminator threshold needs to be programmable over a factor of 10 range. Because of radiation damage expected during the running and downward fluctuations of the signals, the minimum discriminator threshold is 4 fC (24,000 electrons) for the fiber tracker while the maximum is around 5000 fC for the preshower. The signal processor must also provide for up to a 32 crossing delay for forming the L1 trigger. Also 512 channels are needed per circuit board.

The ADC is the SVX IIe chip, which was developed for the silicon detector. It has an 8 bit ADC with programmable gain so that the full scale charge ranges from 25 fC to 150 fC. The fastest rise time is 90ns (42ns charge collection time for 132ns crossing intervals). This does not meet all the requirements mentioned above. To meet these demands, another custom chip (called SIFT) which fits in front of the SVX IIe was designed. It has a selectable gain of 0.25 or 0.5 and a discriminator with a variable threshold of either 3 to 50 fC or 30 to 300 fC. Both the discriminator range and gain are selectable on the chip. The SIFT charge acquisition time is 70ns.

The 11 bit ADC requirement is met by using 2 SIFT-SVX channels for each of the preshower channels. A 3 way capacitor charge divider (figure n) is used so that one channel will get one tenth of the charge of the other giving slightly more than 11 bits of range. The third capacitor shunts the excess charge to ground so that the large amplitude signals are within the range of the SIFT and SVX IIe. For example, by shunting 90% of the charge, the 5000 fC preshower signal will be reduced to 500 fC at the SIFT input. If the SIFT has a gain of 1/4, 125 fC is sent to the SVX IIe which is well within its range. The 300 fC discriminator threshold is on the input charge so this signal is above the highest discriminator setting. At the other end of the scale, a few fC signal is reduced by only a factor of 2 which is also well within the range of the SVX IIe.

Each SIFT chip has 18 useable channels. Four SIFT chips and one SVX IIe are packaged together in a multichip module (MCM) where only 72 of the 128 channels in the SVX IIe are used. There are 8 MCMs on each board and all the SVX chips on each board are connected together into one readout string (the equivalent of one high density interconnect in the silicon system) and read out with a D0 sequencer module.

The output of the discriminator stage is latched to an output driver and therefore remains high for about 100ns. This signal is TTL, which is suitable for driving the following trigger logic.

### 2.2.1.3 CFT Track Finding

#### 2.2.1.3.1 Hit Transfer

Each of the 80 FE sectors subtends about 4.5 degrees. At the lowest Pt envisioned, 1.5 GeV, all tracks which cross the outer detector layer, H layer, are completely contained within the sector, called the home sector, or are partly in the home sector and one of the adjacent sectors, called the neighbor sectors. To form a seamless trigger for all tracks which intercept the H layer, called the anchor layer, within the home sector, hit information from the two neighbor sectors must be imported.

When the logic signal for each of the home sector fibers exits the MCM it is latched into a PLD. The latching action removes the time scatter of the signals due to particle eta value, light path length differences and other sources. This latching PLD then distributes the home signals to the track finding logic on the home board and to the logic on each of the two neighbor sectors. In order to minimize the number of traces on the FE boards, the number of pins on the latching PLDs and the number of back plane lines the data out of the latching PLDs is 4 to 1 multiplexed.

Four latching PLDs are used for the CFT signals and a fifth is used for the CPS signals. A special sorting of the fiber layers into the latching PLDs equalizes the size for each and allows for the different timing of the two inner layers, which are shorter.

#### 2.2.1.3.2 Track Finding

The track finding is performed in parallel within 4(or6) large FPLDs. Figure 2 shows the data flow for the track finding in the CFT FE. Each of these FPLDs gets the entire set of input fiber signals which, consists of 480 fibers from the home sector and 192 fibers from each neighbor. Since each gets all the input information and has identical output connections, which part of the track finding is performed in any PLD is simply a matter of programming. This allows the greatest flexibility for evolving the tracking algorithm as experience is gained with MC and real data or as physics goals change. It is also possible to use different algorithms in each PLD. Details of the baseline algorithm are given below.

#### 2.2.1.3.3 Track Indexing

Finding the track candidates is only half of the problem. The found tracks must be reported out to clients in a meaningful way. Each track candidate is represented by a 16 bit word into which is packed its momentum and its phi value at the outer layer of the CFT.

Sorting through the track candidates and assigning an index to each is resource intensive within the PLD, and in fact requires about the same resources as the track finding itself. The track indexing is contained in the same PLD as the track finding for information handling reasons. At the point in the algorithm where the track candidates are found the information content of the problem is at its maximum. Transferring that information out of one PLD and into another is not possible. Indeed if it were possible the track indexing itself would be trivial.

Since the track indexing is located in the same PLD as the track finding, possible algorithms are not restricted by the hardware external to the PLD and may continue to be optimized, or to be re-optimized to different goals as the run

proceeds. The combined track finding and track indexing portions of the problem require the largest and fastest PLDs available and represent a major component in the expense for the trigger.

#### **2.2.1.4 Transfer to L1 Muon**

The L1 Muon system uses the CFT track candidates as seeds for finding candidate muon tracks. Since these are the seeds for its track finding the list must arrive at the muon trigger crates before the muon chamber information. The muon drift time is about 800ns, thus the timing specification for CFT tracks to muon is within 800ns. Figure 5 shows the timing of the different tracking stages up to reception at muon. (A transmission distance to muon of 90ns was used.) These times are based on simulations of the PLD code and detailed studies of the signal timings.<sup>1</sup>

As the list of six tracks exit the four track finding PLDs they are collected in another PLD which orders them from highest to lowest Pt threshold group and transmits the first six to muon. The list of six tracks is transmitted from the FE's each crossing over a fast serial link that sends 16 bits of information every 53MHz clock cycle. This fast serial link over copper was developed for the muon trigger.

#### **2.2.1.5 CPS Cluster Matching**

The Central Preshower, CPS, axial strips are included in the trigger. The VLPC signals from each strip is passively split into two and each is input to a SIFT channel with separate thresholds. As the CFT logic signals are being input into the tracking FPLDs the CPS logic signals are input into a separate FPLD. This FPLD pipelines the strip information while the track candidates are being found. It then forms the CPS clusters in parallel to decoding the CFT track indexes. A combination of two/three center strips above a high threshold, about 4 mips, with strips on either side below a low threshold, about 1 mip, constitutes a cluster. Then it compares the clusters to the CFT track information to form a track match. If a match is found a bit is set in the original track list for that track. A more detailed note on CPS cluster matching can be found in the references.<sup>1</sup>

#### **2.2.1.6 Isolation**

The logic next determines if the tracks in the list from each FE should be tagged as isolated. As stated above a track is isolated if it is the only track in the home sector and the two neighbor sectors within a Pt threshold bin.

If there are one or more tracks in the home sector the logic raises the level on a line, which via the back plane terminates in the neighbor logic to either side. There is one line per Pt threshold bin and per CFT or CFT/CPS for a total of eight lines. The logic then looks at the corresponding input lines from each of its 2 neighbors, 16 lines. If neither neighbor found a CFT track the CFT track isolation bit is set, and if neither found a CFT/CPS track the CFT/CSP track isolation bit is set.

---

<sup>1</sup> PLD simulations - FB, Detailed studies – MM

### **2.2.1.7 Track Counting**

The L1 muon and L2 preprocessors require a list of tracks, the CFT L1, however, requires a count of the number of found tracks. A by product of the track indexing described above is a count of the number of tracks. This number is transferred to the cluster matching where a second count is created, the count of CFT/CPS tracks, and passed on to the isolation stage. At that stage two more counts are added, isolated CFT and isolated CFT/CPS. This completes the set of 16 counts.

These 16 numbers are moved to an output buffer for transmission to the CFT L1 trigger. This link is the second copper fast serial link mounted on each FE board, which sends 96 bits each crossing. The 16 numbers, each of which is 6 bits wide are packed into this data block and transmitted.

### **2.2.1.8 L2 Pipeline**

The track lists are stored in a pipeline for retrieval upon a L1 accept. There are 4 pipelines, one for each Pt threshold bin. Each is 6 tracks by 16 bits wide, 96 bits wide, by 32 deep. These pipelines are implemented in fast FIFO chips.

### **2.2.1.9 FE Controller**

The control and coordination of all the functions of the FE board requires a sophisticated controller. The controller must receive the 53MHz clock, the crossing signal, the L1 accept and an external reset and must monitor the mode of the on board SVX chips. From these it must generate the clock signals used to move the data between PLDs on the board and internal clock signals for the many PLDs. It must also generate the clock signals used by the SIFT chips and keep those chips in phase with the SVX chips which for technical reasons must be clocked external to the FE board. The controller is not a single chip but a master chip and several subordinate chips located near the chips they support.

### **2.2.1.10 Download Support**

Each of the large PLDs requires about 250Kbits of information for its programming. Programming that is lost on any power interruption. A download system is located on each FE board consisting of non-volatile memory, which stores a copy of the programs for all chips on the board and a download controller, which is a non-volatile PLD. Upon power up or reset the download controller resets itself and then downloads all the FPLDs from non-volatile RAM. During operation an external host reads the contents of the FE RAM and compares it to a master copy. If any differences are found the master copy is again downloaded to the FE board(s). Note that for the as-built detector each tracking PLD may have different tracking programming which has been customized to the surveyed fiber locations.

### **2.2.1.11 Tracking Algorithm**

#### 2.2.1.11.1 Introduction

The goal of the track finder is to achieve the highest efficiency for finding the real tracks while maintaining the largest possible rejection factor for fake tracks. In the fiber tracker the main source of fake tracks is a random fiber hit near a real track that when included with the real track hits results in a fake track of higher Pt than the real track. When this occurs for real tracks just below a Pt threshold the fake track promotes it into a found track. Another significant source when the occupancy is high is the overlap of two or more lower Pt tracks which mimic a single higher Pt track.

The greatest rejection is achieved in the trigger if a hit is required on all of the eight layers of the tracker and the road width at each layer is one fiber pitch wide, about 1mm. Wider roads result in too many extra fake tracks. Particles too often scatter out of narrower roads. The base line set of roads used in the MC show the tracker to be about 97% efficient for muons above 5 GeV and over 95% efficient for electrons over 10 GeV. There are over 850,000 roads in the tracker.

The axial trigger uses field programmable logic devices, FPLD's, to implement the trigger logic. Each road is converted into a logical equation within the device consisting of an eight fold AND of the doublet hit in each layer. Since the doublet hit is a logical OR of two singlet layers its efficiency is over 99.5%. Thus the eight fold efficiency is above 96.5%. The major advantage of using these devices is that, since the trigger logic can be programmed into them when they are in place in the detector, they can be reprogrammed as required by changes in Physics interest or detector geometry at any time during a running period. The hardware design of the boards was purposely kept as general as possible and the specific design choices are implemented in the firmware as much as possible. Thus design changes require only a new software download, not a hardware fix. FPLD's are also extensively used in the commercial market and market forces are expected to both drive down their price and drive up their performance.

The basic geometry of the tracker is discussed in several places.<sup>2</sup> Some of the basic features which are important for discussions of forming the trigger are presented here.<sup>3, 4, 5</sup> Each layer is made up of two single layers. The outer of these two layers is staggered by  $\frac{1}{2}$  a fiber so that there are no gaps, all tracks either pass through the inner, the outer or both layers. There are 8 doublet layers. The fibers are routed to the electronics so that the signals from all 8 layers for exactly  $\frac{1}{80}$ th in phi of the detector go to one board. This  $\frac{1}{80}$ th phi slice of the detector is called a sector and each sector contains 4 cells. A cell is the smallest phi slice that has a non-repeating geometry. A sector is 16 fibers wide at the innermost or A layer, increases by 4 fibers for each layer until it is 44 wide at the 8<sup>th</sup> and outermost layer, the H layer. A cell is 4 wide at the inner, 1 wider on each layer and 11 wide at the outer layer.

#### 2.2.1.11.2 Finding Track Candidates

##### 2.2.1.11.2.1 Doublet Finding

The first part of finding a track is forming a hit in each doublet layer. The individual fiber hits of each pair of singlet layers must be formed into a hit bin in the doublet layer. For the base line design the doublet bin size is the same as the fiber size of each layer. The doublet bin can be formed in the most basic manner possible, just an OR of an inner singlet fiber with one other outer singlet fiber. In equation form this is:

$$hl [ k ] = hi [ k ] \text{ OR } ho [ j ];$$

where k and j are the k'th and j'th fibers on the ribbon. The indexes are such that the inner and outer fibers are adjacent, but whether the outer fiber is to the right or the left of the inner is arbitrary. This manner of forming a doublet doesn't distinguish if a particle transited one or both fibers. Also a particle which transits an inner fiber of one doublet pair and the outer fiber of the adjacent doublet pair will generate two doublet bins hit.

The doublet formation was expanded to eliminate the possibility of a single track forming two adjacent doublet bin hits. The doublet equation is then:

$$hl[ k ] = ( \text{NOT}(ho[ j - 1 ] ) \text{ AND } hi[ k ] ) \text{ OR } ho[ j ];$$

Now if a track passes through  $hi[ k ]$  and  $ho[ j - 1 ]$ ,  $hl[ k ]$  will be FALSE and only  $hl[ k - 1 ]$  will be TRUE. Due to the architecture of the PLD this modification does not take any more logic cells, LC's, but it does require more interconnects.

#### 2.2.1.11.2.2 Track Finding

The eight doublet layer bins are then combined to form a track. The list of roads, which are found both analytically and with a special Monte Carlo, are translated into equations and loaded into the trigger logic. The base line requires that all 8 of 8 possible doublet layers be hit for any equation to be satisfied. There are about 11,000 equations in each sector and 2,600 in each FPLD. These equations are of the form:

$$\begin{aligned} T1013172227323945 = & a[10] \text{ AND } b[13] \text{ AND } c[17] \text{ AND } d[22] \\ & \text{AND } e[27] \text{ AND } f[32] \text{ AND } g[39] \text{ AND } h[45]; \end{aligned}$$

The several terms that share the same A layer doublet number, here 10, and the same H layer number, here 45, are then OR'ed together:

$$\text{Trig\_a10h45} = T1013172227323945 \text{ OR } T10\dots45 \text{ OR } \dots$$

A strait line corresponding to an infinite momentum track drawn from the center of the detector and through the center of an H layer bin passes through just one A layer bin which is defined as the zero offset bin for the H layer bin. The different Pt bins can then be defined with respect to the relative offset from

the zero A layer bin. For the above example the zero A layer for an H layer bin value of 45 is 17. Therefore the offset for A layer bin 10 is -7. Table 3 gives a calculation of the Pt for tracks of differing offsets from the H layer bin.

The output from this stage is a matrix of pins which is 44 phi bin rows, the H layer bins, by 24 Pt bin columns, the A layer offset bins. Each pin in this matrix will be TRUE (1) if a track was found or FALSE (0) if it wasn't.

#### *2.2.1.11.2.3 Serializing the Found Tracks*

The track finding stage outputs a matrix of pins. The array must be searched in decreasing Pt order looking for any pins that are TRUE. As each TRUE pin is found the phi bin address and Pt bin address for that pin are loaded into a register. This is basically a serial problem that must be solved in parallel hardware. If it were done serially the process would take at least  $44 \times 24 = 1056$  steps. To get a result every crossing this processor would have to make 1056 steps times the 27 MHz crossing frequency which requires a clock rate of 30 GHz. Alternatively the problem can be solved using PLD's using a tree structure with many parallel branches in a very short time. However, this method requires significant resources. Most of the pins or elements in this matrix are FALSE since the occupancy of the 1056 pins is expected to be less than 1%. Thus some short cuts can be taken in solving the problem, which are very efficient in their use of logic resources.

The equations are sorted by Pt value into 24 bins and by Phi index into 44 bins giving 1056 2d bins. Each 2d bin is assigned an index number that codes its phi bin value and its Pt bin value. It should be noted that this sorting criterion is arbitrary. The equations could be sorted, for example, according to the mean Pt of the equations and the mean phi value at a particular radius instead of by H value and A offset. Or they could be sorted by outer fiber bin and inner fiber bin. All that is required is that 2d bins of 44 phi units by 24 Pt units are formed.

Next the matrix is subdivided into 4 Pt groups corresponding to the 4 Pt threshold groupings of the L1 trigger terms. Each of these 4 groups is contained within a separate PLD. Each of these sub-matrixes are then 44 phi bins by 6 Pt bins. Then, for each of the 44 phi bins, the 6 Pt bins are input into a priority encoder which outputs the index of the highest priority Pt bin that is TRUE. The order of inputs into the priority encoder is arranged so that the highest Pt TRUE is output. Information about any other bin that may have been TRUE is lost. However, information should be lost less than 1/4% of the time.

At this point the matrix is reduced to a single column of 44 index numbers. The next step scans this list and puts the first six non-zero values into an output buffer. This step is done in a mixed parallel/serial mode to reduce the latency for the process to its minimum. Any information about any tracks beyond six is lost in this stage.

#### *2.2.1.11.2.4 Robustness of the Design*

The finding of track candidates discussed above is done in a set of four FPLD's where each FPLD is used to find the tracks in one Pt threshold range.

The board hardware is designed to hold six and laid out such that the extra two can be added if the necessity arises and the resources are available.

There are many things which would require the number of equations to be increased and hence more FPLD resources needed and few that would allow a decrease. The minimum Pt is a case in point. The number of equations doubles in lowering the minimum Pt threshold from 3.0 GeV to 1.5 GeV. (It scales almost exactly as the inverse ratio of the Pt.) Therefore the low Pt threshold bin requires by far the most equations. The equations used for this design assumed that the fibers were exactly placed on the detector. Studies show that systematic placement errors starting as small as 50  $\mu\text{m}$  significantly increase the number of equations<sup>6</sup>. The interaction vertex in R-Phi for this design is assumed to be a point source. We know from the accelerator that the beam spot will be about 50  $\mu\text{m}$ . The size of the beam spot has the same effect on the number of equations as fiber placement error<sup>7</sup>. Think of it as a fiber at  $r = 0$ . The CFT trigger starts to be inefficient for displaced vertex tracks. Recovering that efficiency requires more equations. Also it is believed that while the efficiency of each doublet layer will be over 99.5% at the start of the run, this efficiency will drop with aging and radiation damage especially if we see high luminosity for much of the run. As the doublet efficiency drops below 99% the base line trigger which requires all eight layers drops below 90%. This can be remedied by only requiring 7 of 8 layers, but a 7 of 8 trigger requires four times the logic resources. All of these argue that the track finder stage should be implemented in as many of the largest FPLD's that fit the budget.

Since the board is set up for 4(6) FPLDs in parallel, tuning of the algorithm independently within each Pt threshold bin is possible. A 7 of 8 trigger could be implemented in the highest Pt bin for example to maintain its efficiency. While the logic for the other Pt bins could be tuned for other criteria.

### 2.2.1.12 L3 Readout

The L3 readout should include the data from the detector and all data created at each stage of the trigger. Only the FE sees the raw data but both the FE and concentrators create trigger information.

#### 2.2.1.12.1 The FE L3 Readout

The CFT/CPS raw data is digitized and pipelined in eight SVX chips on each FE board which are connected into one string and read out by the SERIAL board located in crates located elsewhere on the platform. Each FE string has eight SVX chips for the raw data plus a virtual SVX chip located within a PLD chip for the data created by the trigger. This virtual SVX chip collects the readout information discussed below, pipelines it, and passes it on in a format imitating a single SVX chip. This virtual SVX chip receives the same mode controls as the other SVX chips but interprets them differently. The SVX mode is loaded into each SVX independently during an SVX chip download. The real SVX chips send the data byte by byte. The first byte is the channel address and the second byte is the ADC counts. The first bit of the address has a special meaning so only 15 bits of information are passed per channel. The virtual SVX

receives the data as 16 bit words. It drops the msb and sends the remaining 15 bits with the high byte in the address position and the low byte in the data position.

The input into the FE boards is the analog VLPC signal which in addition to being digitized by the SVX11e chip is discriminated by the SIFT20a chip. The discriminated signal is then presented to the trigger logic where track lists and track counts are formed. These track lists are then sent off board to the triggers. Within the track logic intermediate objects are formed and discarded. The candidate information for transmission to the L3 includes; the discriminator output bits, the resulting track lists, the track counts and information from intermediate logic stages.

Sending all the above information all the time would result in an unduly long readout time and too much L1 dead time. To keep the dead time minimal and to allow for detailed diagnostic ability four levels of readout are formed. They are NORMAL, INPUT, DIAGNOSTIC and TEST.

#### *2.2.1.12.1.1 NORMAL*

The NORMAL mode is the minimum length readout and is designed for use in normal running. (SVX Sparsify Mode.) For this mode the L3 readout for the virtual SVX consists of the list of 24 found tracks, the 16 count numbers, and a 16bit status word. Table xxx shows the contents of each byte of the readout string. The added length is 496bits and adds about 0.58usec to the SVX readout time. *Note that a string of eight SVX chips is 16Kbits long and takes up to 19usec to read out at full occupancy. So the added length is comparable to about 3% occupancy.*

#### *2.2.1.12.1.2 INPUT*

The INPUT mode includes the NORMAL mode data plus the discriminated signals from the home and neighbor sectors for both the CFT and CPS fibers. (SVX Read Neighbors Mode.) This readout adds 1408bits and 1.65usec. While this mode does not add much to the readout length it adds a considerable amount of resources to the logic because logic must be converted to a pipeline fifo to store the hits from each of up to 32 crossings until L2 readout time. Therefore when running in this mode the CFT and CPS trigger PLDs are re-programmed to use less resources, thereby freeing up logic to pipeline the input bits.

#### *2.2.1.12.1.3 DIAGNOSTIC*

The DIAGNOSTIC mode includes the INPUT data plus an extra Kbit of diagnostic information. (SVX Read All Mode.) This readout adds 2448bits and 2.88usec. As above the trigger PLDs are re-programmed in this mode to pipeline the input bits and also to intercept the results of intermediate steps within the logic and output diagnostic information. Note that the diagnostic information for each crossing must also be pipelined, so extra resources are needed to both create the output diagnostics and to pipeline them.

#### *2.2.1.12.1.4 TEST*

The TEST mode adds 2Kbits of information plus a 16bit status word, adding 2.43usec to the readout time. (The undefined SVX Mode.) In this mode any of several test processes are loaded into one or more of the trigger PLDs. For this case the raw data into the trigger logic is ignored so the data read out of the virtual SVX chip is independent of the data read out of the real SVX chips. Therefor in this mode the readout of the real SVX chips is turned off.

## 2.2.2 System Architecture

### 2.2.2.1 FE Board IO

The FE board is an I/O intensive board. It has three back plane connections of 160 pins each, plus 8 bottom edge connections of 88 pins each for a total pin count of about 1200. Each of the bottom edge connectors recieves 64 new signals every 132 ns for a bit rate of 3.88 Gbits/sec. 320 of the

#### **CFT/CPS Trigger FE Board I/O Types**

##### **Back Plane**

- 1553 Link
- Sequencer Link
- TCL Input
- Isolation Flags
- PS Signal Transfer
- Fiber Signal Transfer
- Cryo Support I/O
- Power & Grounds

##### **Bottom Edge Connector**

- VLPC Bias Supply
- VLPC Bias Return / Signal Source
- Cryogenic Services

##### **Front Pannel Connections**

- Muon L1 Copper Link Transmitter
- Broadcaster Crate Copper Link Transmitter

##### **Front Pannel Displays**

- Bottom Edge Connection Indicator
- Serial Link Status Indicators
- L1/L2 Mode indicator Light
- Download Status Indicator Light
- Hex Status Display

##### **Front Pannel Probe Points**

- Power Sense
- 16-bit Status

back plane pins transfer data every 25ns for a bit rate of 12.8 Gbits/sec.

### 2.2.2.2 Transfer to L1 Muon

The transfer of track information from the CFT FE board to the Muon Trigger System is done through a pair of serial transmitter and receiver daughter boards. The detailed I/O specification of these boards can be found in [1].

In each octant, CFT trigger information from 10 CFT FE would be transferred to a MTC05 ( Muon Trigger Card “05” ) located inside one of the three Muon Trigger Crates. Each MTC05 card accepts 16 inputs but only 10 are from the CFT FE whereas the others are inputs from the scintillator hits.

From each CFT FE, data of 6 tracks each with 16 bits and a reference clock are fed into a serial transmitter daughter board which is plugged into the CFT FE board. From this transmitter board, the CFT information is sent to the serial receiver daughter board imbedded in the MTC05 over coaxial cable ( RG58 or equivalent ) using the AMCC Gbit/s serial link chipset [1], in which data is transferred in groups of 96 bits.

Group	Signal	GND	Description
<b>Total</b>	<b>285</b>	<b>67</b>	
SVX Cont	25		3 Signals used to control & readout SIFT and SVX
Next Neighbor	96		12 Fiber Signals from Next Neighbor
Prev. Neighbor	96		12 Fiber Signals from Previous Neighbor
VLPC Bias	2		0 VLPC bias supply and return
Cryo Heat / Temp	8		0 Cryo heater lines and temperature sensor lines
Isolation	12		0 Isolation information
FE Cont	10		4 2 coax for clock + 8 buss for commands
			0
Dig 5V	12	12	
Dig 3.3/2.5V	12	12	
An 5V	12	12	
			0
			0

There are seven RF clock cycles per 132 ns and data is transferred as six data words plus a parity word during each bunch crossing. During the Synch Gap, Fiber Channel synch characters ( K28.5 ) are sent instead.

In each coaxial cable, the necessary inputs from the CFT FE to the MTC05 are as follows:

- ◆ 10 sets of CFT track information, each from a CFT FE board and having a maximum of 6 tracks;
- ◆ RF Clock
- ◆ Enable
- ◆ Parity\_Enable

“RF clock” is the clock running at the accelerator RF frequency. All other inputs, including “Enable”, are referenced to this clock. “Enable” indicates the end of Synch Gap and the start of real beam crossing. Data is transmitted when "Enable" is high, and odd parity is transmitted when both "Enable" and “Parity\_Enable” signals are high. The parity word is typically added as the 7th word after the 6 data words sent for a bunch crossing.

The following figure shows the relationship among the terms described above.

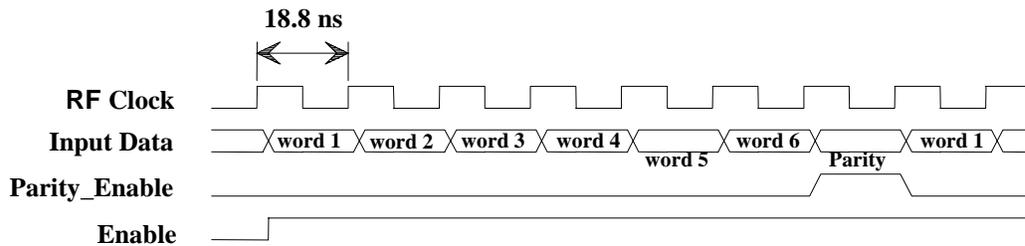
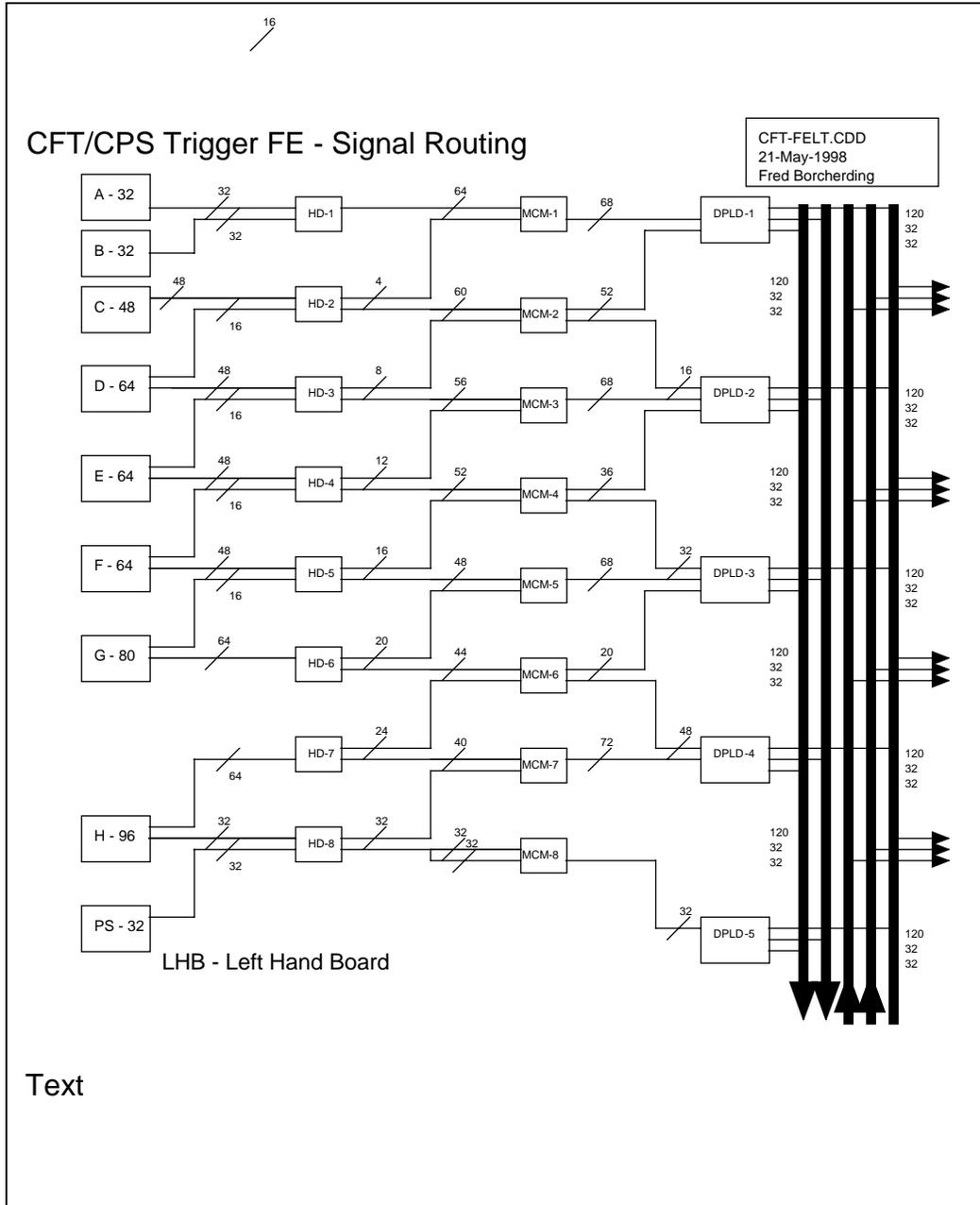


Figure 1: The input timing relationship among the RF Clock, input data, “Parity\_Enable” and “Enable”.

At the receiver daughter board, there will be two clocks, "Ref\_Clock" and "Receive\_Clock". “Ref\_Clock” is input from the motherboard ( MTC05 ) and should be at the accelerator RF frequency. “Receive\_Clock” is the extracted from the input signal, i.e. the above-mentioned RF\_clock from the transmitter. These two clocks have the same frequency but may not be in phase with each other and the phase difference depends on the length of the cable carrying the serial input data. A FIFO can be used to switch the parallel data from the “Receive\_Clock” to “Ref\_Clock”.









## 2.3 The Broadcaster System

As described on §3 , the FET sends information to various subsystems of the Trigger. Among them there are the L1 Trigger Manager and the CFTpp and SVTpp of the L2 Trigger. The information generated by the FET needs to be modified before these systems can use it; the function of the Broadcaster System is to collect the information generated by the FET, preprocess it and send it to the CFTTM and the CFTpp and SVTpp systems.

### 2.3.1 Global description

#### 2.3.2 CFT Receiver / Concentrator Crate

Two physical crates, each with capacity to accommodate up to 21 PC boards, will be used on the implementation of the Broadcaster System. These crates will be located in the xxxxxx of the platform. The expected design parameters for these crates are as follows:

t	Inser	Tabl	Here			
	e					

Each physical crate will be divided into three "logical" crates with a common crate controller.

#### 2.3.2.1 Functionality

A Broadcaster crate does not only holds the necessary boards to communicate downward with the FE T boards and upward with the CFTTM, CFTpp and SVTpp, it also serve as the logical organizer for the mapping of the CFT FE into the 60<sup>0</sup> sectors required by the Si detector organization.

#### 2.3.2.2 The required architecture

As mentioned before, an important function of the Broadcaster System is to make the transition between the five-fold symmetry of the CFT to the six-fold symmetry of the Si Vertex Detector. In other words, the signals from the 80 FE boards that are logically organized into five groups of 16 must be mapped into six sets. Obviously this is only possible if some of the FE boards are split so their signals are sent to two adjacent sets. Using the numbering scheme of the FE boars adopted through this document, the six-fold symmetry requires the following mapping of FE boards into 60<sup>0</sup> sectors:

Geographic sector	Startin g $\Phi$	Ending $\Phi$	Startin g FET	Ending FET
1	270 <sup>0</sup>	330 <sup>0</sup>	61	* 74
2	330 <sup>0</sup>	30 <sup>0</sup>	** 74	** 7
3	30 <sup>0</sup>	90 <sup>0</sup>	* 7	20
4	90 <sup>0</sup>	150 <sup>0</sup>	21	* 34
5	150 <sup>0</sup>	210 <sup>0</sup>	** 34	** 47
6	210 <sup>0</sup>	270 <sup>0</sup>	* 47	60

In the table the FET boards 7,34,47 and 74 are shared boards between two geographical sectors. The way to interpret the usage of the \* is as follows:

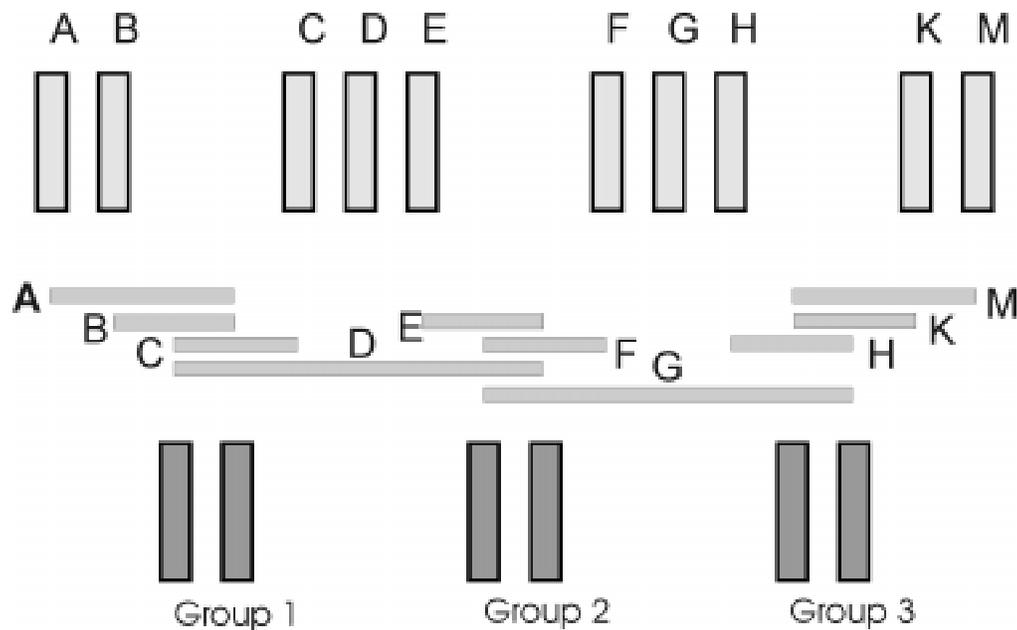
- 1) if the sector number is proceeded by one \* then only one third of the 4.5<sup>0</sup> F pie served by the board is used in the geographical sector to which it is assigned
- 2) if the sector number is proceeded by two \*\* then only two thirds of the 4.5<sup>0</sup> F pie served by the board is used in the geographical sector to which it is assigned.

This rather difficult split of the data proceeding from FET boards 7,34,47 and 74 will done inside the Concentrator Boards and will be described later. From the point of view of the Broadcaster crates these signals must be routed to two adjacent Concentrators. Proper routing is achieved by an proprietary back plane.

### 2.3.2.3 The Back Plane

The proprietary back plane must be able to carry all the signals from all the Receiver Boards assigned to a 60<sup>0</sup> geographical sector to the Concentrator Boards serving that sector. Knowing that each FET board generates data in 16 bits format, it is easy to calculate the total number of traces serving the Concentrator Boards. Each Concentrator Board receives data from 14 FET boards (through the services of the Receiver Boards). Thus, 14x16 = 224 traces are needed to carry this information to the two concentrators serving each 60<sup>0</sup> geographical sector. The following figure shows the proposed layout of the back plane.

Figure 2-1



The assumption made here is that each Receiver Board (RB) serves four FE Boards. These boards are tagged **a, b, c, d, e, f, g, h, k** and **m** and the horizontal lines, also tagged, represent traces in the back plane connecting the corresponding RB with the Concentrators. Note that lines **a, b, c, e, f, h, k**, and **m** connect RB to a single Concentrator group and each represent  $16 \times 4 = 64$  traces. Line **d** and **g** connect RB **d, g** to two Concentrator groups. Specifically, line **d** represents 16 traces going to the first Concentrator group, 32 traces going to the second group of Concentrators and 16 traces serving both. Likewise, line **g** represents 32 traces to the second Concentrator group, 16 traces to the third Concentrator group and 16 traces going to both groups. The total number of traces serving a Concentrator group is

$$N = 64 * 3 + 16 + 16 = 32 + 16 + 64 * 2 + 32 + 16 = 224.$$

This organization of the boards in the crate results in minimal length of the traces connecting Receiver Boards and Concentrators.

### 2.3.3 CFT Receiver Board

#### 2.3.3.1 Functional Description

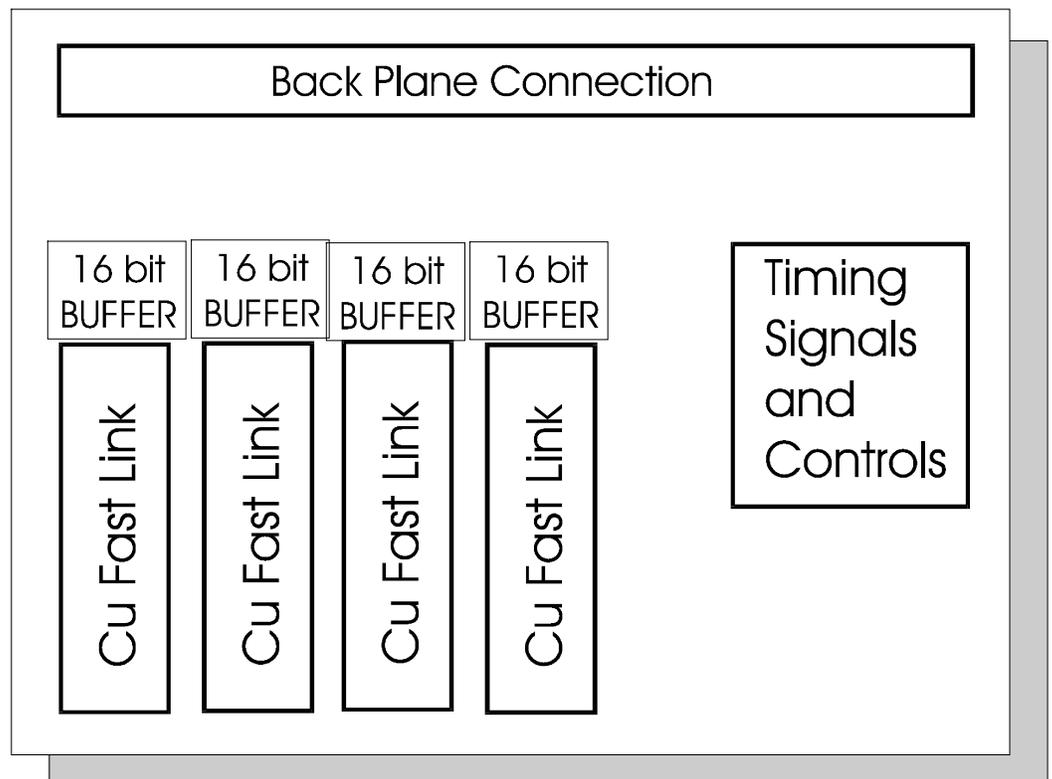
As its name indicates, the principal function of the Receiver Board (RB) is to receive information sent by the CFT FE boards. This information is then transferred to the Concentrator Boards through a back plane. Each RB receives information via Cu Fast Link connections from four different CFT FE. This information is different depending in which mode the CFT Trigger is as described in the § dealing with the

FE description. It is important to recall here the broad differences. As long as the L1 Accept has not been asserted, the RB receives information regarding the crossing number and the number of tracks found by the Track Finding Algorithm. When a L1 Accept occurs, the information arriving to the RB changes to show track information in sufficient detail to be utilized by the L2 Trigger. Regardless of the data arriving, the RB role could be thought of as a totally passive.

### 2.3.3.2 Board Architecture

The architecture of the RB is very simple. A block diagram is shown in Fig. Mmm

Figure 2-2



The ti

The timing signals are those needed by the Cu Fast Link and the controls are to present to the back plane the information in a timely fashion.

### 2.3.4 CFT L1 Concentrator Board

There are four Concentrator Boards in the system sending information the CFTTM. Their functionality and implementation is described on the following §§.

**2.3.4.1 Functional Description**

The CFTL1 Concentrator board collects specific information generated by the FET boards and transfers it, after proper modifications to the CFTTM. The information received from each FET is shown schematically in Fig. ##

**Table 2-1**

# A1 (4bits)	# B1 (4bits)	# C1 (4bits)	# D1 (4bits)
# A2 (4bits)	# B2 (4bits)	# C2 (4bits)	# D2 (4bits)
# A3 (4bits)	# B3 (4bits)	# C3 (4bits)	# D3 (4bits)
# A4 (4bits)	# B4 (4bits)	# C4 (4bits)	# D4 (4bits)
Padding bits		Tick Number	
Turn Number			

Were the numbers **1,2,3,4** correspond to the four Pt ranges defined in the CFT Trigger and the letters **A, B, C, D** refers to the situations when:

- A the track is isolated and tagged by the CPS
- B the track is isolated but not tagged
- C the track(s) is (are) tagged but not isolated
- D the track(s) is (are) neither tagged nor isolated.

The information collected needs to be modified so the CB can report to the CFTTM the total number of tracks found in each category for the 60<sup>0</sup> geographical sector that the CB encompass assuring that no track is counted more than once. This presents no problem for al FE sectors except for those whose information is given to more than one CB. I decision must to be made for these. Referring to Table ## presented in the § 2.3.2.3 it appears that the logical decision is to associated, for these purposes, the FET as shown on **Table 4-2**

**Table 2-2**

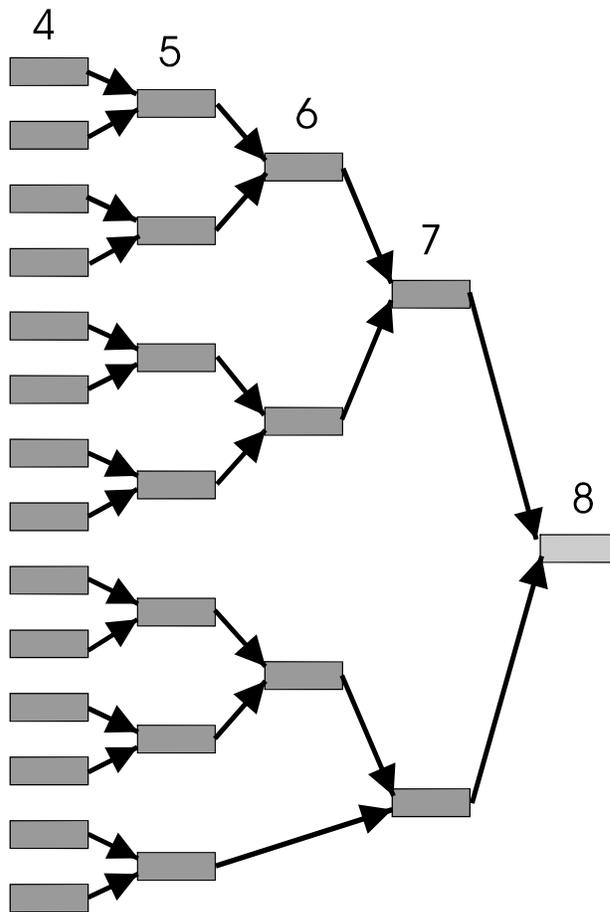
FET Sector	Associated Geographic Sector	Total Extent
<b>74 and 7</b>	330 <sup>0</sup> - 30 <sup>0</sup>	63.0 <sup>0</sup>
<b>34 and</b>	150 <sup>0</sup> - 210 <sup>0</sup>	63.0 <sup>0</sup>

<b>47</b>		
-----------	--	--

Note that these Geographic Sectors became  $63.0^{\circ}$  in lieu of  $60^{\circ}$ . Conversely, the other four Geographic Sectors are reduced to  $58.5^{\circ}$ .

With these changes in mind, the functionality of the L1CB is reduced to add the information of the 13 or 14 FET and report the end result to the CFTTM. A ladder adder as shown below achieves this.

**Figure 2-3**



The information sent to the CFTTM has the following structure

<b>Pt1,isolated and tagged. 6 bits</b>	<b>Pt1,isolated, not tagged. 6 bits</b>
<b>Pt1, tagged not isolated. 6 bits</b>	<b>Pt1,neither isolated nor tagged. 6 bits</b>
<b>Pt2,isolated and tagged. 6 bits</b>	<b>Pt1,isolated, not tagged. 6 bits</b>
<b>Pt1, tagged not isolated. 6 bits</b>	<b>Pt1,neither isolated nor tagged. 6 bits</b>
<b>Pt3,isolated and tagged. 6 bits</b>	<b>Pt3,isolated, not tagged. 6 bits</b>
<b>Pt3, tagged not isolated. 6 bits</b>	<b>Pt3,neither isolated nor tagged. 6 bits</b>
<b>Pt4,isolated and tagged. 6 bits</b>	<b>Pt4,isolated, not tagged. 6 bits</b>
<b>Pt4, tagged not isolated. 6 bits</b>	<b>Pt4,neither isolated nor tagged. 6 bits</b>

As result the information send to the CFTTM is condensed into sixteen 6 bit bytes from the original 52 (56) 16 bit bytes. Because the output of the ladder adder is 8 bits a truncation of the data needs to be performed. In addition the code 111111 will be consider an "non valid code".

#### 2.3.4.2 Board Architecture

The L1Concentrator Board is implemented in a multilayer 9U board. The mayor functional blocks are shown on Fig. Xxxx and a more detailed block diagram of the adder structure is shown on Fig. XXX.

It is worthwhile to note that there are some standard functions used in the implementation of the L1Concentrator. These standard functions are also implemented in a standard manner. This reduces the need for EE development time and it is consider important enough to sacrifice for some flexibility in the design. As an example we can mention the implementation of the data structure used to send data from the L1Concentrator to the CFTTM. It was consider to be a worthwhile reduction in effort the ability to use the Trigger Manager Cards developed by the  $\mu$  system instead of designing our own. This affects the way data can be coded. The  $\mu$  system expects to receive a 96-bit stream of data as 16 frames of 6 bits each. The logical data structure generated in the L1Concentrator calls for a 128-bit stream of data codes as 8 frames of 16 bits each. To accommodate the  $\mu$  system data stream several things need to be donned before data is presented to the Cu Fast Serial Link:

- 1) data coming from the ladder adders must be truncated from 8 bits to 6 bits
- 2) data needs to be stored in a FIFO before it can be presented to the Cu Link

In other words, the adoption of the  $\mu$  system type of TM card haves pros and cons. Some of these are listed below.

##### **Pros.-**

Minimum development time and resources

Less proprietary PC Boards, thus, easier maintenance and debugging

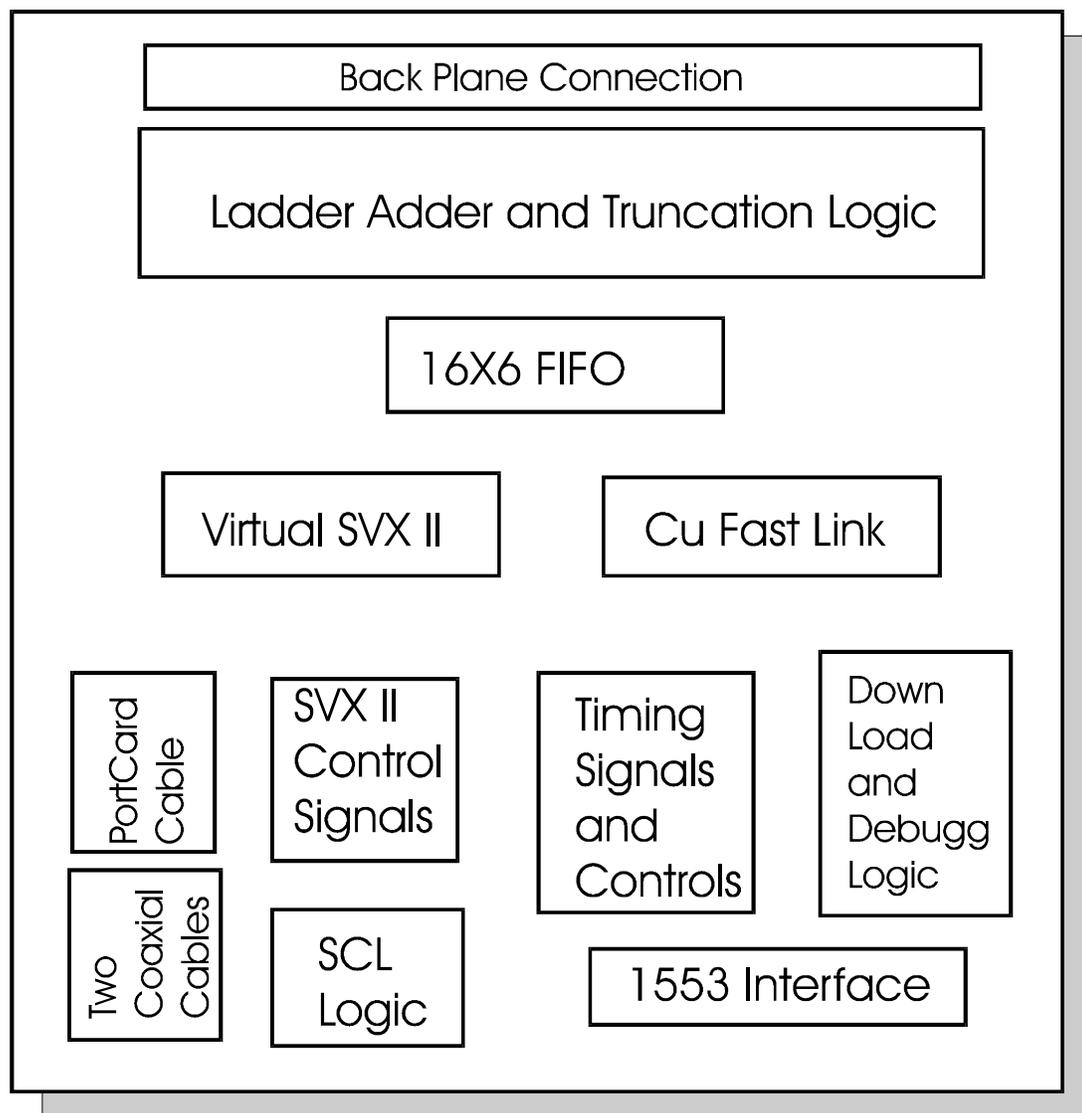
**Cons.-**

Incurred complexity in the design of the L1Concentrator card

Need for more logic and more real state to implement the additional functions

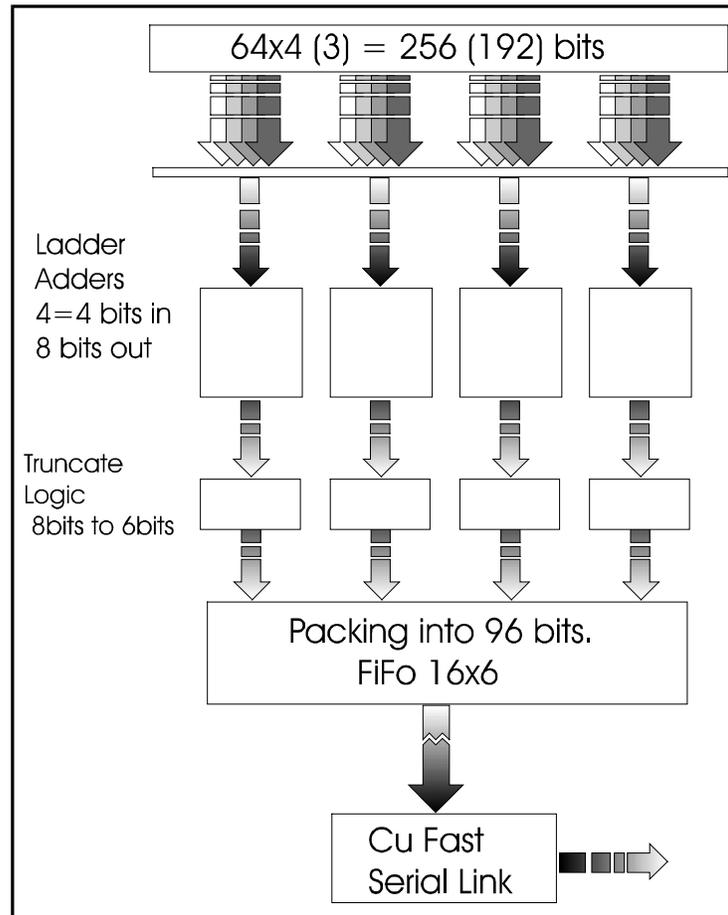
Incurred additional delay in the transfer of data to the CFTTM card. This additional time is expected to stay below 60ns.

**Figure 2-4**



The connection to the back plane is achieved through Eurocard or Fast Bus type connectors.

The Ladder Adder and truncation logic will be implemented in a FPLD type device. The hardware equivalent of such implementation is shown on Fig. xxxx



Each of the four Ladder Adders is an implementation of the logic shown in Fig. Nnnn. The FIFO is required to present the data to the Cu FSL in 16 bits bytes.

## 2.3.5 CFT L2pp Concentrator Board

### 2.3.5.1 Functional Description

### 2.3.5.2 Board Architecture

### 2.3.6 Comments

## **2.4 CFT Trigger Manager, CFTTM**

### **2.4.1 Functional Specification**

The CFTTM receives a set of 16 numbers from each of eight CFTcon and sums them. After the sums are formed each is compared to a cut number downloaded from the trigger framework. If the sum in any of the 16 meets its requirement the corresponding bit in the L1 AND-OR network term is set. The meaning of the individual AND-OR terms is given in table 1.

The Muon Trigger Manager, MTM, board without modification is used as the CFTTM board. And the CFTTM resides in the Muon Trigger Crate located on the east side of the detector platform. All of the external I/O with the exception of the eight links to the CFTcon are supplied and maintained as part of the Muon L1 system. The unique software used in the CFTTM's PLDs is provided and maintained by the CFT trigger group while the common software is provided and maintained by the Muon L1 group.

### **2.4.2 Implementation**

According to the standard of Muon Trigger boards, the CFTTM is equivalent to a CFT Flavor Board plugged into a Muon Trigger Card ( MTCxx ). The MTCxx card is uniform throughout the L1 Muon Trigger system and also the CFTTM. Different inputs, outputs and algorithms are accommodated by the use of a Flavor Board connected to a MTCxx. The Flavor Board is named as such that it changes the nature or flavor of the Trigger Card in question. To change the MTM into CFTTM, we only need to modify the trigger logic in the FPGA's on the Muon Trigger Flavor Board ( MTFB ) to a CFT Flavor Board.

The physical connection between the CFTcon and CFTTM will be the same as the connection between CFT FE and MTC05 as both MTC05 and CFTTM use essentially the same MTCxx. For each trigger term from each CFTcon, the information transferred to the CFTTM is the total number of track found, which has a maximum of 50 and therefore only needs to occupy 6 bits. The total number of bits from CFTcon to CFTTM is therefore  $8 \times 16 \times 6$  bits, which is only half of that for MTM. The CFTTM logic for making trigger decisions is expected to be simpler than the MTM trigger logic and should be easily accommodated and implemented by Altera EPLD, which is what the MTM would use.

## **3. Central Fiber Tracker Stereo System, CFT Stereo**

The Central Fiber Tracker Stereo system is a small subset of the CFT/CPS system. The major differences are, first it has no L1 Trigger, second it has no L2 Trigger, and third it has no link to the Muon L1 system. The result is that the system has only FE boards and crates and the command system for the

L3 readout only. The analog part of each Stereo FE board is the similar but not the same as for the CFT Trigger FE board. It differs in that it has no CPS channels and therefore none of the analog inputs are split into two. It does use the same board layout as the CFT/CPS trigger board but the unused parts of the board are not populated.

**3.1 CFT Stereo System Overview**

The CFT Stereo system has a L3 readout only. During normal running the signals are stored in the SVX pipeline. On a L1 accept the SVX digitizes the information and reads it out through the Sequencer boards to a VRB crate where it is available to the DAQ system.

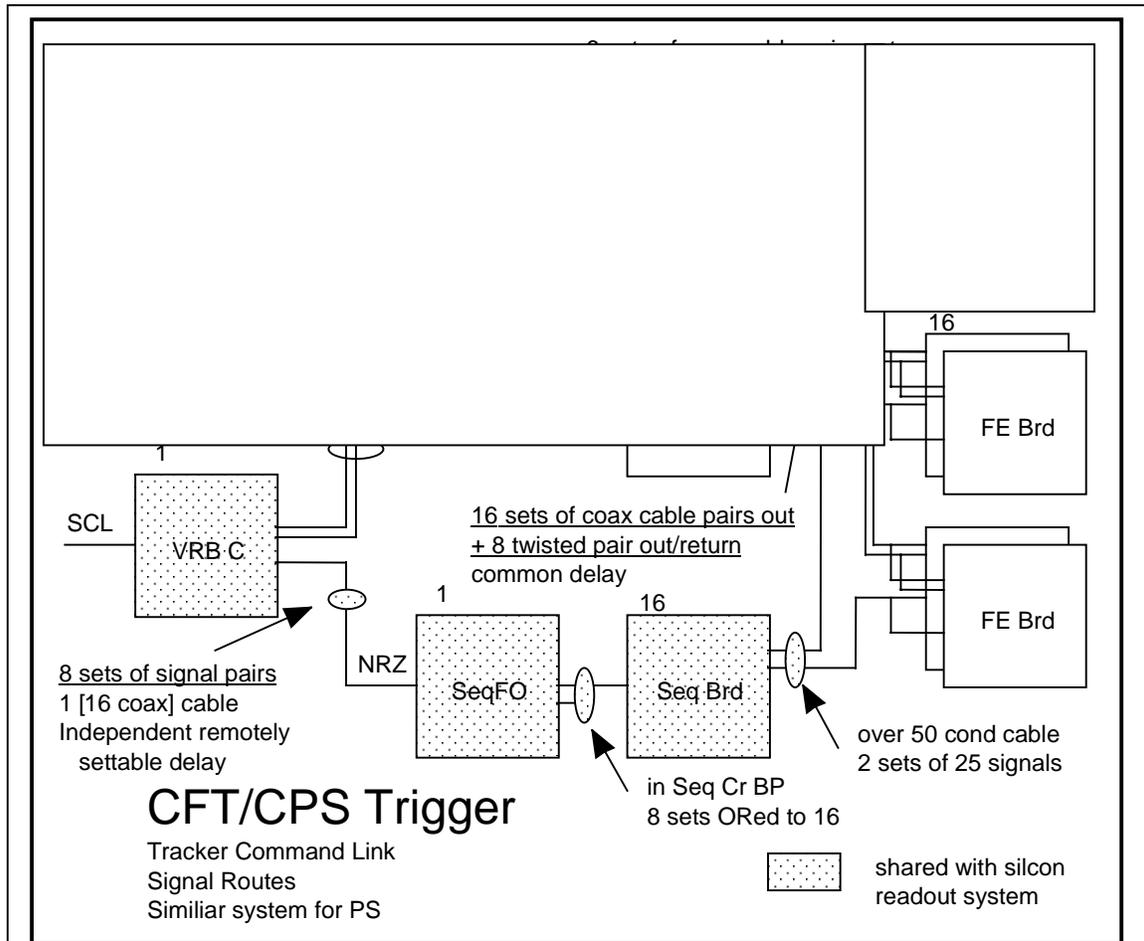


Figure 6. Tracker command link system. This is an overall view of the entire system.

**3.1.1 Functional Description**

During ...

**3.1.1.1 Geometry and Definitions**

To ensure consistent results between the FE trigger, the online, the offline and the Monte Carlo processing a unified coordinate system and system of definitions must be adopted. This section describes the coordinate system and definitions. A detailed geometry of the detector is given elsewhere.

The  $D\emptyset$  standard coordinate system is used...

**3.1.2 System Architecture****3.1.2.1 Hardware Inventory**

The CFT/CPS Trigger system has;

1	GS with SCL
1	VRB Crate
1/2	Sequencer Crate
5	Front End Crates
75	FE Boards, 38 RHB & 37 LHB

Each VRB crates has;

1	VRB Controller board with SCL receiver
10	VRB Boards
10	VEPA Boards
40	Optical link receivers (from Seq)

Each  $\frac{1}{2}$  Sequencer crate has;

$\frac{1}{2}$	Sequencer Controller Board with SCL receiver
10	Sequencer boards
40	Optical link transmitters (to VRB), 4 per board
38	50-Conductor Cables, 4 per board

Each FE crates has;

8	Right Hand FE Trigger Boards
8	Left Hand FE Trigger Boards
8	BP Connectors for 50-Conductor Cables
8	BP Connectors for Cryo I/O

Each FE board has;

1	1553 Node to receive down load
1	SVX String
$\frac{1}{2}$	50-Conductor Cable from Sequencer
1	Analog and Serial Clock generator
8	MCM, each with 1 SVX and 4 SIFT chips

### **3.1.2.2 Hardware description**

Figure 1 shows the overall data flow of the system. It could also be considered a crate level diagram of the system since each box corresponds to one or more crates.

The data starts in each of the 80 FE boards located on the VLPC cryostat in the center platform. During L1 live time each FE continuously transmits information for each crossing, within the time of one crossing, to two different destinations.

## Preshower Trigger System, PS Trigger

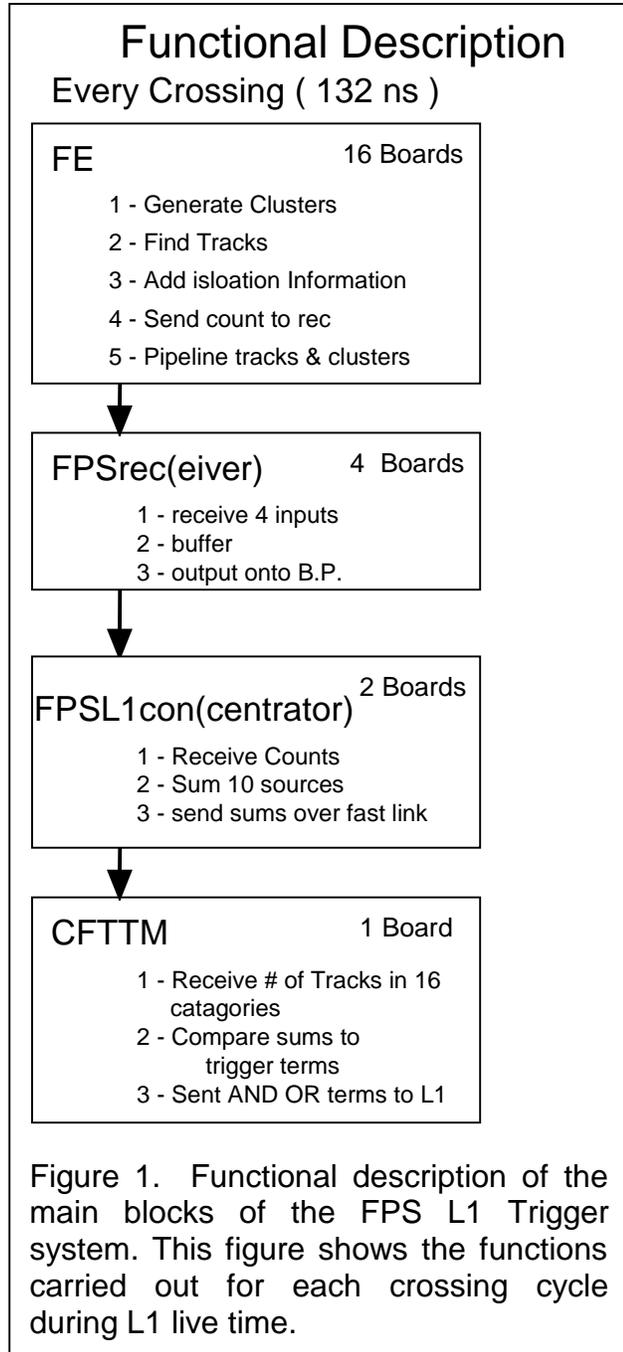
The Preshower Trigger system, which includes all of the Forward Preshower channels and the Central Preshower stereo channels, is similar to that of the CFT/CPS in most ways. The major differences are, first it has fewer FE boards, second it has a different track algorithm, and third it has no link to the Muon L1 system. Also the CPS part of the system has no L1 trigger capabilities. In addition in each of the PS channels the signal is divided into a low and high range and both are digitized. Therefore each of these FE boards has 512 sets of signal dividers on the board and twice that number of SIFT and SVX channels and MCM's.

### 3.2 PS Trigger System Overview

The Preshower, PS, trigger system provides the means for triggering at level 1 on the information from the FPS detector only and supplies information for the level 2 Preshower Trigger Preprocessor, PSpp, from both detectors. It also supplies, from the FE boards, the raw data from the VLPC channels for the level 3 read out.

*For the L1 FPS Trigger it counts the number of clusters found. These clusters are tagged with the absence or presence of a MIP in the upstream layers to distinguish between electrons and photons. A loose match is also required between clusters found in the U and the V layers. The numbers of clusters found is forwarded to the FPS Trigger*

*Manager, FPSTM, for the global L1 decision. For the L2 preprocessor the system pipelines cluster information indexed by eta and  $\phi$  in the forward and*



only  $\phi$  in the central, and upon the receipt of a L1 accept compresses, sorts and forwards this information to the PSpp.

### 3.2.1 Functional Description

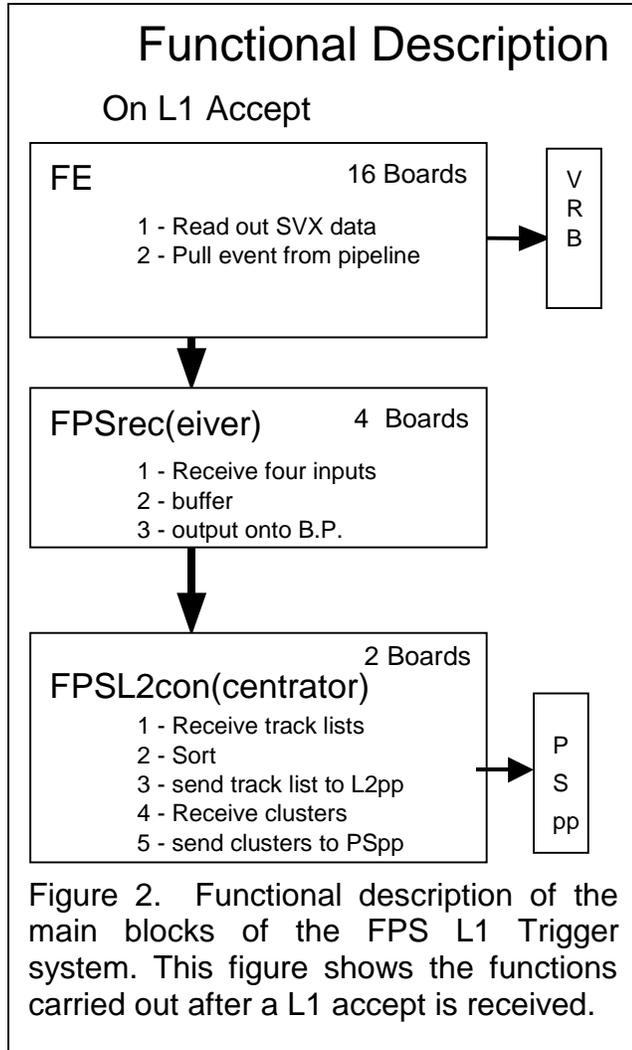
During normal running the operation of the system can be separated into four function blocks as shown in figure 1. The strips from each of the sixteen physical segments of the detector are routed to a single FE board so no sharing of hit information across the back plane is necessary.

Independently in each of the U and V back layers clusters are found. Both the location and width of each cluster is found. For each cluster found a mask whose position and size are dependent on the cluster position and width, is placed over the front layer. If any strip within that mask has a MIP the cluster is tagged as an e-type cluster. The found clusters are grouped into two groups by eta, called the high-eta and a low-eta. If the U-strip high-eta group has at least 1 e-type cluster and the V-strip high-eta group has at least 1 e-type cluster the number of clusters for both U and V strips are recorded. Note that since the U and V strips cross each other at an angle

some of the V-strip are used in matching both high and low eta types. This matching is done for both e-type and non-e-type, and for high-eta and low-eta groups and results in eight numbers. These numbers are then sent to the PSreceiver board.

The cluster information is kept at the FE for use by the L2. The cluster information for all found clusters, even those that didn't contribute to the counts outlined above are placed into a pipeline of the FE board for retrieval on a L1 Accept for both the L2 and L3 readouts.

The FPS receiver boards, the second box in figure 1, each receives information from several FE boards over a serial link and puts this information onto parallel links, which pass through the crate back plane and terminate in the



FPS L1 Concentrator boards. These boards which are the third box in figure 1, receive the individual counts and sum them into a single set per board and send this set out over another serial link to the FPS Trigger Manager, the bottom box. The trigger manager sums the several sets it receives. At this point the individual sums, which represents counts over the entire FPS detector, are compared to cuts set by the host and are used to set bits in the AND/OR cable to the trigger manager.

Whenever a L1 accept for the system is issued it stops normal processing and shifts to L2 readout mode. The functional description for this can be divided into three blocks as shown in figure 2. First in each FE the data for the correct crossing is pulled out of the pipeline and sent to the FPS receiver boards. This data is also placed into the virtual SVX, VSVX, for inclusion in the L3 readout stream. Also at each FE the raw data is pulled out of each SVX pipeline, digitized and readout out for the L3. The L3 readout system is shared with the silicon system and is not detailed in this document.

The FPS receiver boards operate in the same manner as for normal readout but now a different board, the FPS L2 concentrator board pulls the data off the back plane busses. The L2 concentrator board combines the tracks from several front ends into a single list and sends a truncated list to the L2 preprocessors. While the list is necessarily truncated to keep the system deterministic, MC results have shown that the list is long enough so that truncation adds less than 1% to the inefficiency of the trigger.

### **3.2.1.1 Geometry and Definitions**

To ensure consistent results between the FE trigger, the online, the offline and the Monte Carlo processing a unified coordinate system and system of definitions must be adopted. This section describes the coordinate system and definitions. A detailed geometry of the detector is given elsewhere.

The  $D\emptyset$  standard coordinate system is used.

The FPS is divided into two parts. One at the North end of the interaction region and one at the South. Each of these parts has 16 sectors and each sector subtends 22.5 degrees. These sectors are separate physical modules that overlap slightly and contain four layers of scintillating strips.

### **3.2.1.2 Trigger Sectors**

For a high speed trigger such as that needed for level 1 it is necessary to have all the data needed to make a trigger decision concentrated at one location. This trigger achieves this by dividing the global trigger into a series of local triggers each of which are independent of one another. This trigger finds tracks which propagate through all ..

The sectors are arranged in 2 FE crates in

## **3.2.2 System Architecture**

### **3.2.2.1 Hardware Inventory**

The FPS/CPS Trigger system has;

GS with SCL  
VRB Crate  
1/2 Sequencer Crate  
FPS Front End Crates, 8 cassette crates  
CPS Front End Crates, 3 cassette crates  
FPS FE Boards, 16 RHB & 16 LHB  
CPS FE Boards, 5 RHB & 5 LHB  
Broadcaster Crates  
1\* MTM Crate

Each VRB crates has;  
VRB Controller board with SCL reciever  
VRB Boards  
VEPA Boards  
Optical link recievers (from Seq)

Each 1/2 Sequencer crates has;  
1/2 Sequencer Controller Board with SCL receiver  
Sequencer boards  
Optical link transmitters (to VRB), 4 per board  
50-Conductor Cables, 4 per board

Each FPS FE crate has;  
Right Hand FPS FE Trigger Boards  
Left Hand FPS FE Trigger Boards  
BP Connectors for 50-Conductor Cables  
BP Connectors for Cryo I/O

Each CPS FE crate has;  
3(2) Right Hand FE CPS Trigger Boards  
3(2) Left Hand FE CPS Trigger Boards  
BP Connectors for 50-Conductor Cables  
BP Connectors for Cryo I/O

Each FE board has;  
Serial link to broadcaster crate  
1553 Node to receive down load  
SVX Strings  
50-Conductor Cable from Sequencer  
Analog and Serial Clock generator  
MCM, each with 1 SVX and 4 SIFT chips

Each Broadcaster crate has;  
Controller board  
L1 Concentrator Board  
L2 Concentrator Boards

Receiver Boards  
Copper Serial link receivers (from FE)

Each Controller Board has;  
50-conductor cable receiver  
1553 Node

Each Receiver Board has;  
Copper Serial link receivers

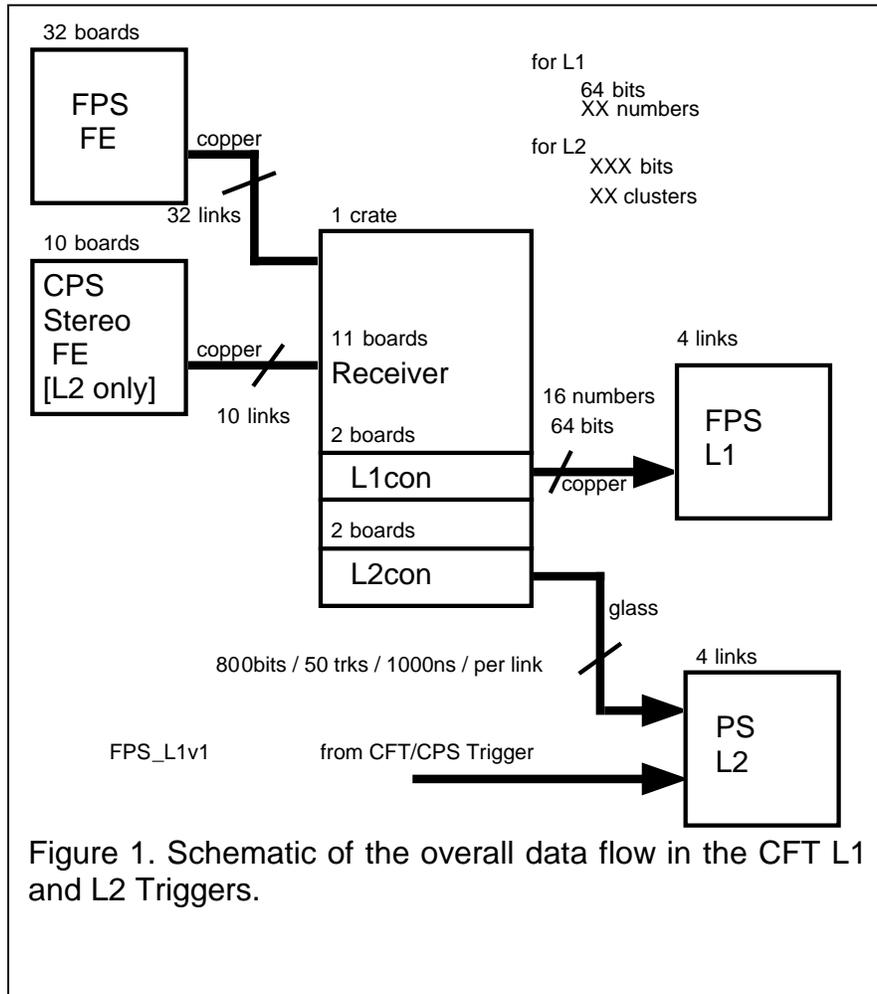
Each L1 Concentrator Board has;  
Optical Serial link transmitter

Each L2 Concentrator Board has;  
Optical Serial link transmitter

### **3.2.2.2 Hardware description**

Figure 1 shows the overall data flow of the system. It could also be considered a crate level diagram of the system since each box corresponds to one or more crates.

The data starts in each of the 80 FE boards located on the VLPC cryostat in the center platform. During L1 live time each FE continuously transmits information for each crossing, within the time of one crossing, to two different destinations. One link is to the muon L1 located on the east platform and consists of 80 fast serial copper links. The other link, which serves a dual function, uses the same type of hardware and goes to eight crates on the west



platform. During L1 live time this second link carries track counts from the CFT FE. And from each of these crates fast serial links transmit data to the CFT Trigger Manager, CFTTM, in the same crate as the Muon Trigger Manager on the east platform. When a L1 accept is received this link transmits track lists from each FE to the same four crates. And from there the track lists are transported to L2 preprocessors located in the mobile counting house over a fast optical serial link. Figure 3 is a functional diagram of the system during L1 times and figure 4 is a functional diagram of the system upon a L1 accept.

### 3.2.2.3 Data Transfer

3.2.2.3.1 From FE to Concentrator

3.2.2.3.1.1 L1 Transfer

Each FE sector counts the number of matched clusters in 8 categories. The count of clusters tagged as an electron or gamma candidate for each of the U and V stereo views for each of high and low eta is made in the FE and sent to the Broadcaster crate. Each number is 6 bits for a total data size of 64 bits.

The meaning of the numbers transmitted is:

Number	Count of
1	U-cluster / e-tag / eta-low
2	U-cluster / e-tag / eta-high
3	U-cluster / g-tag / eta-low
4	U-cluster / g-tag / eta-high
5	V-cluster / e-tag / eta-low
6	V-cluster / e-tag / eta-high
7	V-cluster / g-tag / eta-low
8	V-cluster / g-tag / eta-high

The data packet format is:

Number	Count of
1	U-cluster / e-tag / eta-low
2	U-cluster / e-tag / eta-high
3	U-cluster / g-tag / eta-low
4	U-cluster / g-tag / eta-high
5	V-cluster / e-tag / eta-low
6	V-cluster / e-tag / eta-high
7	V-cluster / g-tag / eta-low
8	V-cluster / g-tag / eta-high

3.2.2.3.1.2 L2 Transfer

3.2.2.3.2 From Broadcaster to Preprocessors

**4. Forward Proton Detector, FPD**

XXX

**4.1 FPD System Overview**

XXX

**4.1.1 Functional Description**

XXX

**4.1.2 System Architecture**

XXX

## 5. Tables

Term Number	Description of Term			
Term_15		CFT above	Highest	Pt Threshold
Term_14		CFT above	High	Pt Threshold
Term_13		CFT above	Medium	Pt Threshold
Term_12		CFT above	Low	Pt Threshold
Term_11		CFT/CPS above	Highest	Pt Threshold
Term_10		CFT/CPS above	High	Pt Threshold
Term_9		CFT/CPS above	Medium	Pt Threshold
Term_8		CFT/CPS above	Low	Pt Threshold
Term_7	isolated	CFT above	Highest	Pt Threshold
Term_6	isolated	CFT above	High	Pt Threshold
Term_5	isolated	CFT above	Medium	Pt Threshold
Term_4	isolated	CFT above	Low	Pt Threshold
Term_3	isolated	CFT/CPS above	Highest	Pt Threshold
Term_2	isolated	CFT/CPS above	High	Pt Threshold
Term_1	isolated	CFT/CPS above	Medium	Pt Threshold
Term_0	isolated	CFT/CPS above	Low	Pt Threshold

Table 1. The definition, version 1.0, of the AND-OR terms from the L1 CFTTM. The NOMINAL Pt threshold values are; Highest > 8 GeV > High > 5 GeV > Medium > 3 GeV > Low > 1.5 GeV.

Format of Data Words from CFT Front End				
Bit #		Field	Bit #	Use
15	Most Sig.	0	-	Track Found Flag [1=found]
14		0	-	High CPS Threshold Track Match
13		0	-	Low CPS Threshold Track Match
12		0	-	spare
11		0	-	spare
10		0	-	Sign of the Pt for Track
9		3	msb	Inner (A) Layer Offset from Outer Layer Bin
8		2		
7		1		
6		0	lsb	
5		5	msb	Outer (H) Layer Phi Bin
4		4		
3		3		
2		2		
1		1		
0	Least Sig.	0	lsb	

Format of Data Words from CFT Front End				
Bit #		Field	Bit #	Use
19	Most Sig.	0	-	Track Found Flag [1=found]
18		0	-	High CPS Threshold Track Match
17		0	-	Low CPS Threshold Track Match
16		0	-	spare
15		0	-	spare
14		0	-	Sign of the Pt for Track
13		3	msb	Inner (A) Layer Offset from Outer Layer Bin
12		2		
11		1		
10		0	lsb	
9		9	msb	Extended Outer (H) Layer Phi Bin
8		8		
7		7		
6		6		
5		5		Outer (H) Layer Phi Bin
4		4		
3		3		
2		2		
1		1		
0	Least Sig.	0	lsb	

Table 2. Definition of bits for the 16(20)bit CFT/CPS track word. Six(ten) bits are used to identify the phi position. Five bits are used to identify the momentum including its sign. Four bits are used to identify matches with the CPS. And one bit is used to tag the word as containing valid track information.

Offset	Pt Index	Min	Mean	Max
0	0000	18.00	21.40	
1	0001	9.00	16.90	
2	0010	6.50	11.00	21.00
3	0011	4.50	6.80	10.50
4	0100	4.00	5.00	7.00
5	0101	3.25	3.90	5.00
6	0110	2.75	3.30	4.00
7	0111	2.50	2.80	3.50
8	1000	2.20	2.40	2.80
9	1001	1.80	2.20	2.50
10	1010	1.80	1.90	2.20
11	1011	1.60	1.76	2.00
12	1100	1.50	1.62	1.80
13	1101	1.40	1.53	1.60
14	1110	-	-	-
15	1111	-	-	-

Table 3. Track Pt as a function of bin offset. The first column is the bins offset, the second is the Pt bin index, the third through fifth columns are the minimum, mean and maximum Pt's for a track with the given offset. The numbers are from histograms of the Pt which were generated by a MC which generated tracks over all outer bins for a sector.

Bin # for 44 Bins	Binary Code	Bin # for 44 Bins	Binary Code
47	1011 11	23	0101 11
46	1011 10	22	0101 10
45	1011 01	21	0101 01
44	1011 00	20	0101 00
43	1010 11	19	0100 11
42	1010 10	18	0100 10
41	1010 01	17	0100 01
40	1010 00	16	0100 00
39	1001 11	15	0011 11
38	1001 10	14	0011 10
37	1001 01	13	0011 01
36	1001 00	12	0011 00
35	1000 11	11	0010 11
34	1000 10	10	0010 10
33	1000 01	9	0010 01
32	1000 00	8	0010 00
31	0111 11	7	0001 11
30	0111 10	6	0001 10
29	0111 01	5	0001 01
28	0111 00	4	0001 00
27	0110 11	3	0000 11
26	0110 10	2	0000 10
25	0110 01	1	0000 01
24	0110 00	0	0000 00

Table xxx. Translation of PHI bin index in the FE to bin number. The Phi bin

## Coordinate System

Right hand system.

+Y is up

+X is horizontal and to the West

+Z is horizontal and South

Proton downstream is increasing Z

Phi = zero along +X axis

Increasing Phi is +X axis to -Y axis

## CFT Trigger

Sector index is from 1 to 80

Sector 1 is from  $\Phi = \text{zero}$  to  $\Phi = 2\pi/80$

Sector n is from  $\Phi = 2\pi(n-1)/80$  to  $2\pi(n)/80$

Phi index within a sector is from 1 to 44

Phi index m in sector n is from

$$\Phi = (m-1)(n-1)(2\pi/80)/44 \text{ to } m(n-1)(2\pi/80)/44$$

For a POSITIVE Pt track the  
Phi value INCREASES as the  
radius INCREASES

## External I/O for the CFT Concentrator System

Name	From	To	via	Discription
<b>Input</b>				
53MHz Clock		L1con Brd	coax	53MHz Accelerator RF Clock
7.6MHz Clock		L1con Brd	coax	1/7 of above marking 132ns crossing positio
RESET		L1con Brd	coax	Reset the System
Crossing Indicator		L1con Brd	coax	Signals Crossing present
Mode Control	Host	L1con Brd L2pp con		1553 1553
FE Data N	FE Sector N	Reciever Brd	Cu Serial	
<b>Output</b>				
L1 Sums	L1con	CFTTM	Cu Serial	
L2pp Track Data	L2ppcon	L2pp	GI Serial	
L3 Data	L1con & L2ppc SVX Sequencer			50 cond cbl
Status Blk	Host	L1con L2ppcon		1553 1553
Diagnostic Blk	Host	L1con L2ppcon		1553 1553

## Internal I/O for the CFT concentrator System

External I/O for the CFT FE System

Name	From	To	via	Discription
<b>Input</b>				
53_Clock		FE BP	coax	53MHz Accelerator RF Clock
7_Clock		FE BP	coax	132ns crossing clock
RESET		FE BP	coax	Reset the System
Crossing		FE BP	coax	Signals Crossing present
PRST		FE BP	coax	Reset the SIFT Preamp
SVX_Mode	SVX Squ	FE Brd	Cable	
SVX_Control	SVX Squ	FE Brd	Cable	
SVX Download	SVX Squ	FE Brd	Cable	
PLD Download	Host	FE Brd	1553	
<b>Output</b>				
FE Data N Sums Track Lists	FE Brd	Reciever Brd	Cu Serial	
FE Muon Data	FE Brd	Muon L1	Cu Serial	
Status Blk	FE Brd	Host	1553	

Name	From	To	via	Discription
<b>Input</b>				
53MHz Clock		FE BP	coax	53MHz Accelerator RF
7.6MHz Clock		FE BP	coax	1/7 of above marking
RESET		FE BP	coax	Reset the System
Crossing Indicator		FE BP	coax	Signals Crossing pres
Mode Coni	SVX Squ	FE Brd	Cable	
SVX Contr	SVX Squ	FE Brd	Cable	
SVX Down	SVX Squ	FE Brd	Cable	
PLD Down	Host	FE Brd	1553	
<b>Output</b>				
FE Data N Sums	FE Brd	Reciever E	Cu Serial	

Internal I/O for the CFT FE System

<b>Input</b>	<b>to</b>	<b>Discription</b>
VDD_A	SIFT (all)	+5V Analog Power
VSS_A	SIFT (all)	GND Analog
VDD_D	SIFT (all)	+5V Digital Power
VSS_D	SIFT (all)	GND Digatal
PCASP	SIFT (all)	Preamp Cascade Volt
PVI	SIFT (all)	Preamp VI Volt
NCAS1	SIFT (all)	Preamp Cascade Volt
NCAS2	SIFT (all)	Preamp Cascade Volt
VSFN	SIFT (all)	Anlog Buffer Volt
VICDS	SIFT (all)	
DVI	SIFT (all)	Digital VI
DCAS	SIFT (all)	Digital Cascade Volt
VREF	SIFT (all)	SVX Reference Volt
PRST	SIFT (all)	Preamp Reset
READ	SIFT (all)	Transfer Qout to SVX
SH	SIFT (all)	Transfer Qout to Hold in SVX
DRST	SIFT (all)	Discriminator Reset
PCLMP	SIFT (all)	Reset SIFT to SVX level
VH_DR_A	SIFT_A1/2	Dynamic Range Voltage
VL_TH_A	SIFT_A1/2	High Threshold Volt Set
VH_TH_A	SIFT_A1/2	Low Threshold Volt Set
GAIN1_A	SIFT_A1/2	Discriminator Gain Setting
GAIN2_A	SIFT_A1/2	Qout Gain Setting
GATEOVR_A	SIFT_A1/2	Defeat Gate on Qout
VH_DR_B	SIFT_B3/4	Dynamic Range Voltage
VL_TH_B	SIFT_B3/4	High Threshold Volt Set
VH_TH_B	SIFT_B3/4	Low Threshold Volt Set
GAIN1_B	SIFT_B3/4	Discriminator Gain Setting
GAIN2_B	SIFT_B3/4	Qout Gain Setting
GATEOVR_B	SIFT_B3/4	Defeat Gate on Qout
QIN_A1(2:19)	SIFT_A1	Q Inputs for SIFT A1
QIN_A2(2:19)	SIFT_A2	Q Inputs for SIFT A2
QIN_B3(2:19)	SIFT_B3	Q Inputs for SIFT B3
QIN_B4(2:19)	SIFT_B4	Q Inputs for SIFT B4
<b>Output</b>	<b>from</b>	<b>Discription</b>
VOUT_A1(2:19)	SIFT_A1	Disc Outputs for SIFT A1
VOUT_A2(2:19)	SIFT_A2	Disc Outputs for SIFT A2
VOUT_B3(2:19)	SIFT_B3	Disc Outputs for SIFT B3
VOUT_B4(2:19)	SIFT_B4	Disc Outputs for SIFT B4

## MCM I/O For SIFTS

Name	Discription
------	-------------

6. Misc. Figures

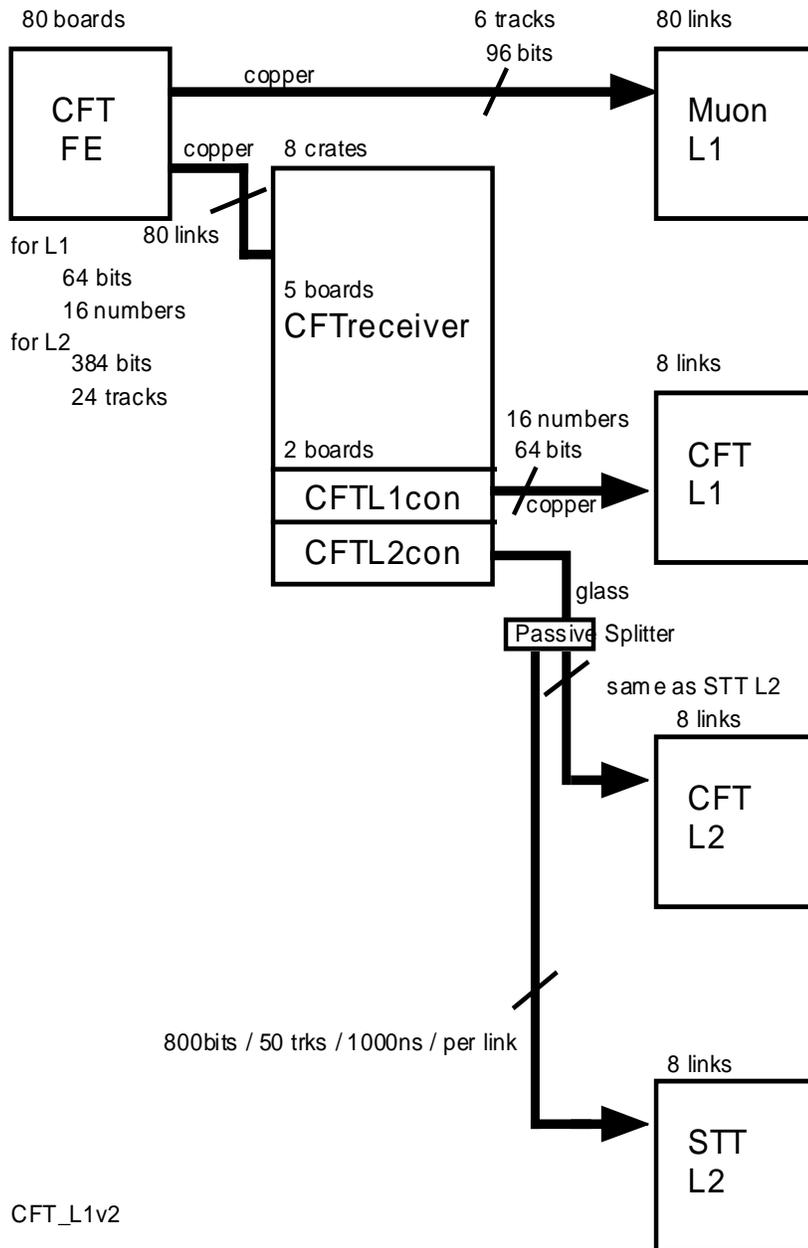


Figure 1. Schematic of the overall data flow in the CFT L1 and L2 Triggers. The data starts in the CFT FE. One path from there is over 80 serial links to the muon L1. The other path is over another 80 serial links to eight CFT Receiver/ Concentrator Crates. From each crate track counts flow to the CFT L1 crate over one serial link. The track lists flow on another serial link per crate to the L2 preprocessors. A passive splitter at the end of this link fans out the same data to one or more preprocessors.

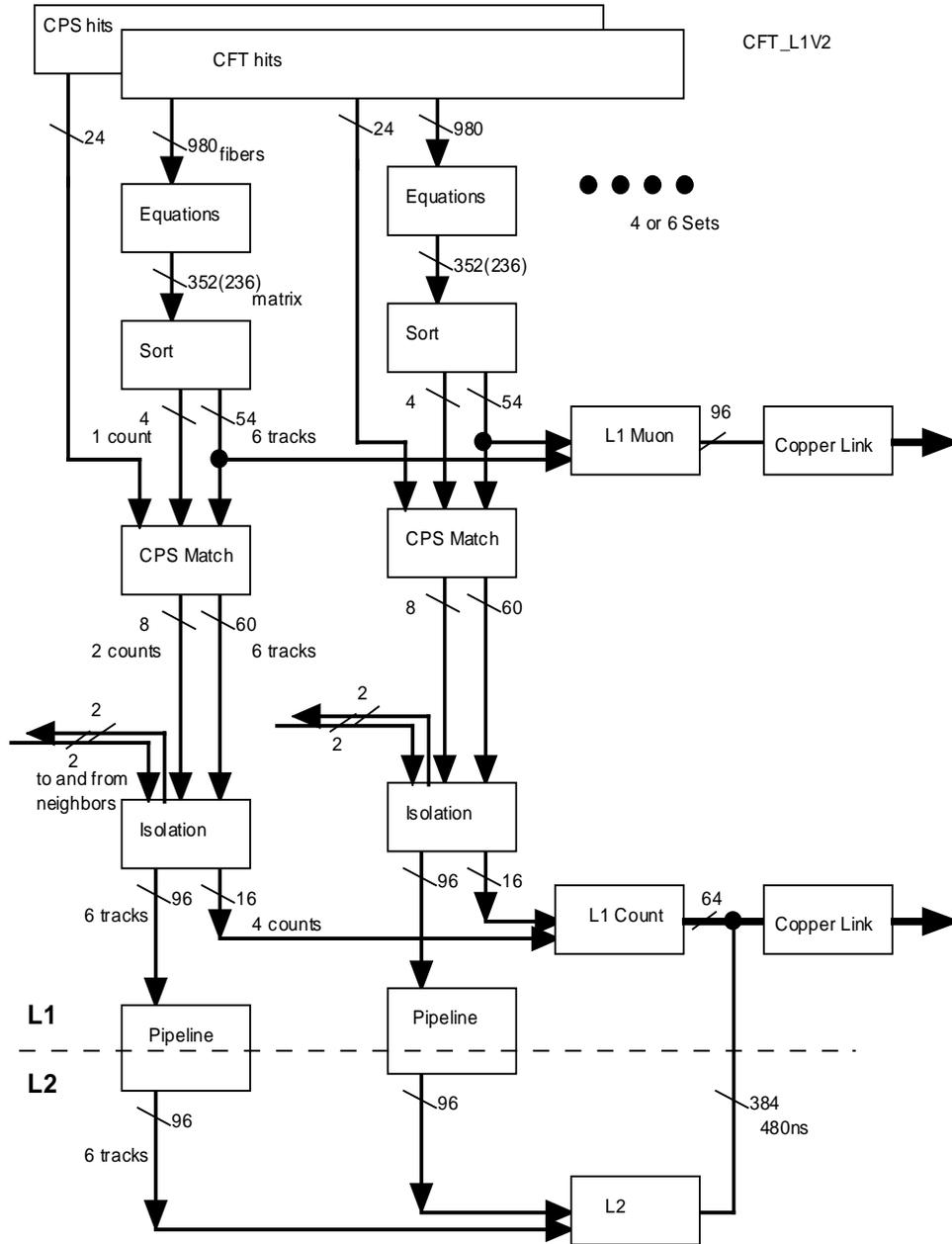


Figure 2. Schematic of the data flow in the FE. The raw hit information enters at the top. The track list for Muon L1 is sent over a copper serial link. The track count values for CFT L1 are sent over a second copper serial link. This second link is also used at L2 time to transfer track lists to the preprocessors.

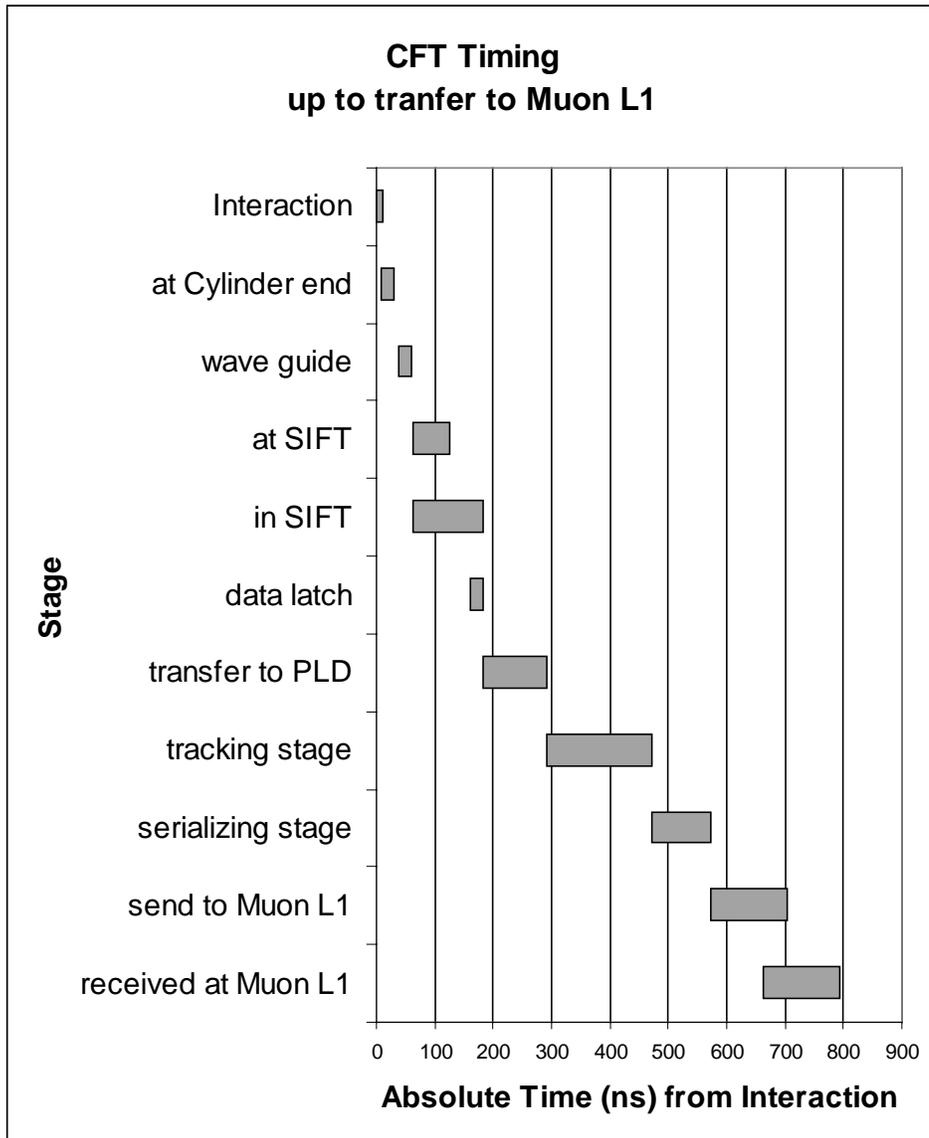


Figure 9. Timing diagram of the timing in the L1 trigger through the reception of track information at the Muon L1 trigger.

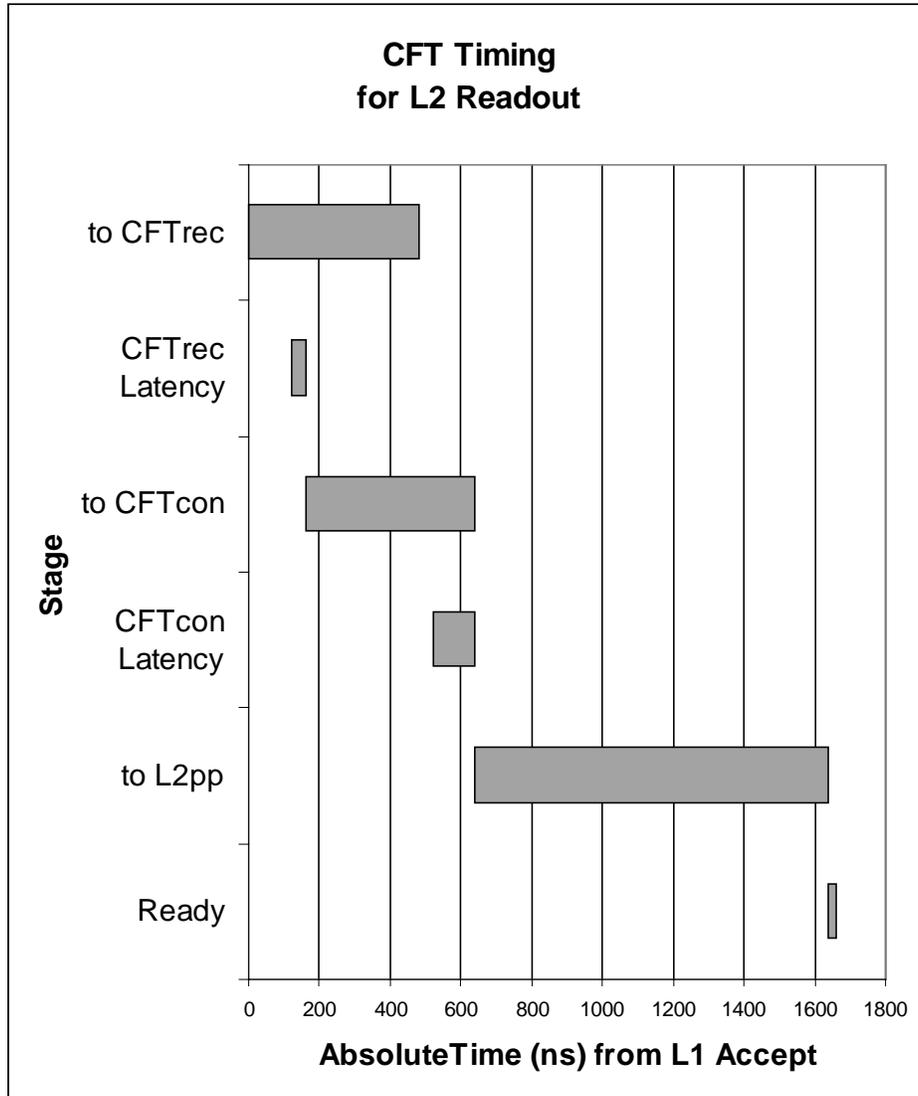


Figure 6. Timing diagram showing the absolute time starting with a L1 accept through the reception of all the tracking information at the L2 preprocessors. The 'to L2pp' time is for 50 tracks.

<sup>1</sup> Note on CPS

<sup>2</sup> The 'Official' Detector parameter files are on the Web at: [http://d0server1.fnal.gov/www/Upg\\_CFT/base\\_line.html](http://d0server1.fnal.gov/www/Upg_CFT/base_line.html)

<sup>3</sup> D0 Note 2139, Electronics Design Specifications for the D0 Upgrade Scintillating Fiber Detector with a Level 1.0 Trigger, Alan Baumbaugh, Fred Borcharding, Marvin Johnson, Jesse Costa, Lourival Moreira, Sudhindra Mani, Steven Glenn and David Pellett, 19-July-1994

---

<sup>4</sup> D0 Node 2359, Level 1 Trigger Design for the D0 Upgrade Central Fiber Tracker, Fred Borcharding, 21-November-1994

<sup>5</sup> D0 Note 3058, D Zero Central Hardware Trigger Preliminary Implementation Studies of the "Base Line Design", R. Angstadt and Fred Borcharding, 15-August-1996.

<sup>6</sup> D0 Note 2504, A study of the Effects of Fiber Placement Errors on the Level 1 CFT Trigger, Fred Borcharding, 17-March-1995

<sup>7</sup> Addendum to: D0 Note 2504, A study of the Effects of Fiber Placement Errors on the Level 1 CFT Trigger, Fred Borcharding, 12-April-1995