Mount resistor this way to route to the left. Blowup sketch of four-the module.
All parts on this page, if installed, are installed in both left-handed and right-handed boards.
Phase 3a: 53 MHz clock to half of CPLDs
Phase 1b: 53 MHz clock to Clock Generator
Phase 2b: 53 MHz clock to LVDS drivers (righthand)
Phase 2a: 53 MHz clock to LVDS drivers (lefthand)

Clock generator. Creates 53 MHz from XING clock.

One copy of VSVX_CLK goes to each VSVX CPLD (next to each MCM);

CPLD_53MHZC Layout Note: Put

CPLD_53MHZ_B
All parts on this page, if installed, are installed in both left-handed and right-handed boards.
Heater 1 is driven by a DAC channel, local to board.

Cryostat heater resistor driver

Decoupling for op495 amp

LPBACKB_OUT

LPBACKB_IN

LPBACKA_OUT

XL1

XL2

XL3

XL4

J116

HEATER1_B

HEATER2_B

SENSOR_B

SENSOR_A

VBIAS 4

VBIAS 6

VBIAS 8

Decoupling for diff amp

0.001 uF

Decoupling for diff amp

0.001 uF

Decoupling for diff amp

0.001 uF

20 nA per volt

10 uA constant current source

100K

1K

51.0K, 0.1%

100K

CAGE Code DWG NO Rev

Drawn:  J.T. Anderson

Q input, Flex Cable #3, MCM #3

Batavia, IL 60510

Fermi National Accelerator Laboratory

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Heater 1 is driven by a DAC channel, local to board.

Gain = \( \frac{49.4\,K}{R} + 1 \) = 19.297 (2.7K)

Current sensor