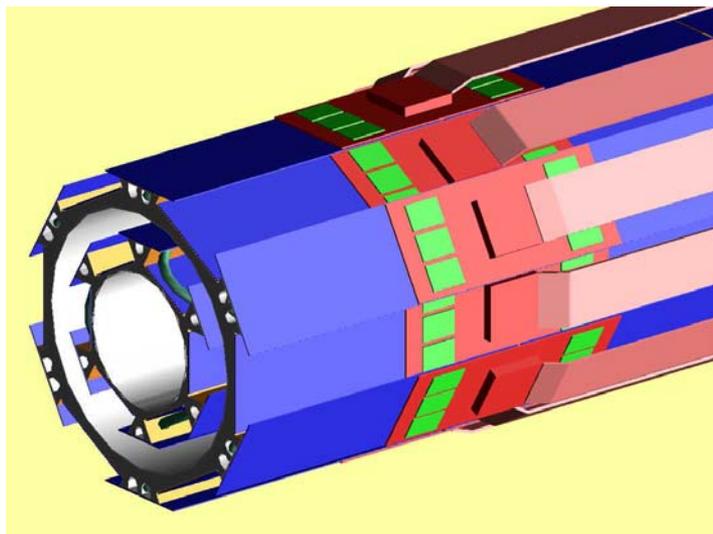


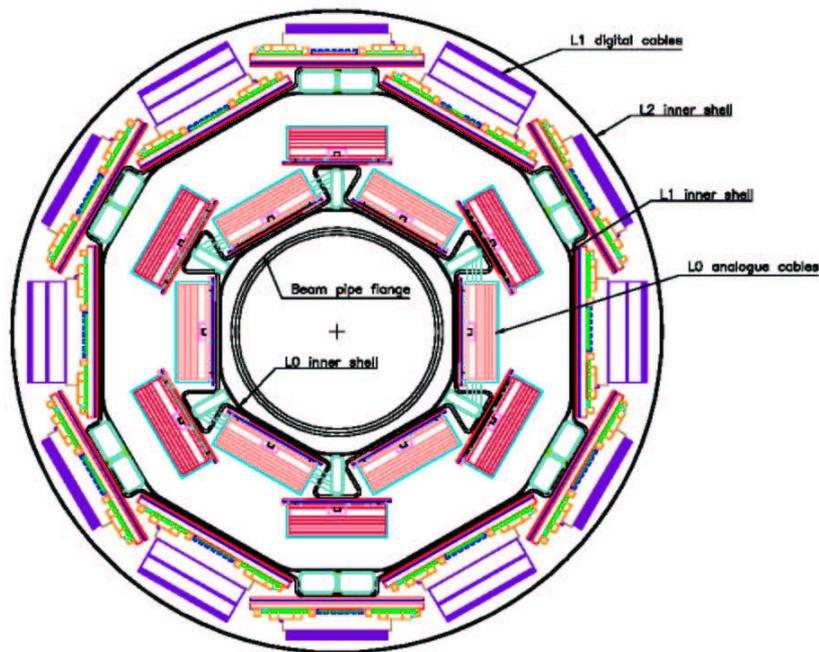


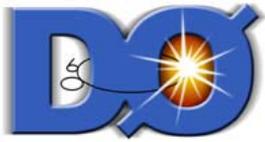
Layer 0 in D0 Silicon Tracker for run2b



Kazu Hanagaki / Fermilab
for D0 run2b Silicon Tracker group

- Motivation & concept
- Analog flex cable
- Prototypes
- Noise/Shielding studies
- Summary and prospects





Motivation

- Higgs search, new phenomena search, top physics, b physics... ← all needs b tagging.
- B tagging by means of the longer life time of B meson/baryon
→ better impact parameter resolution.
→ measurement at position close to the decay point.

$$\sigma \sim \sigma_{\text{meas}} \left(1 + \frac{R_{\text{in}}}{R_{\text{out}}}\right)$$

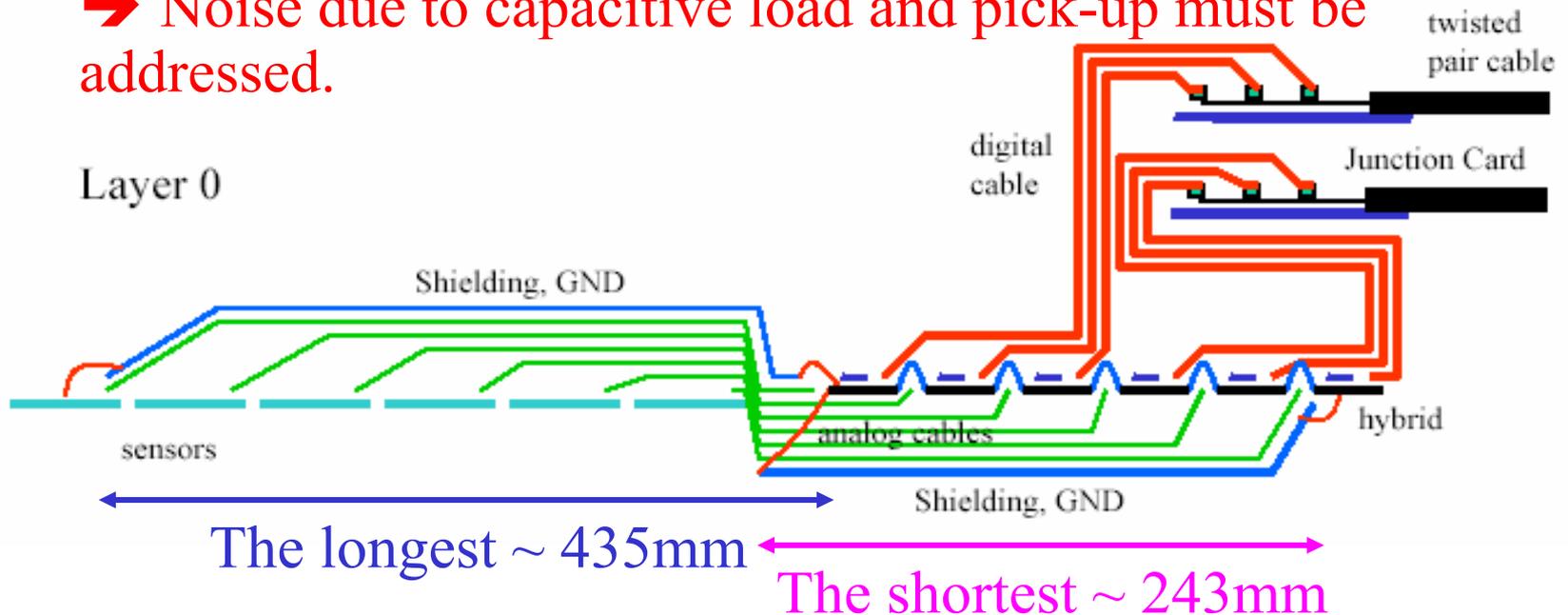
(0.11 for run2b, 0.27 for run2a)

- Design goal: $S/N > 10$ after 15fb^{-1} for the Layer 0 (L0).
- Simulation for $WH(\rightarrow \bar{b}b)$ events:
b jet tagging efficiency $\cong 69\%$ for run2b (50% for run2a)



Concept

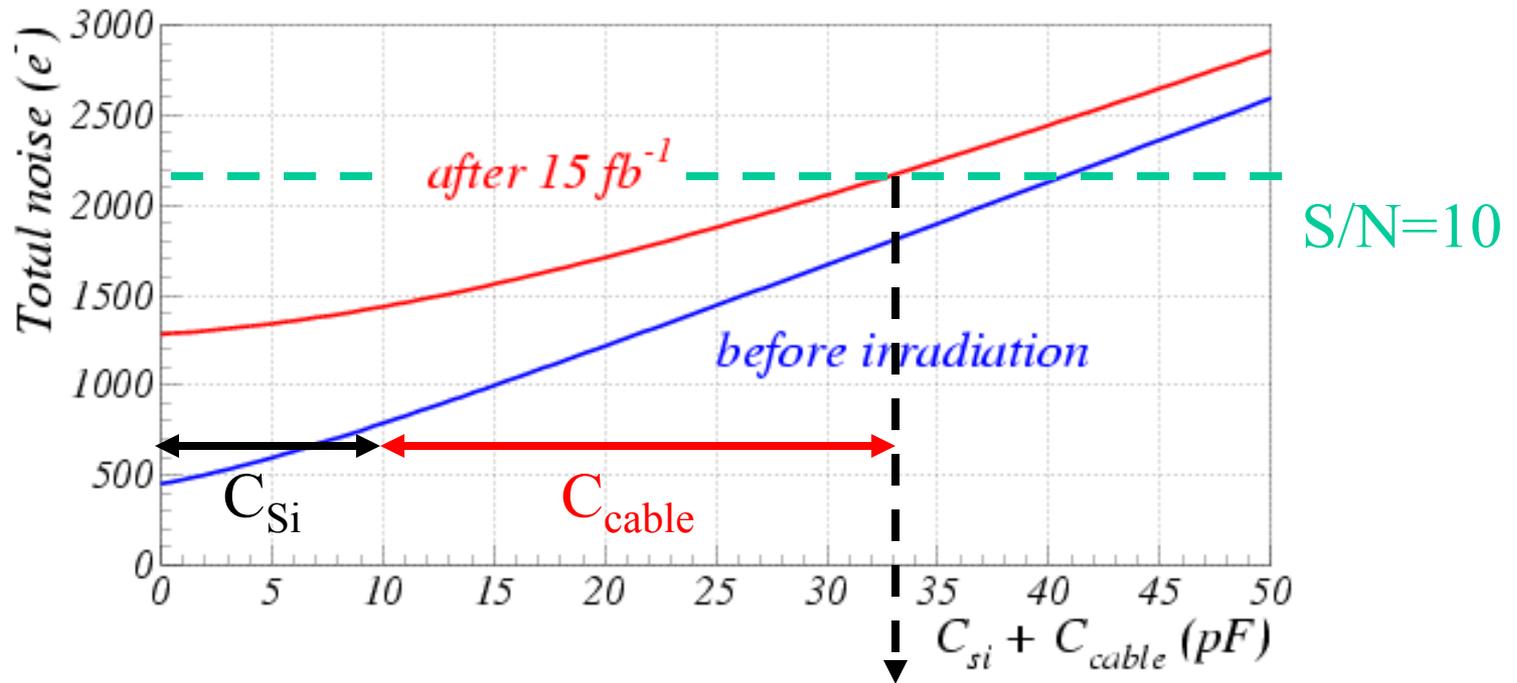
- SVX4 chip cannot sit on the sensors because of the cooling and space issues.
 - Signal must be read out from the sensor to the chip.
 - Also bias voltage and its return must be provided.
 - Low mass analog flex cable.
 - Noise due to capacitive load and pick-up must be addressed.





Requirement to Analog Cable

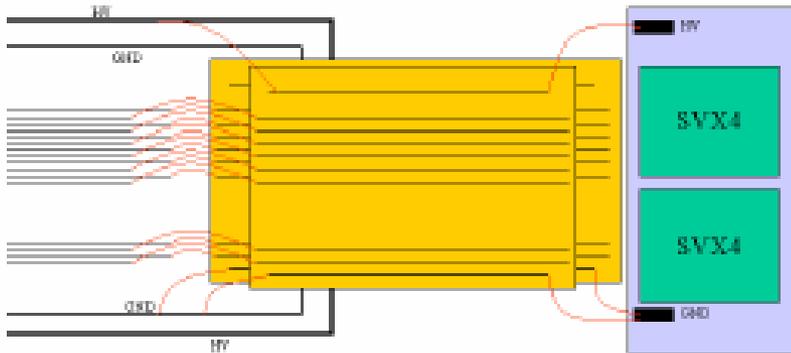
Total noise estimates VS total capacitance ($C_{si} + C_{cable}$)



$S/N=10$ after $15fb^{-1} \rightarrow C_{cable} < 23pF$ for 43.5cm long cable
 $\rightarrow C_{cable} < 0.53pF/cm$

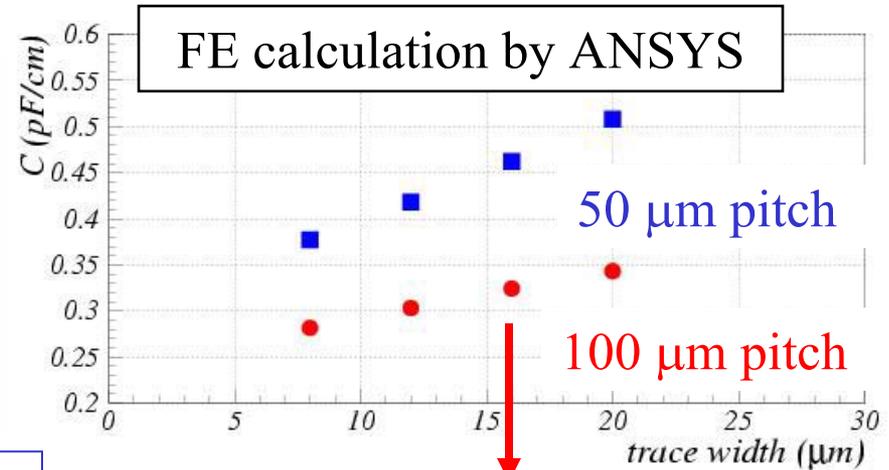


Analog Cable Design



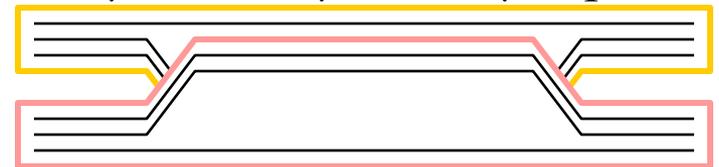
- 91 μm trace pitch.
- 16 μm trace width.
- No fan-in/out region.
- Two cables laminated at the edges with 45 μm offset.
- 50 μm thick polyimide (Kapton type) substrate.

→ Use technically simpler solution which maintains low capacitance.



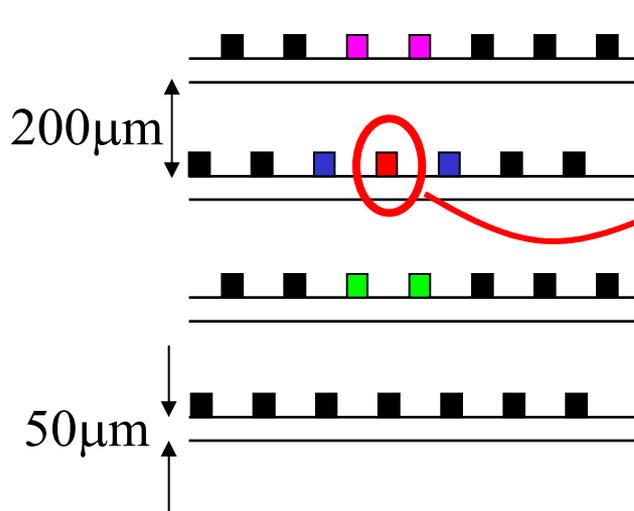
16 μm wide trace with $\sim 100 \mu\text{m}$ pitch satisfies the requirement of $< 0.53 \text{ pF/cm}$

- Alternative for 50 μm pitch readout
50 μm + 100 μm + 50 μm pitch





Analog Cable Design (cont'd)



100µm pitch
8 x 16µm traces

$$C = 0.328 \text{ pF/cm}$$

Contribution from:

Two neighbors = 0.208 pF/cm

Two top neighbors = 0.014 pF/cm

Two bottom neighbors = 0.017 pF/cm

- 200 µm is enough to avoid significant contribution from other cables.
- Low ϵ_r material for spacer.
← polypropylene mesh.

ϵ_r (spacer)	C (pF/cm)
1	0.328
2	0.449
3	0.566

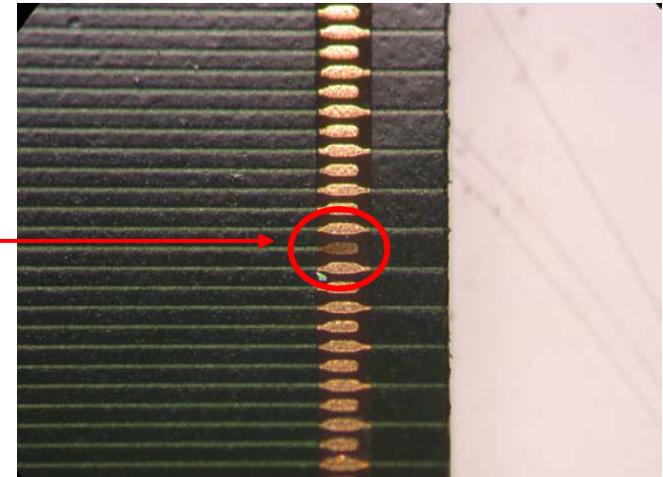


Prototype Cable by Dyconex

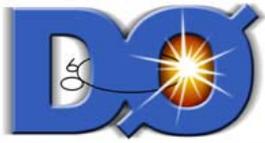
- visual inspection on cables:
 - look for not gold-plated (copper) pads as evidence for an open trace

# open traces	0	1	2	>2
#cables	22	13	4	0

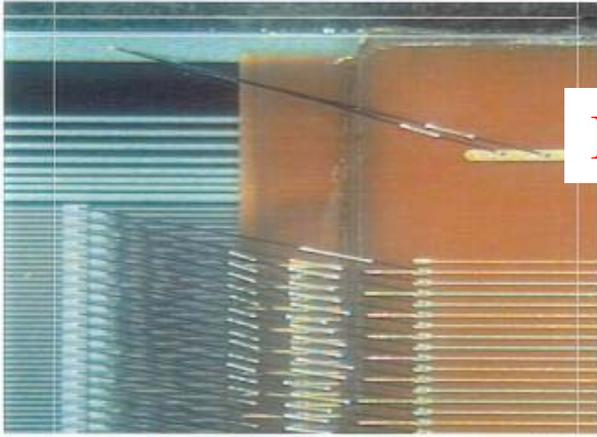
- 129 traces → one open is allowed.
- check trace width on cables:
9-12 μm depending on cable.



Capacitance (one to neighbors) $\sim 0.35\text{pF/cm}$.

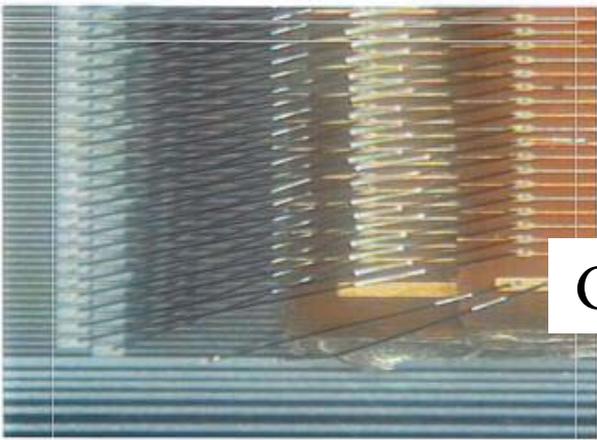


L0 Prototype for noise studies

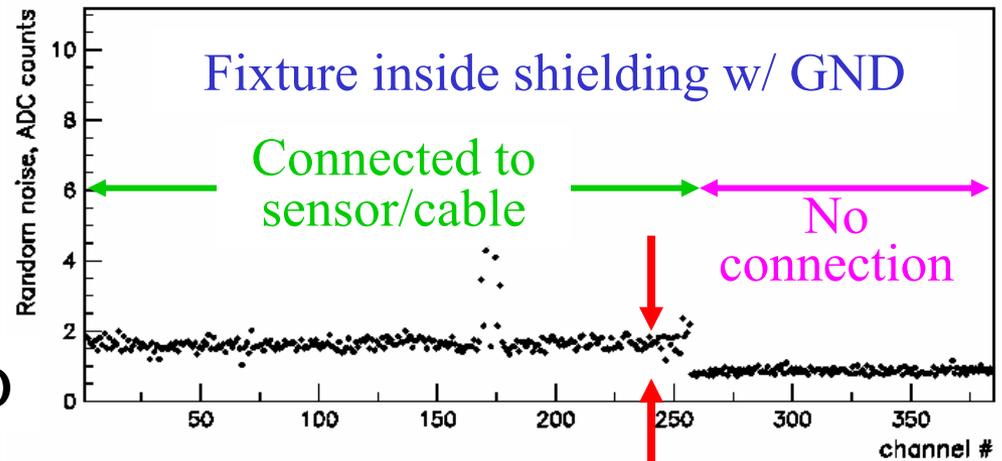


HV

- Dyconex analog cable + ELMA prototype sensor + SVX2 chip (for run2a)
- Noise increase $\sim 1000 e$
← consistent with SVX2 noise performance.



GND

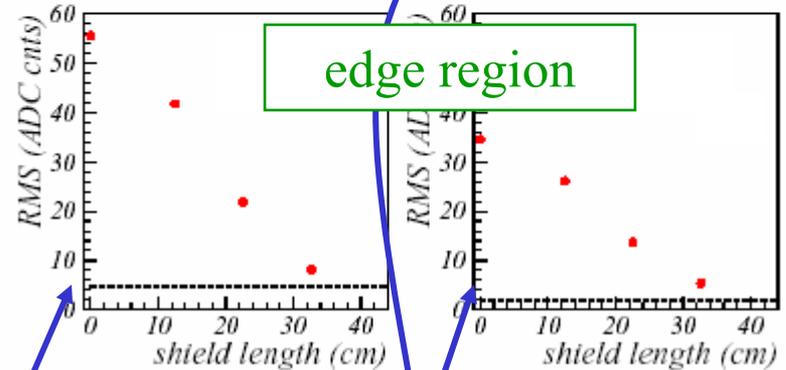
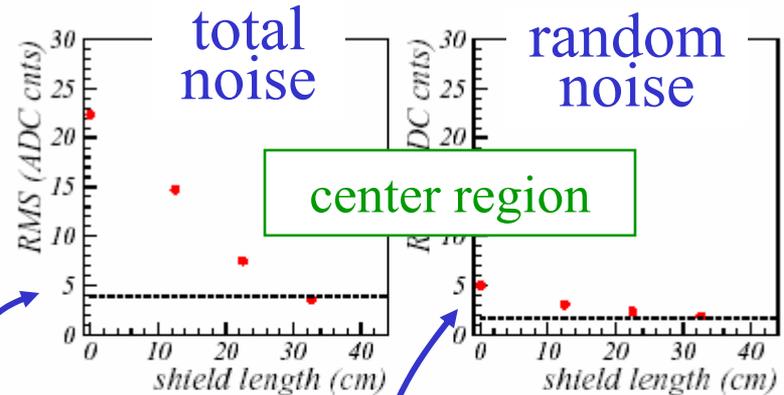
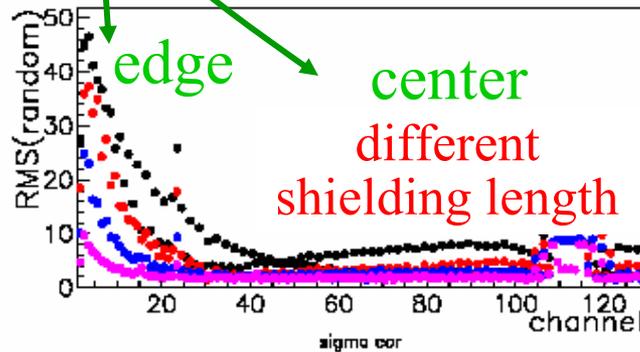
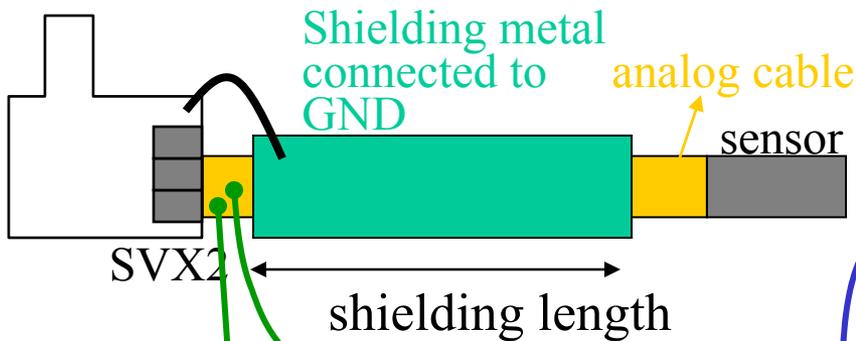


Noise increase due to capacitive load



Shielding

- RF pick-up by the analog cable.
- No external but shielding (= aluminum foil) only around the analog cable.

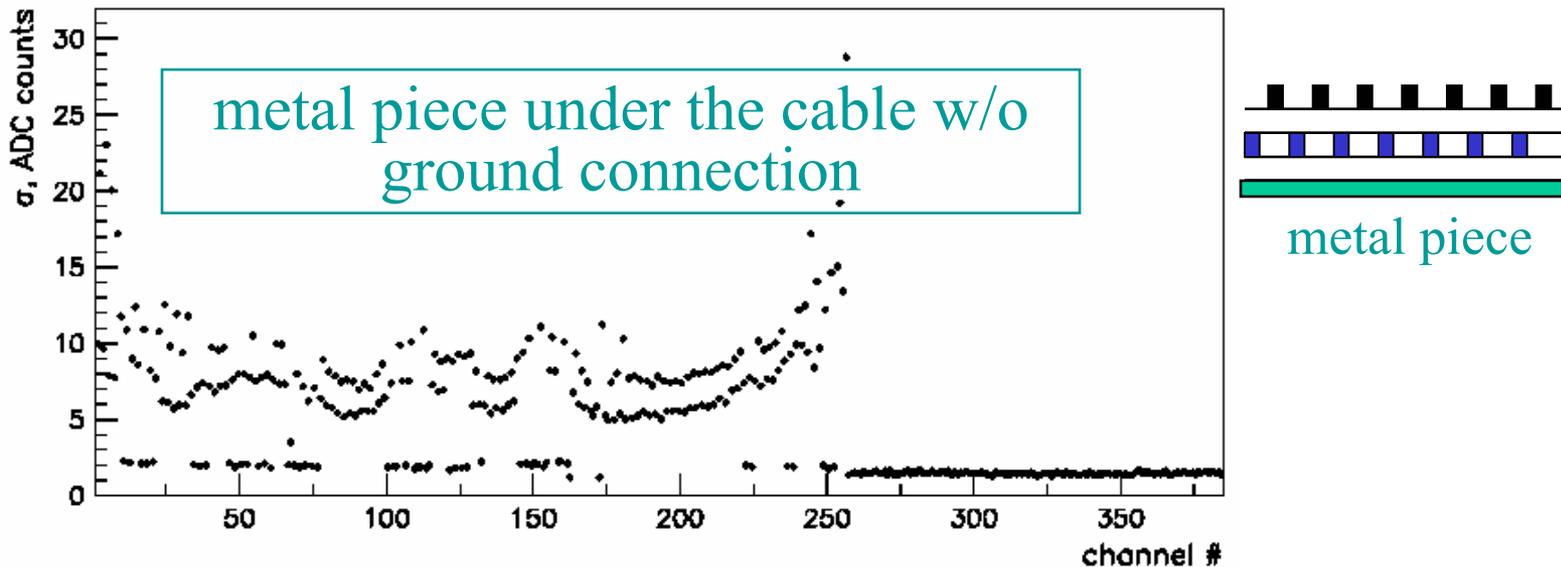


Noise level w/ ext. shielding



Shielding (cont'd)

- Must be careful about capacitive coupling to nearby floating metal.

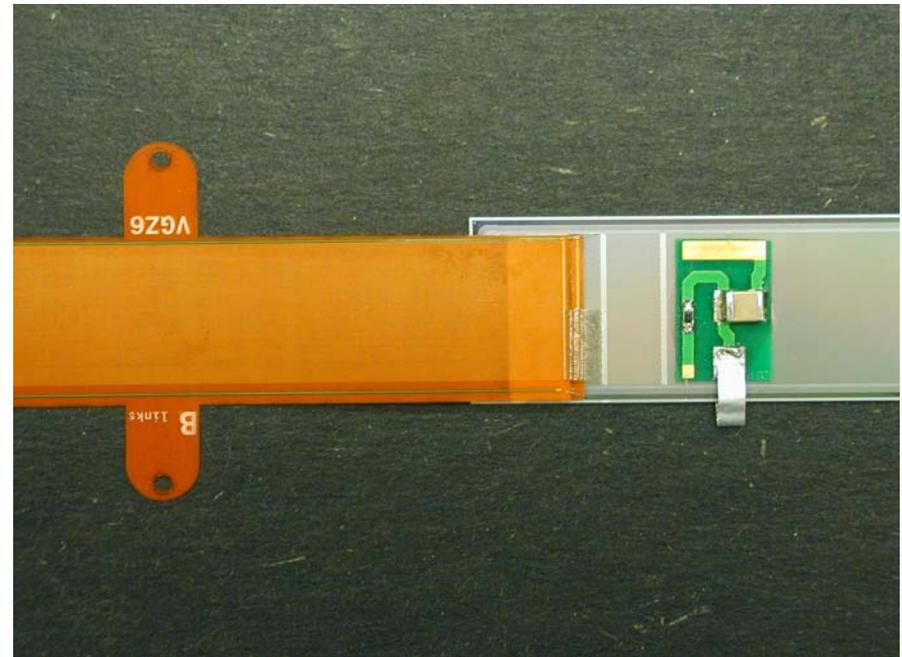
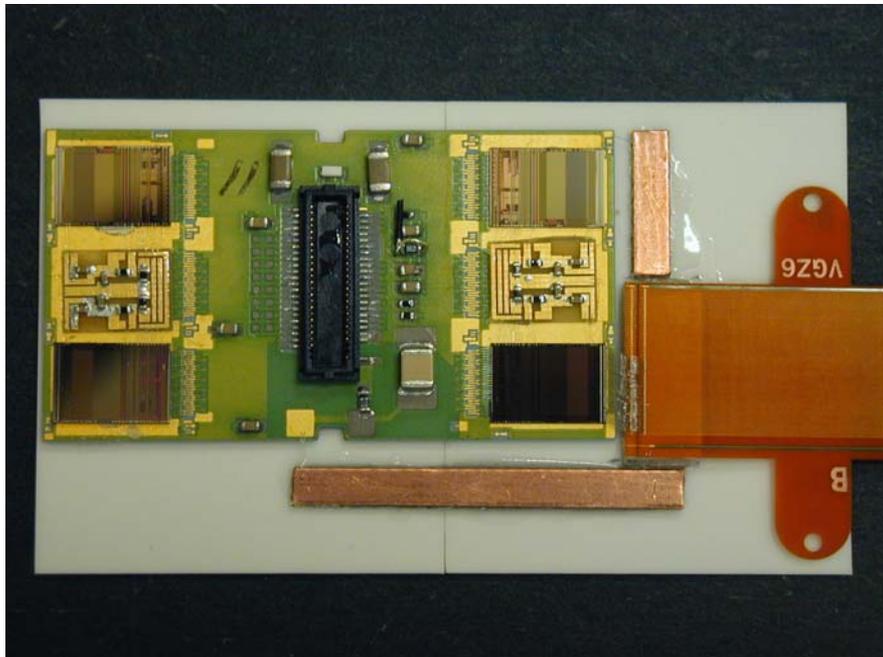


- Clear even-odd effect indicates capacitive coupling to the analog cable. ← Distance between the traces to the metal; top-metal $\sim 100\mu\text{m}$, bottom-metal $\sim 50\mu\text{m}$.



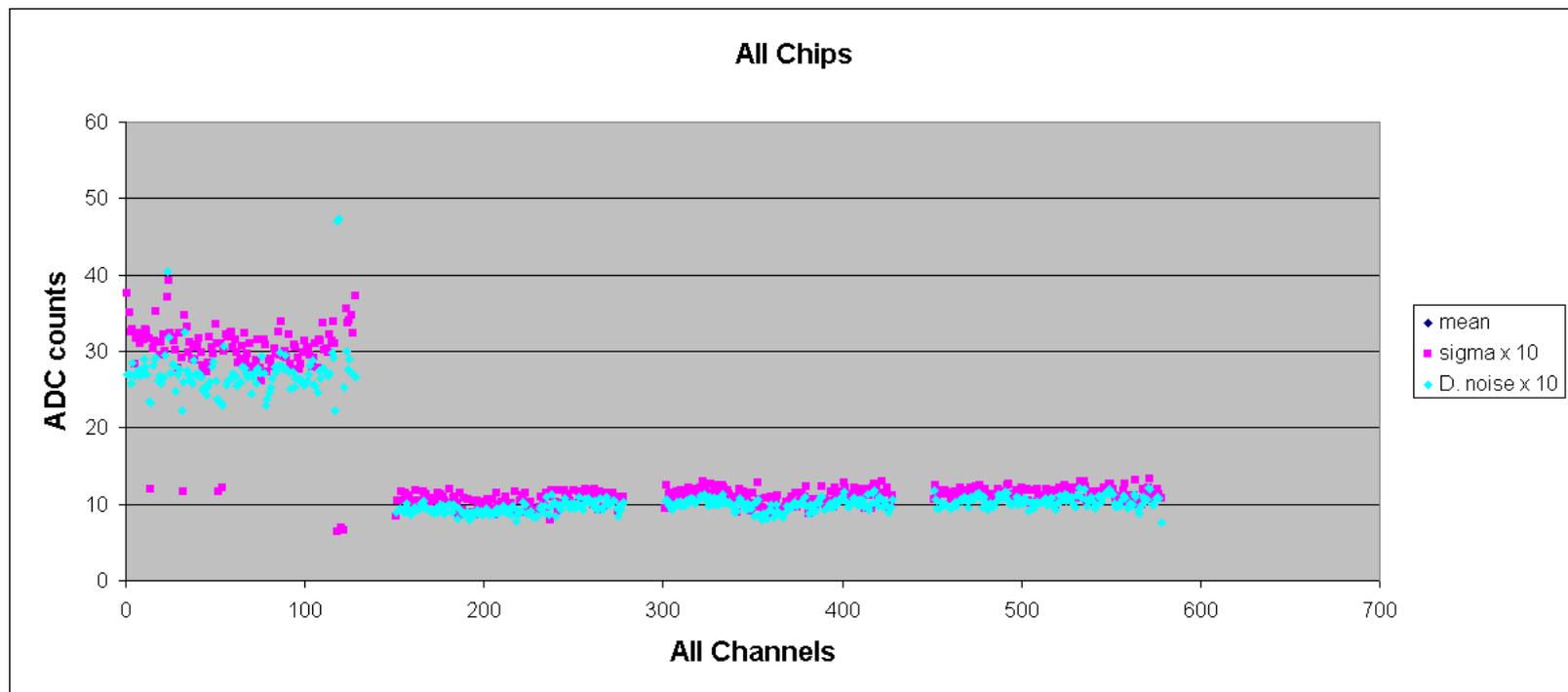
L0 Prototype with SVX4

- First prototype using new SVX4 chip.
 - Large capacitive load
 - Long analog cable ← signal transmission
- L1 prototype hybrid with SVX4.





Prototype w/ SVX4 (cont'd)



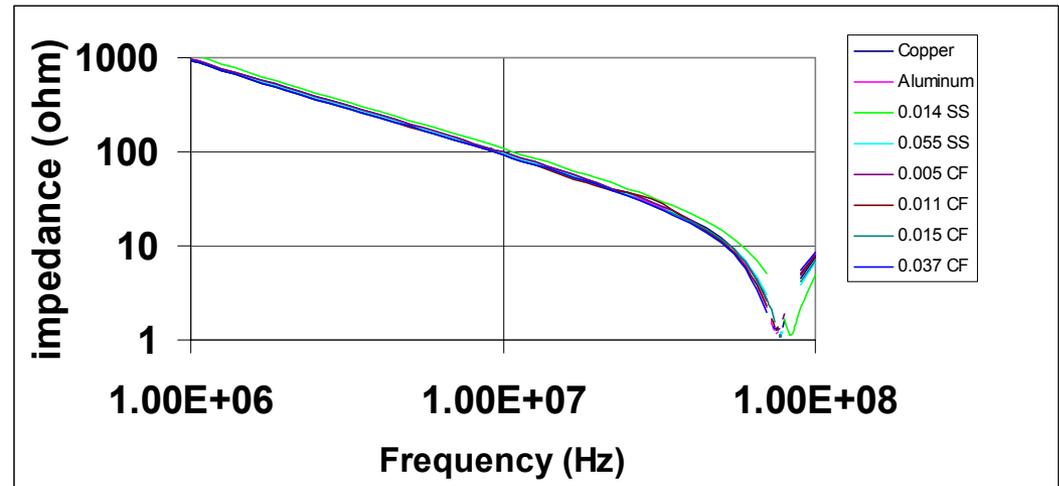
- **Successfully reads out!**
First time for SVX4 through long analog cable.
- (Systematic noise studies not yet done...)



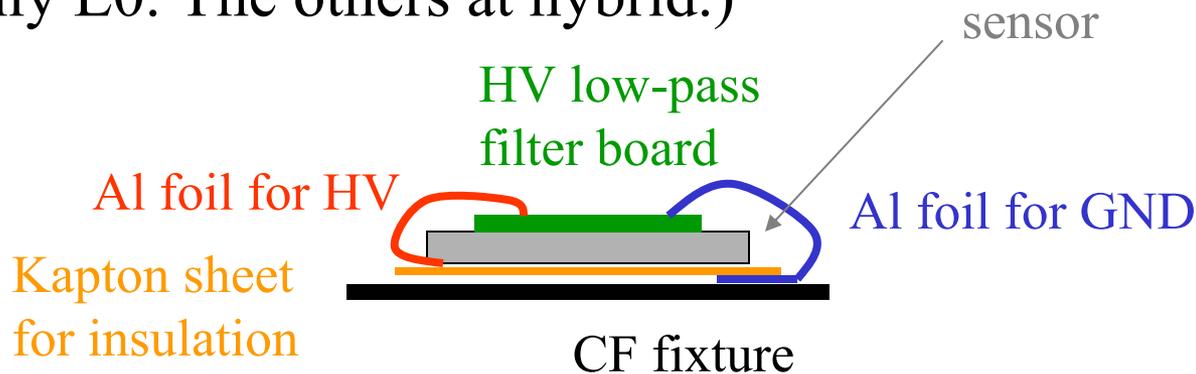
Grounding

- Carbon Fiber (CF) support structure is regarded as a conductor for high frequency.

← talk by B. Quinn



- Sensor ground will be tied together to the CF structure. (Only L0. The others at hybrid.)





Summary & Prospects

- Established baseline design for the analog cable.
- Test results of prototype analog cable are encouraging.
- L0 prototype addresses the feasibility of our baseline design.
- Noise studies are in progress.
- Grounding scheme will be tested by having prototype module.