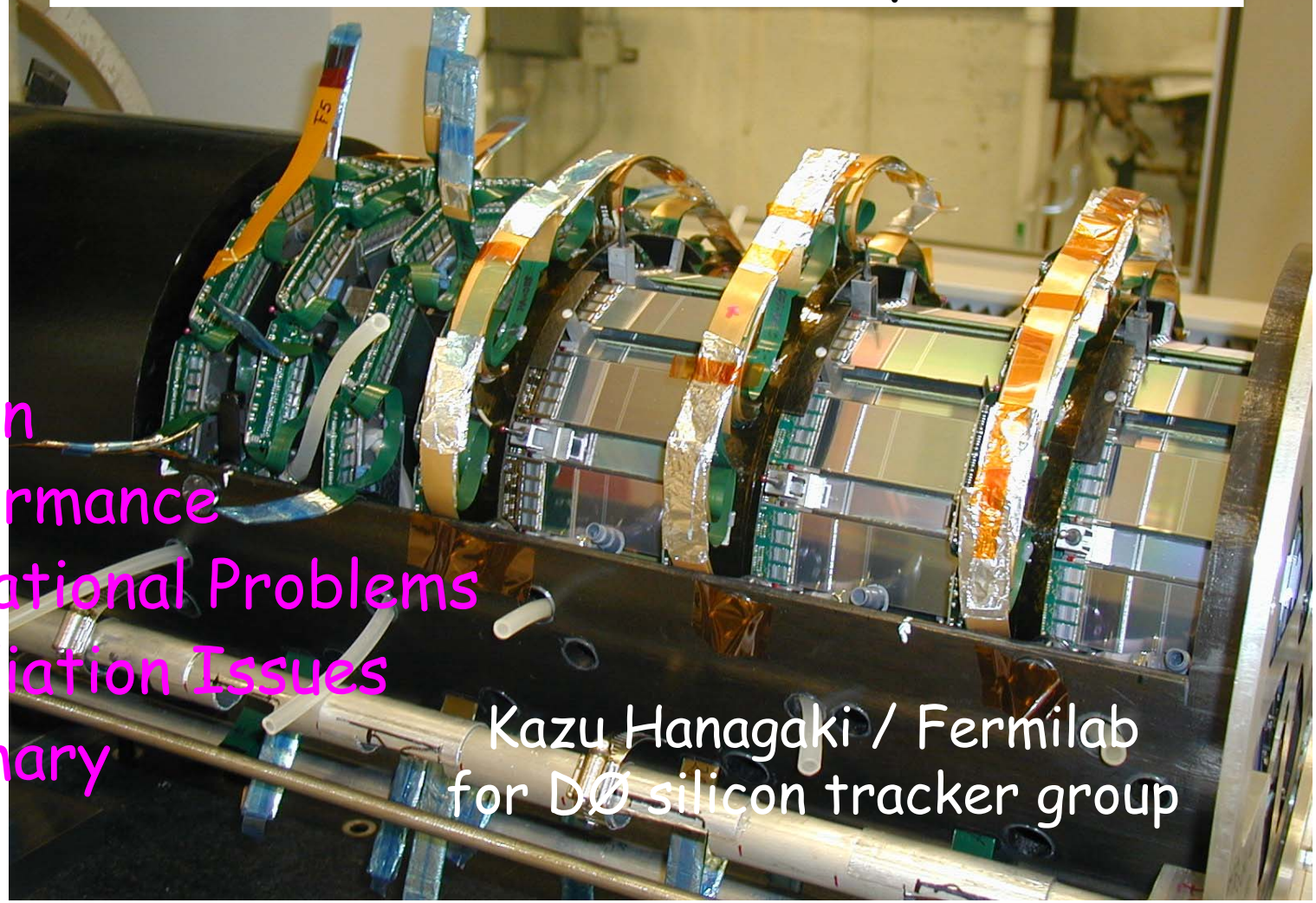
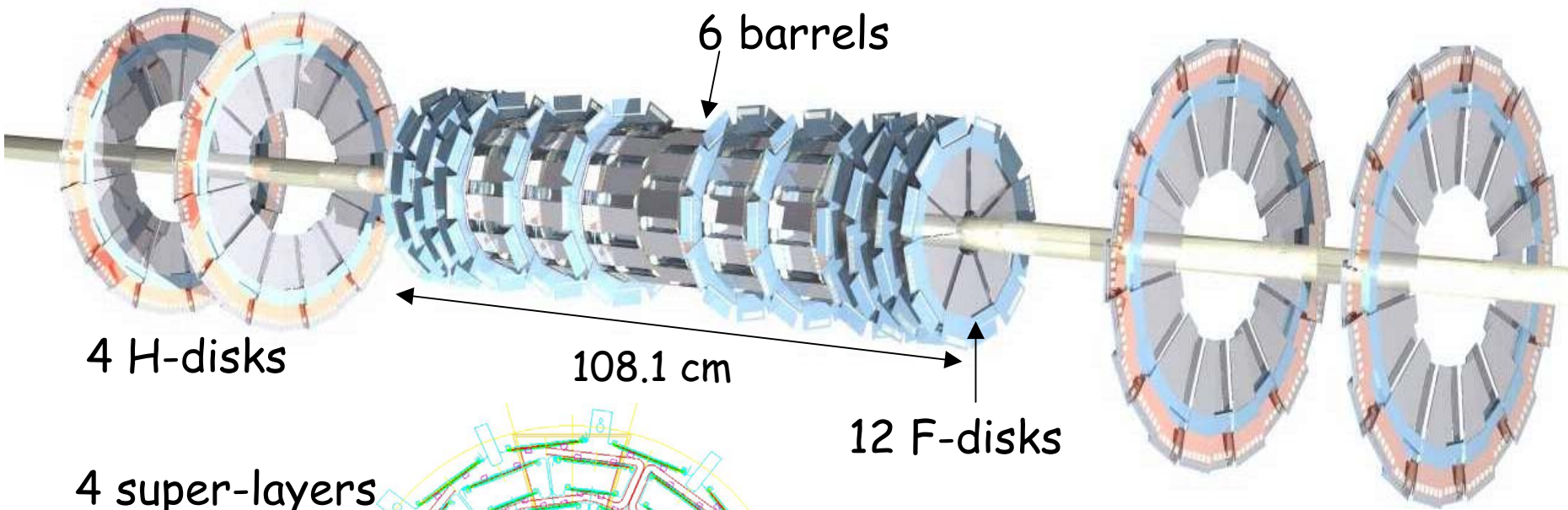
Lessons Learned from the DØ Silicon Micro Strip Tracker



- Design
- Performance
- Operational Problems
- Irradiation Issues
- Summary

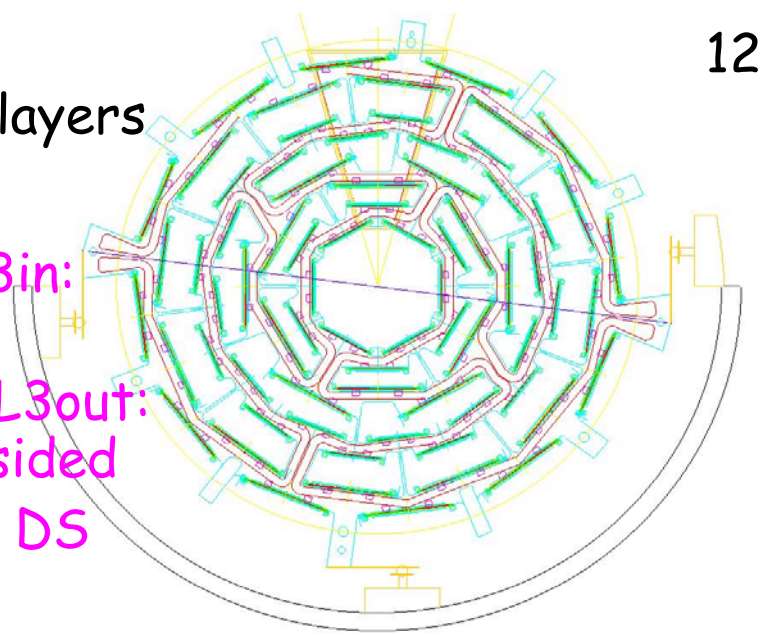
Kazu Hanagaki / Fermilab
for DØ silicon tracker group

Design



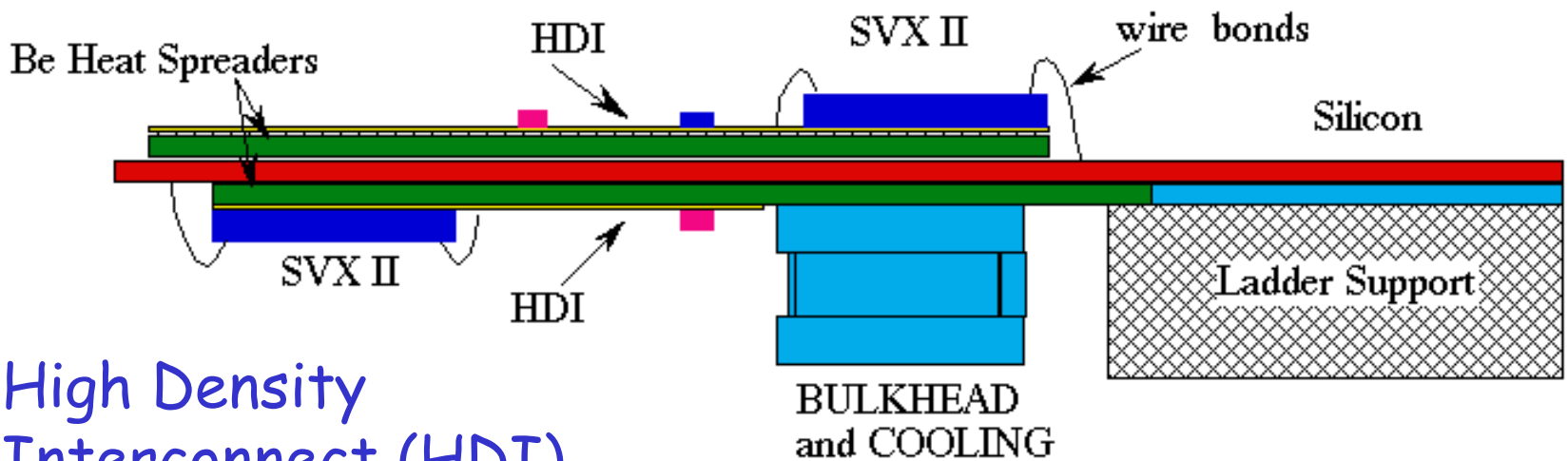
4 super-layers in barrel

- L1in, L3in: DSDM
- L1out, L3out: single sided
- L2, L4: DS



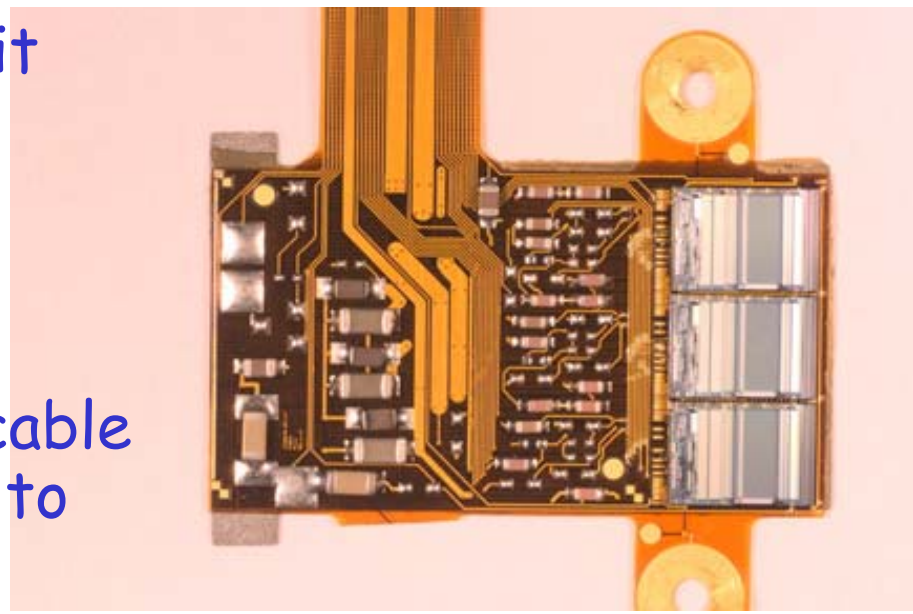
	Barrels	F-Disks	H-Disks
Channels	387072	258048	147456
Modules	432	144	96
Si Area	1.3 m^2	0.4 m^2	1.3 m^2
Inner R	2.7 cm	2.6 cm	9.5 cm
Outer R	9.4 cm	10.5 cm	26 cm

Module

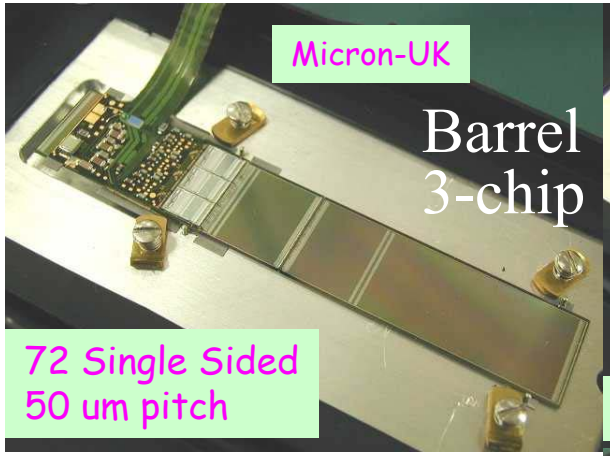


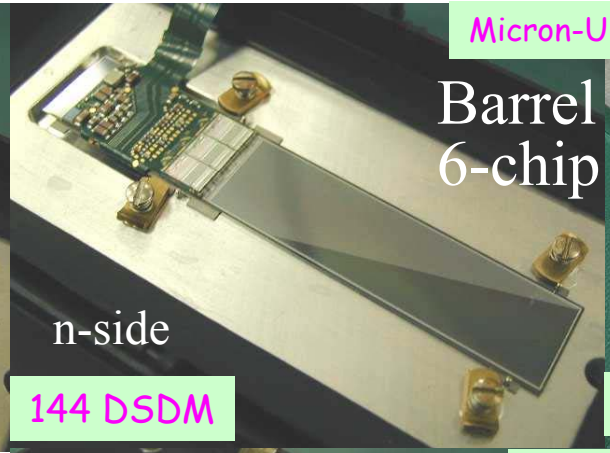
High Density Interconnect (HDI)

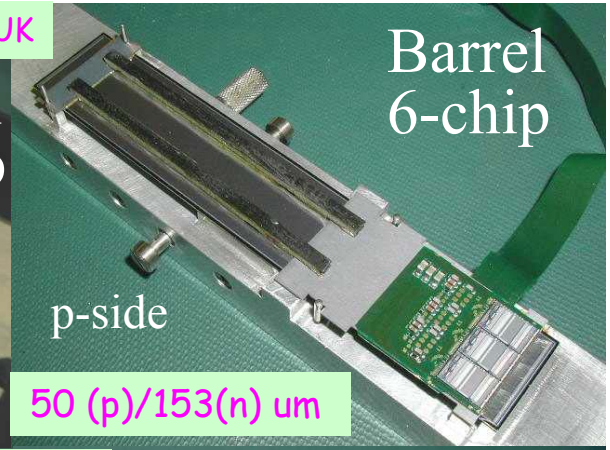
- Kapton based flex circuit with SVX IIe
- Laminated to beryllium substrate, and glued on silicon sensor
- Connected to low mass cable which carries signal out to the interaction region

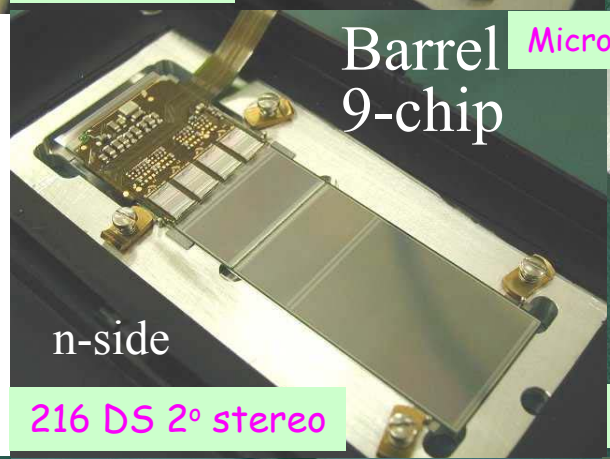


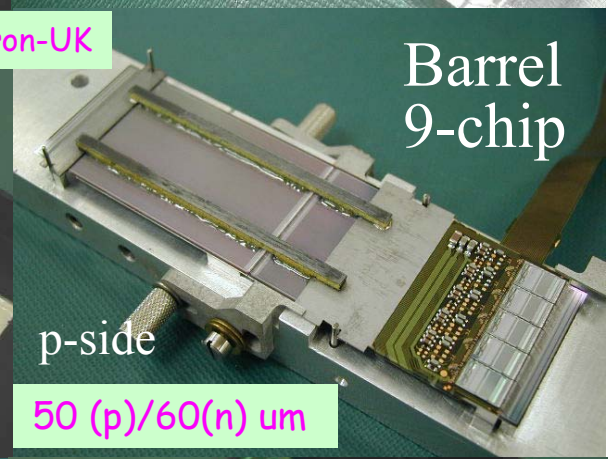
Various types of detectors (all AC coupled)

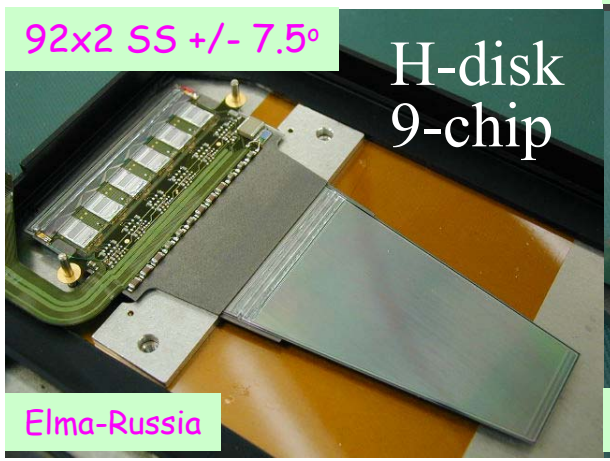


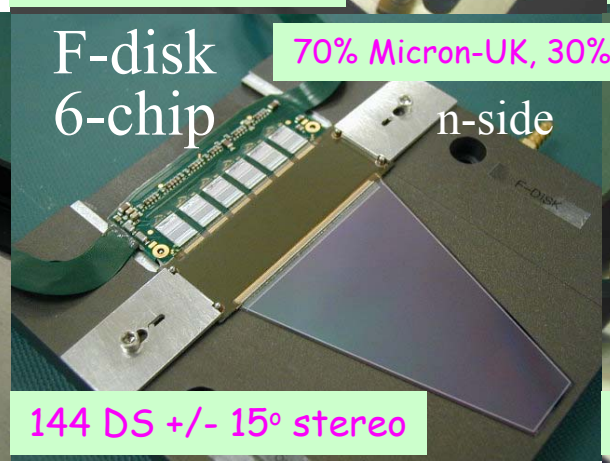


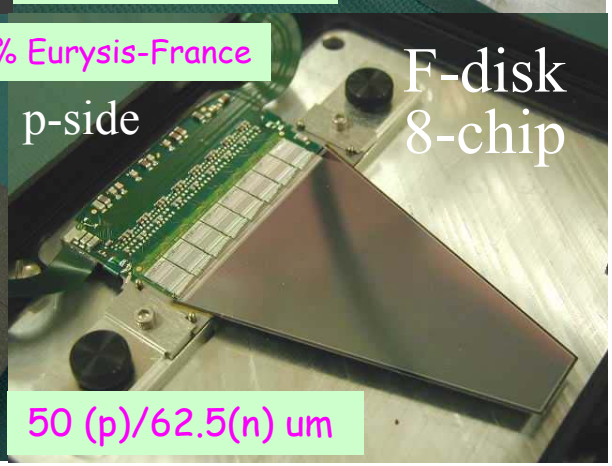




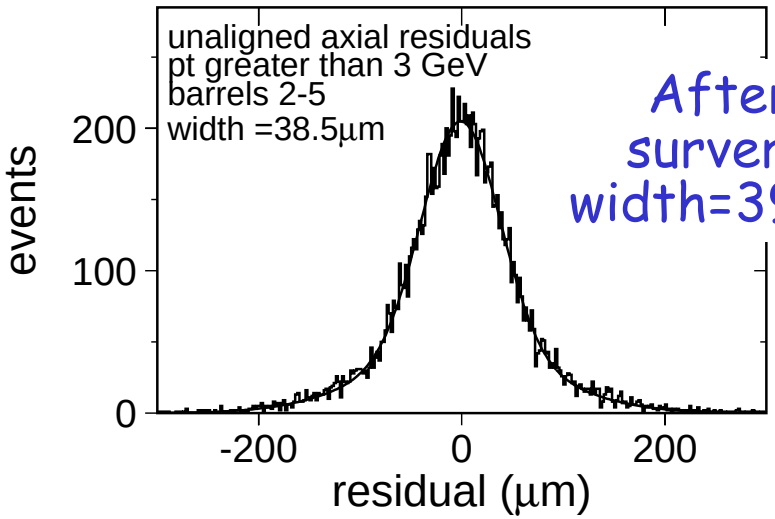




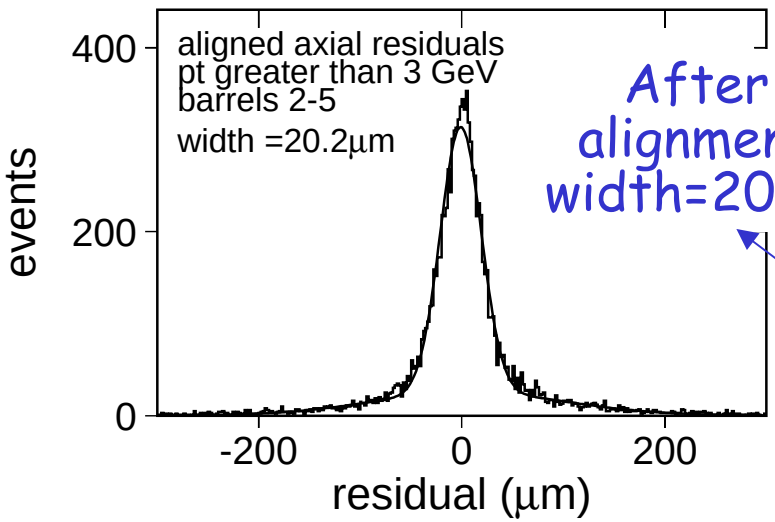




Alignment

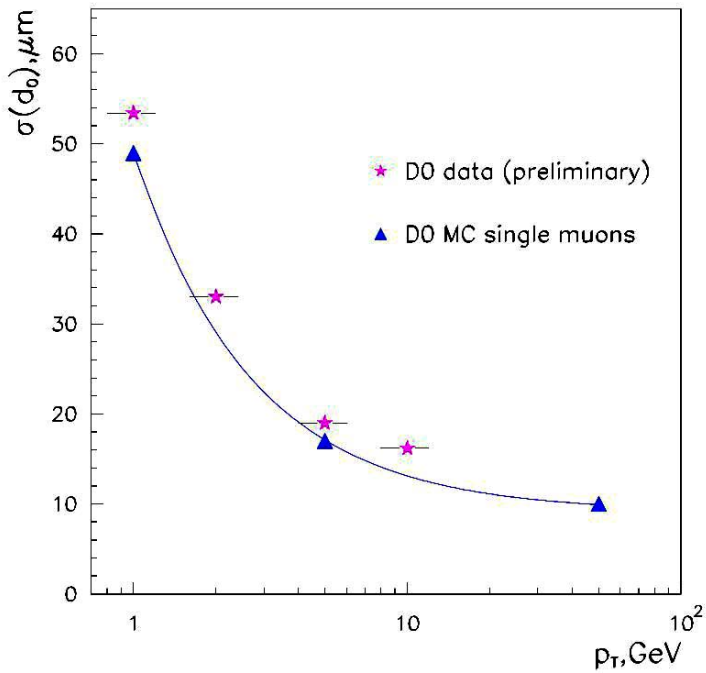


After survery width=39μm



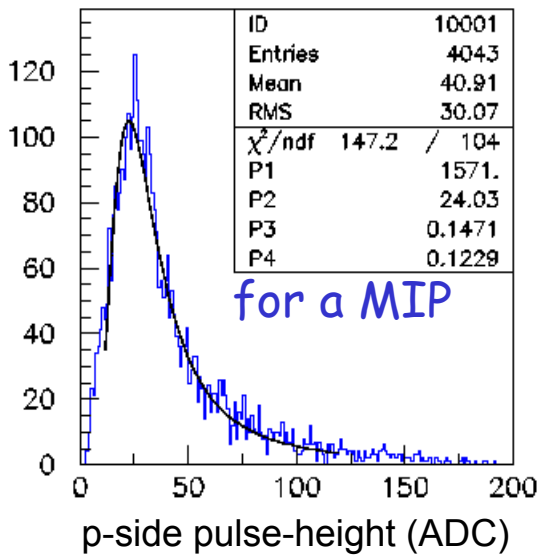
After alignment width=20μm

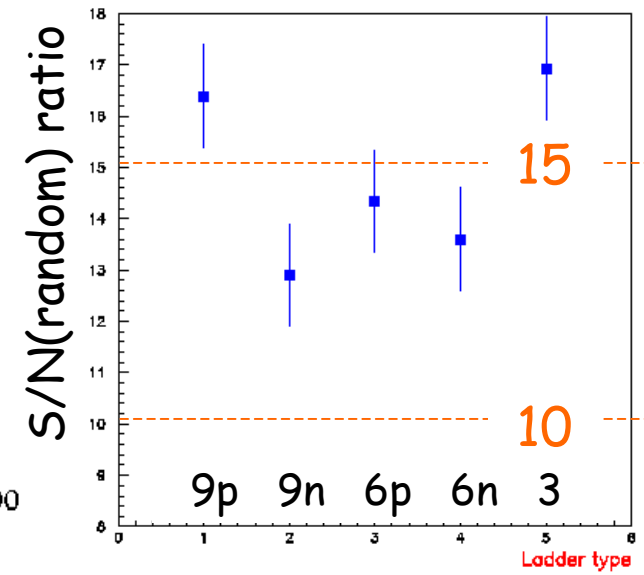
Perfect alignment in MC : 16μm

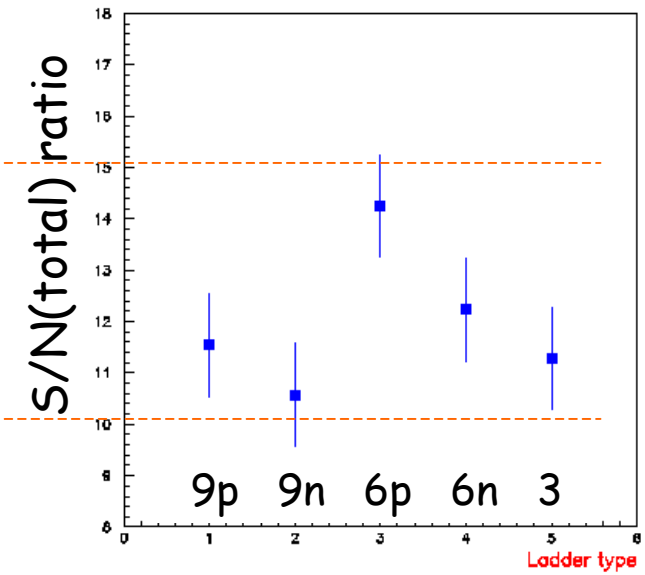


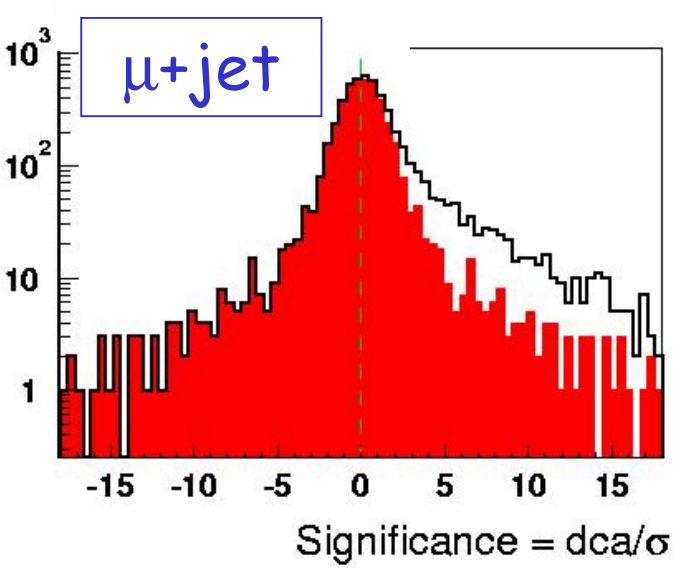
- Reasonably well aligned
  - Only a few μm of mis-alignment

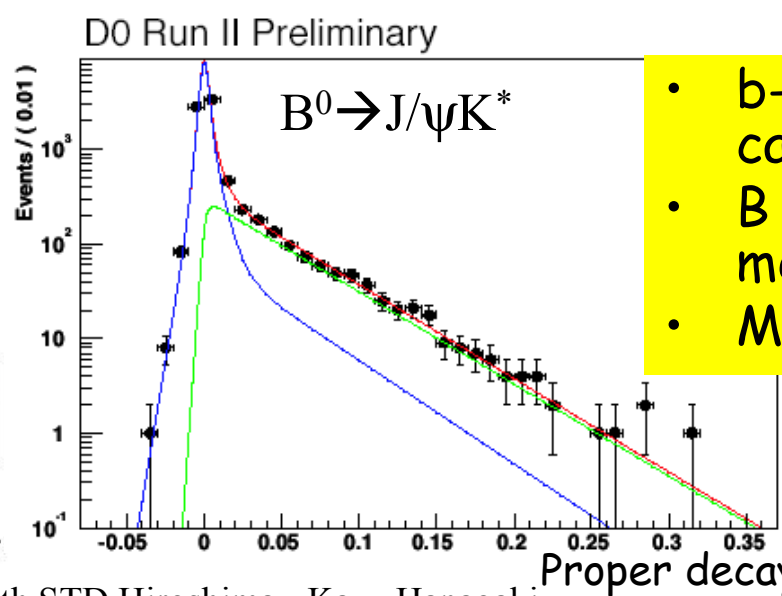
Performance







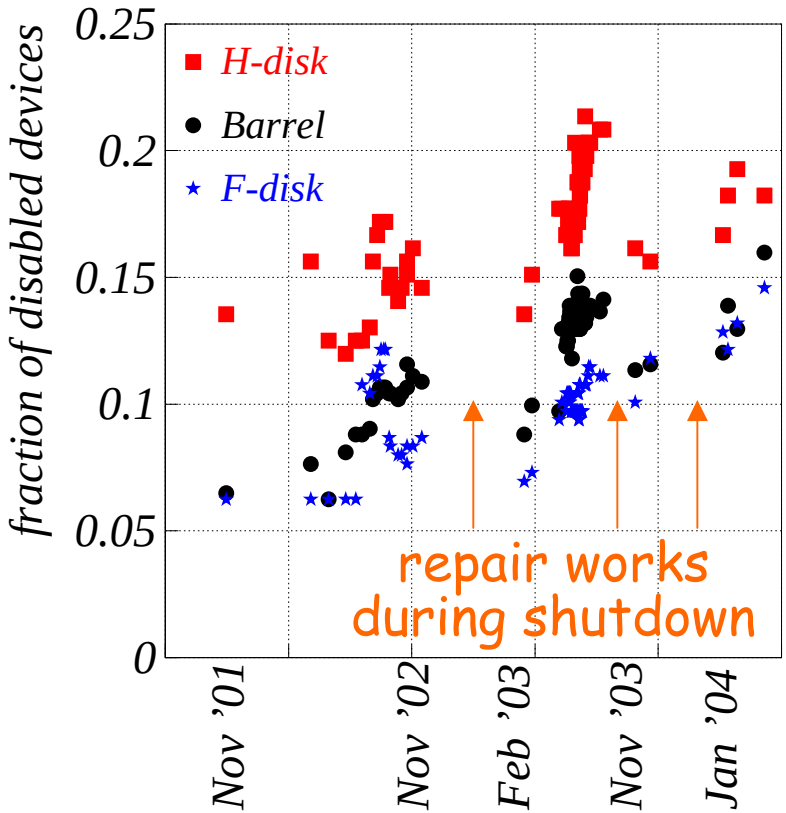


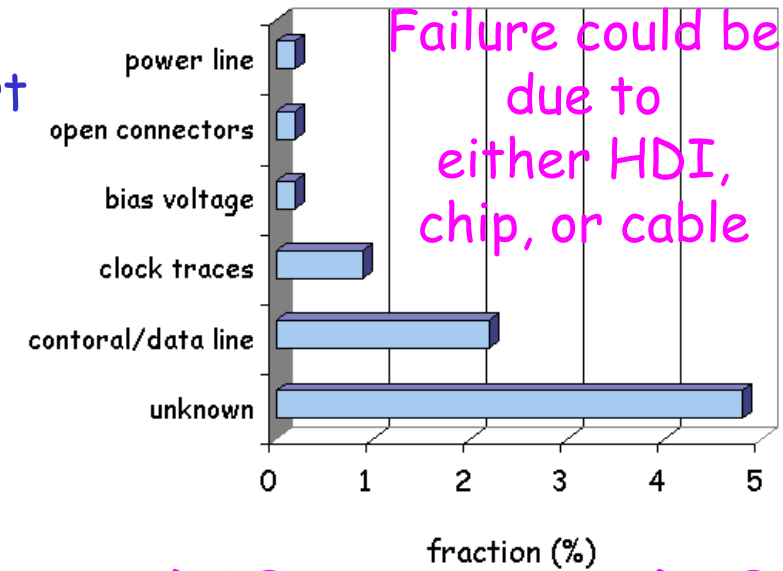


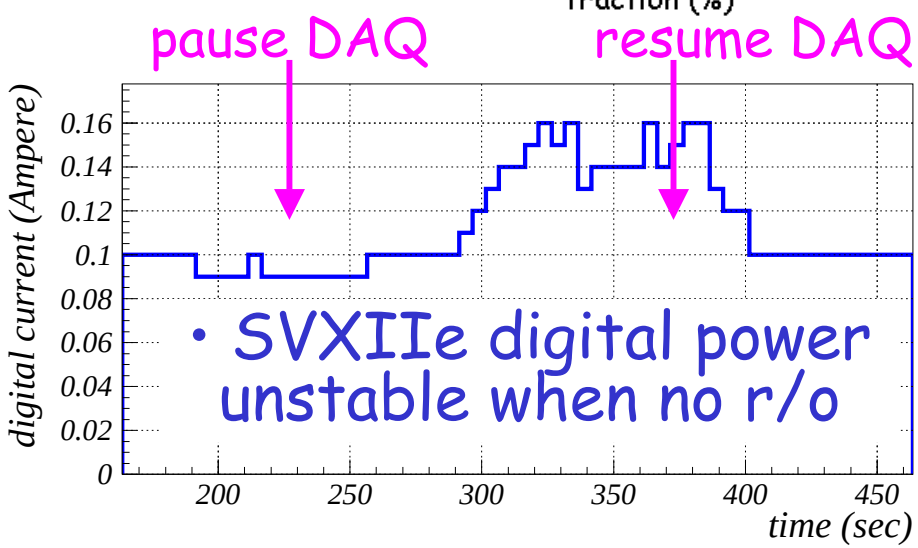
- b-jet tagging capability
- B lifetime measurement
- More…

HDI failure

- 85% of channels are healthy
  - 9% problems in non accessible part
  - 7% unstable

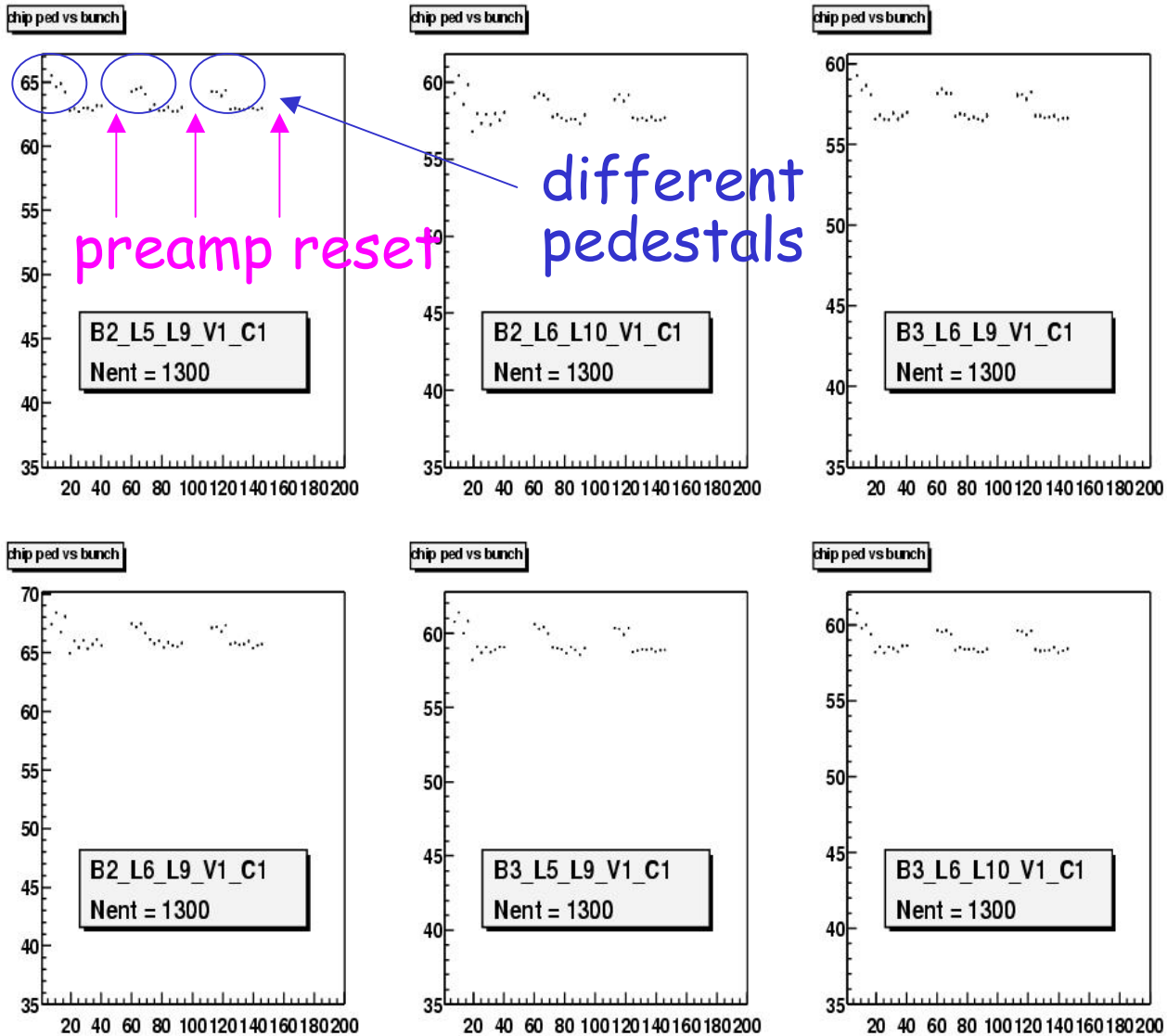




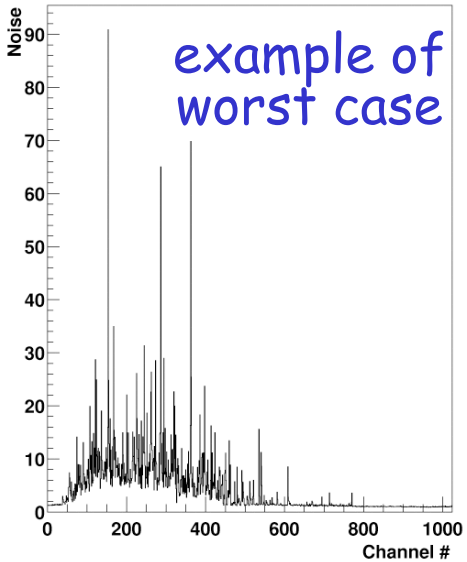


Pedestal Shift

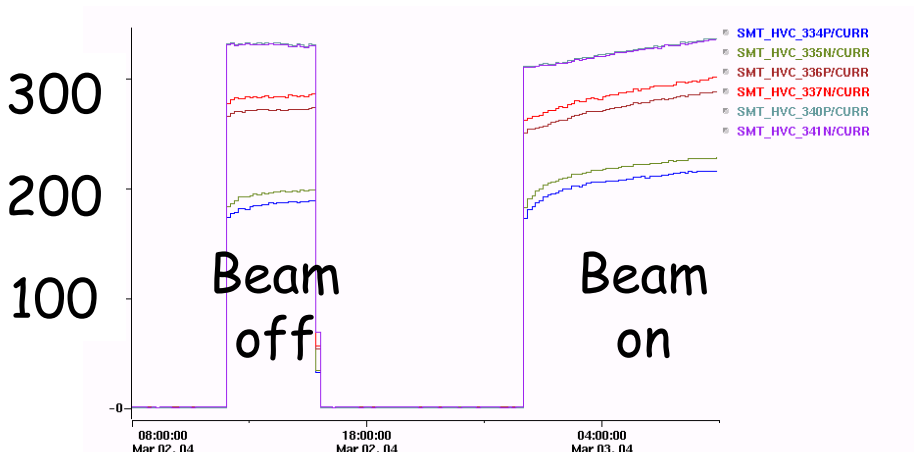
- 3 super-bunches
- 12 bunches in each super-bunch
- Correlated with preamp reset, but the reason is not so clear…
- Resetting preamp is much faster
- Grounding???



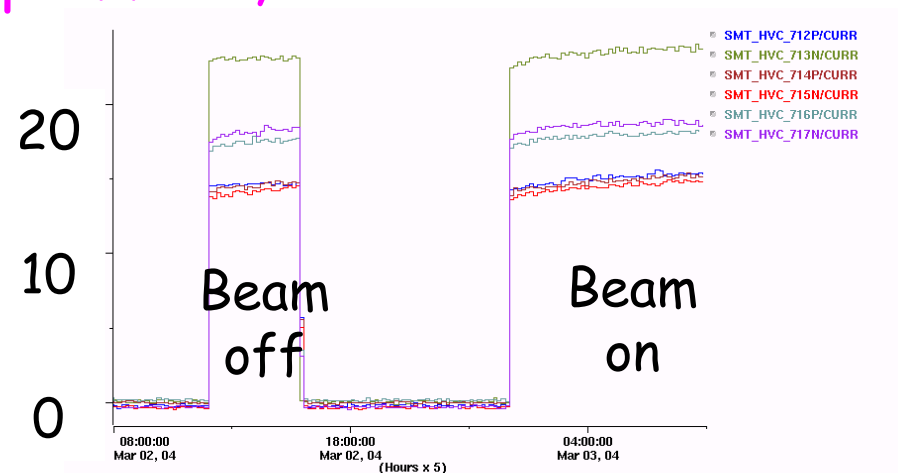
F-disk Noise



- This appeared only after a several months operation
- Only p-side of fraction of the Micron sensor
  - Looks like micro-discharge
- Force us to asymmetrically bias the sensors
- Charge-up effect, too



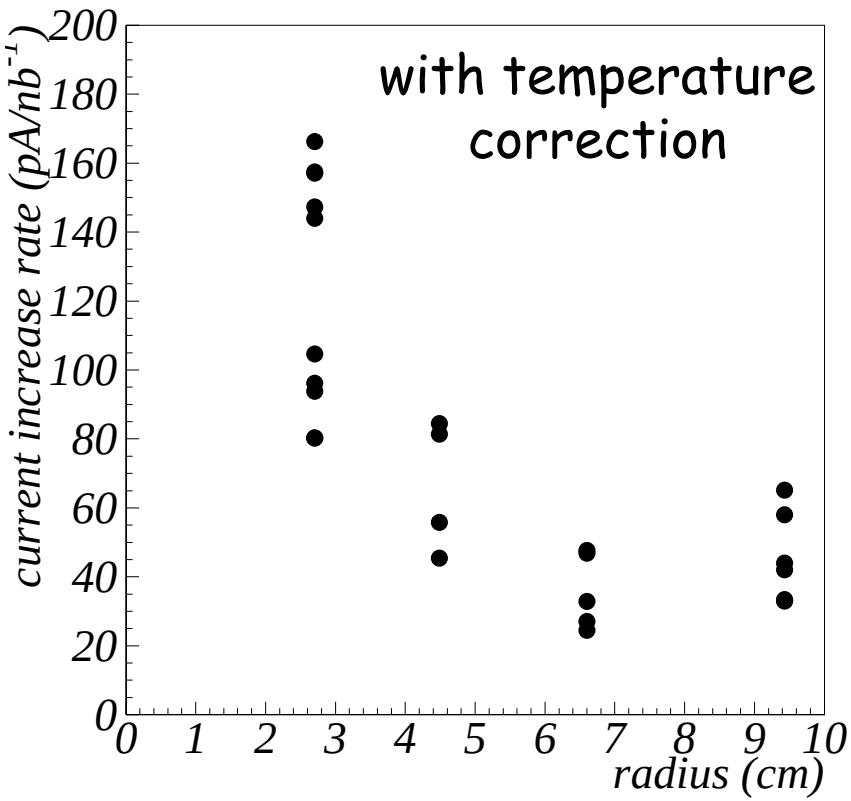
Micron sensors

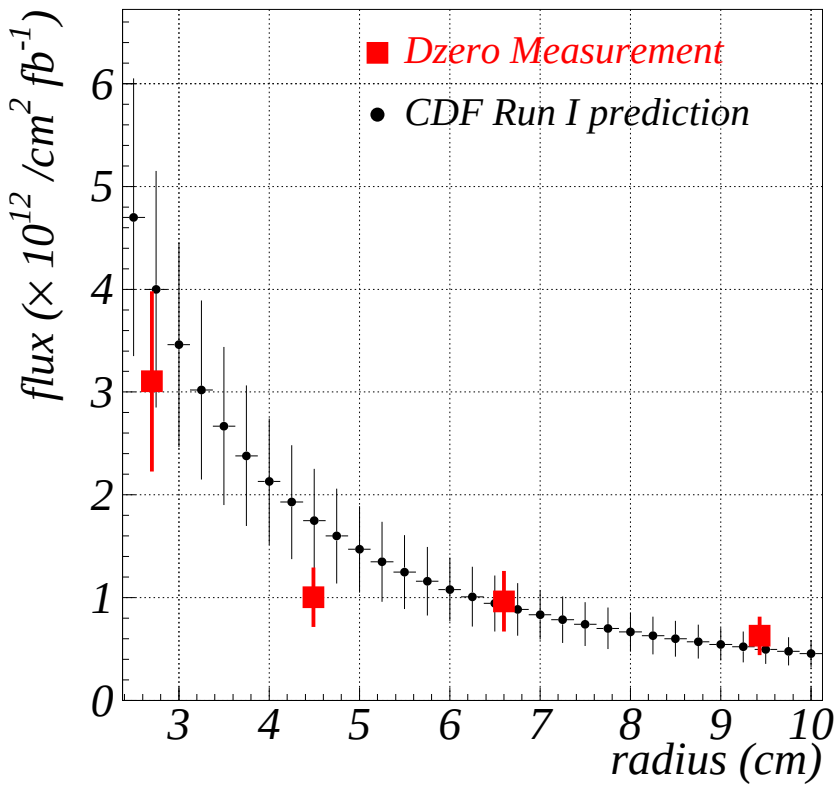


Eurysis sensors

Ageing

- Closer the beam, more rapidly the bulk current increases with time, as expected

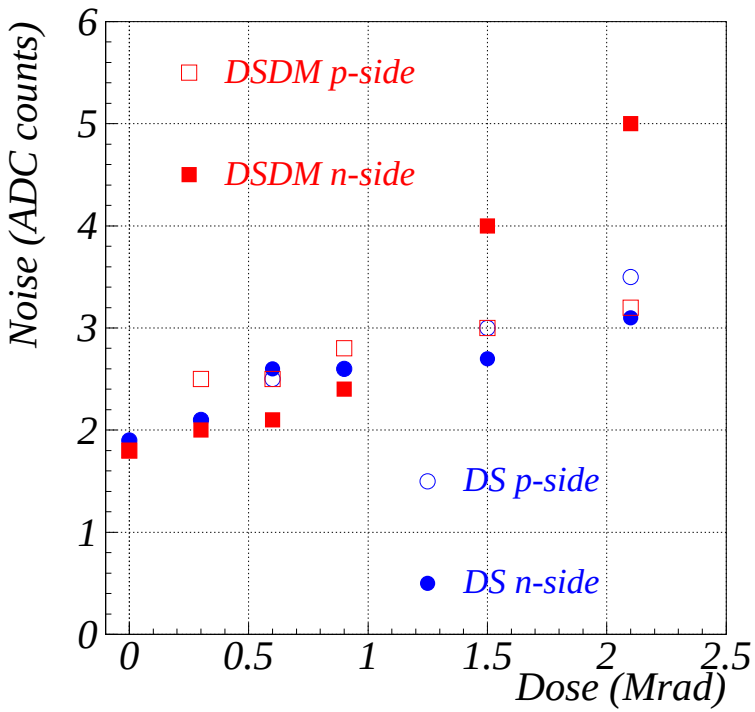




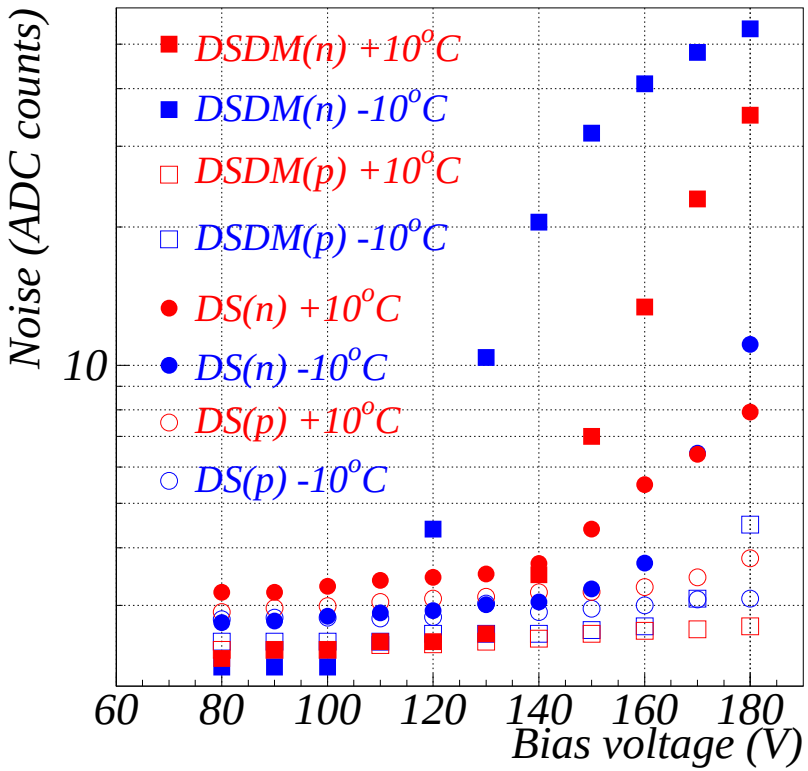
Irradiation

- Increase of leakage current
  - Increase in shot noise; not the show stopper
- Increase in trapped and surface charges in insulating layers
  - Lowers threshold for junction breakdown (micro-discharges)
  - Helps (!) to increase lifetime limited by micro-discharge on the n-side because the trapped positive charge tends to decrease the fields at n-p junctions
- Change in effective impurity concentration:
  - Remove donors and form acceptors in bulk silicon
  - n-type inverts to p-type after about 300 KRads
  - Depletion voltage decreases until inversion, then increases with dose
    - coupling capacitor breakdown
    - micro-discharge ← actually limits the lifetime

Irradiation – beam test

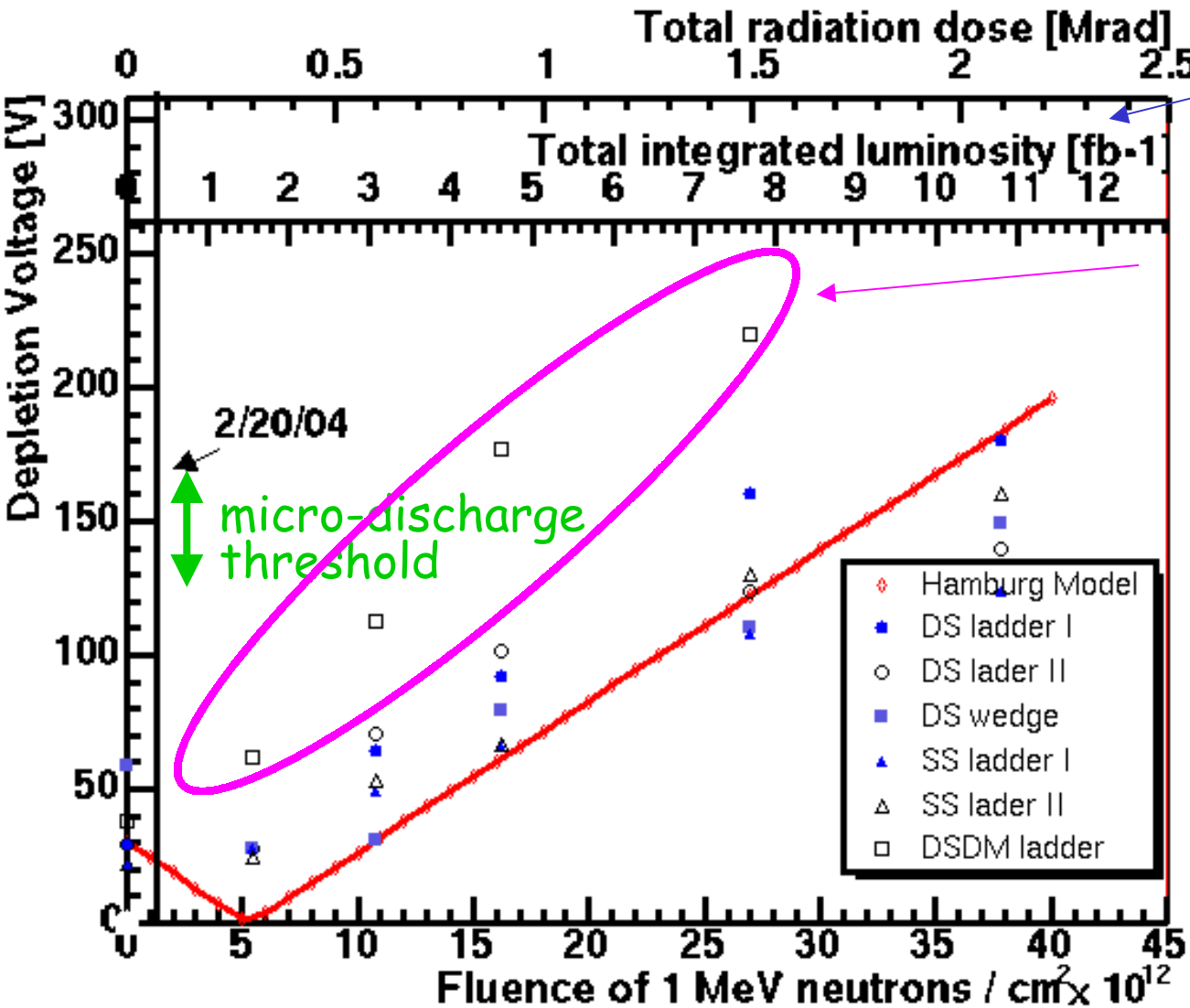


after 2.1 Mrad



- Rapid increase in noise vs bias voltage is typical characteristic of micro-discharge (@DSDM n-side)
  - Junction is close to n-side after type inversion
  - Temperature dependence

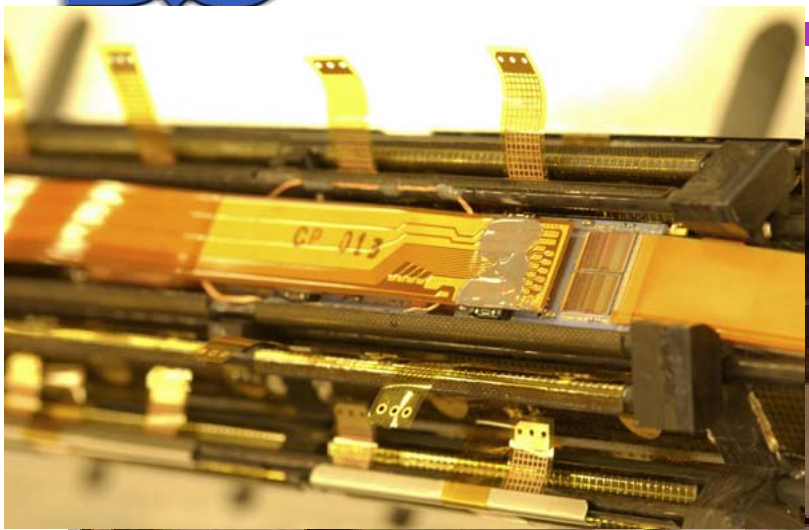
Irradiation – impact



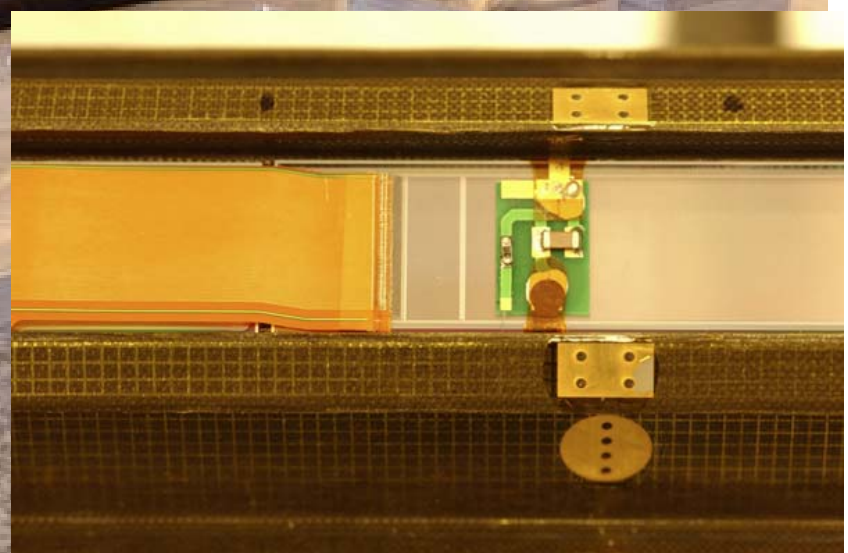
scaled at innermost layer (L1)

- Lifetime will be limited by abnormally fast reverse annealing at DSDM sensor ← 3.6~4.9 fb^{-1} with large (~50%) error

Addition of Innermost Layer (L0)



- Mitigate tracking losses due to radiation damage and HDI failure
- Provide more robust pattern recognition for higher luminosity



- Improve physics reach
  - Increase b-tagging efficiency by 20%
- Benefit from substantial investment for run IIb

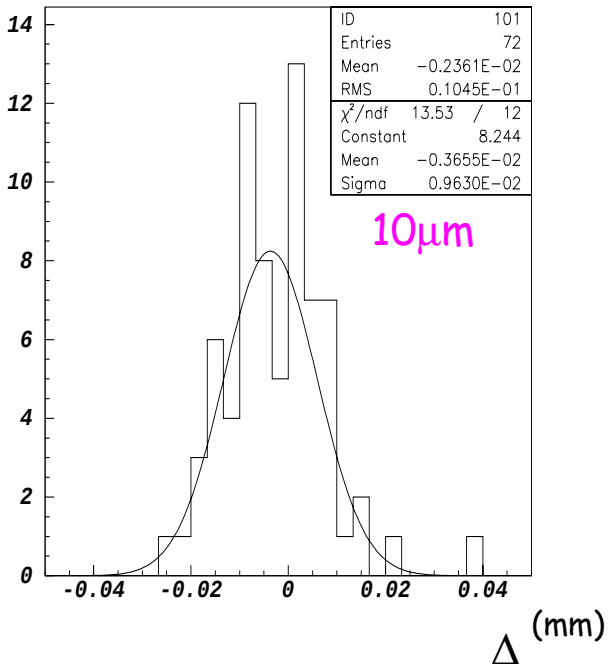
Conclusions

- Detector is working well, providing excellent physics, despite some operational problems
  - 10-15% of channels have problems of HDI
    - Mechanism of HDI failure needs to be understood
  - F-disk noise
- Using many types of sensors results in complications
  - Experience of DSDM sensor
  - Simpler design is preferred for future
- Micro-discharges of DSDM sensor at Layer 1 will limit the lifetime
  - L0 will be installed inside the Layer 1, which will insure functionality through run II

…backup slides

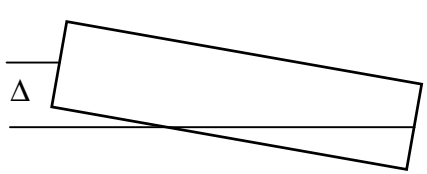
CMM Survey

In the plane of the ladder

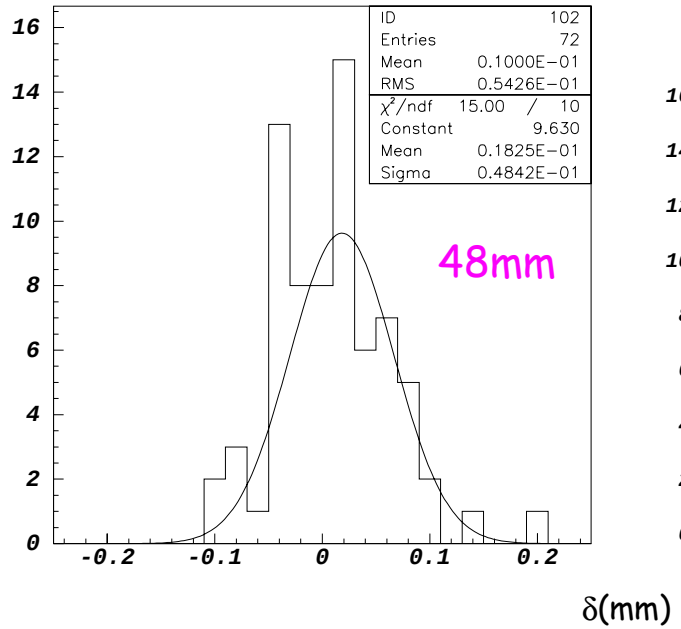


=10μm induces a 3μm error

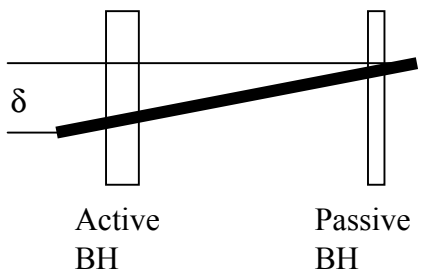
σ(Δ)



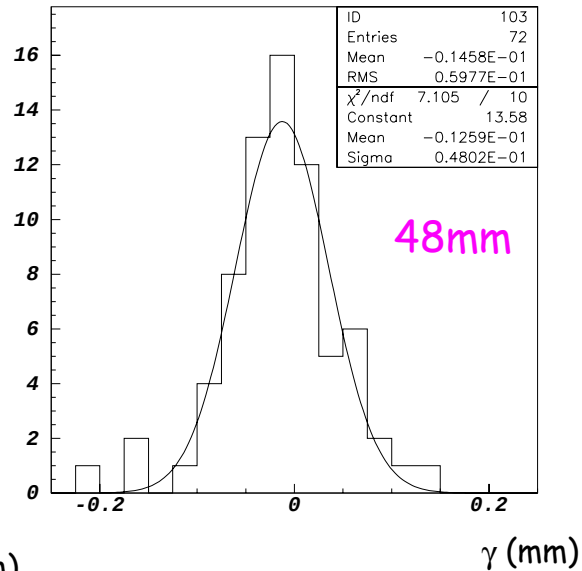
Around ladder short axis

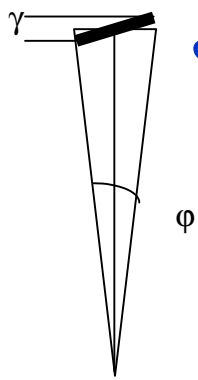


σ(δ) =48μm induces a 3μm error



Around ladder long axis

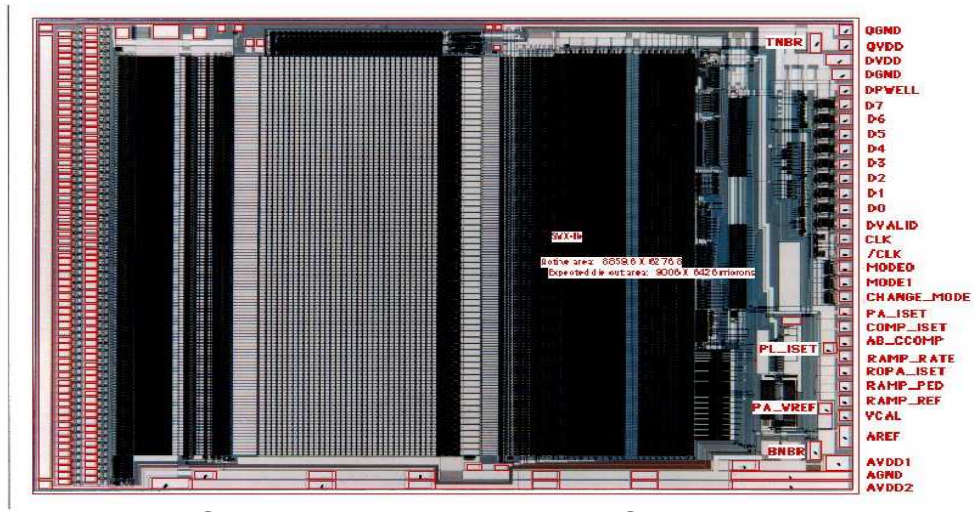


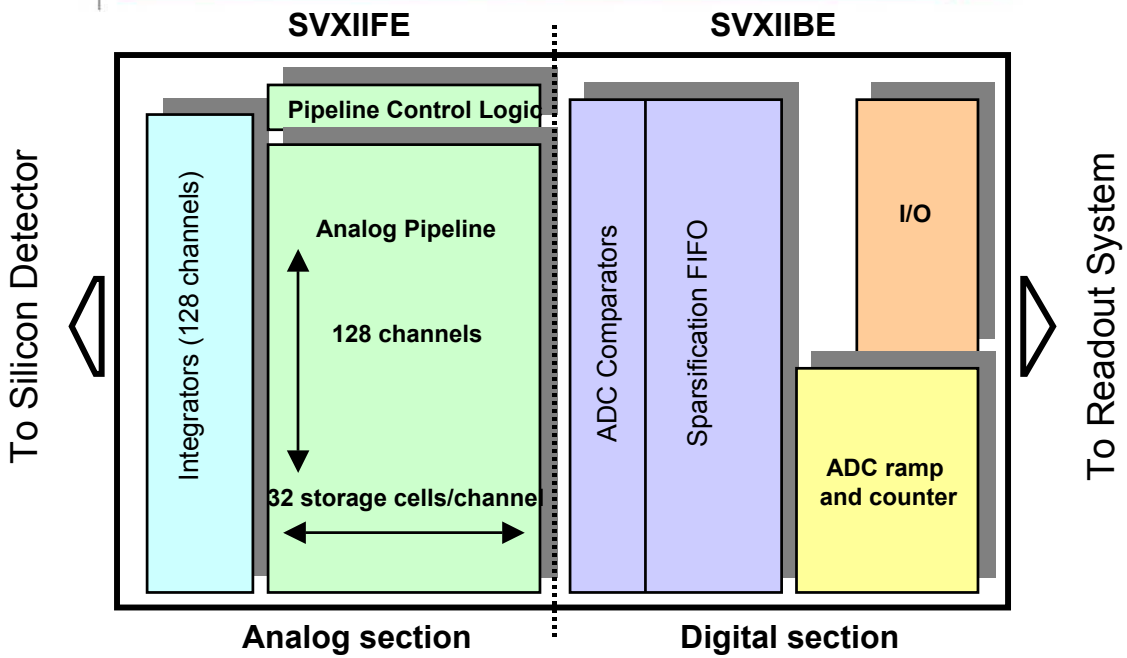


σ(γ) =48μm induces a 2μm error

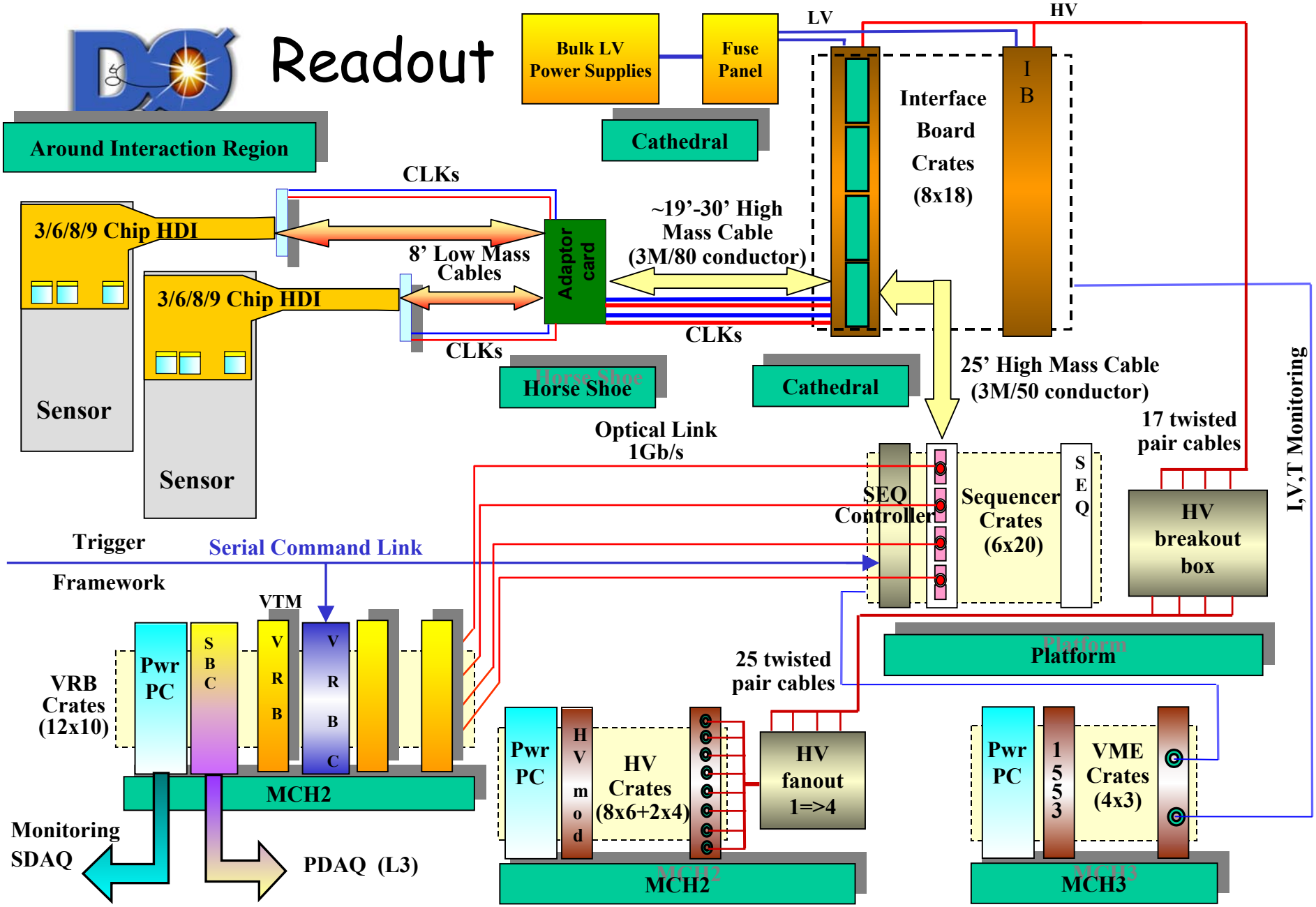
SVXIIe chip

- 1.2 um CMOS amplifier/analog delay/ADC chip fabricated in the UTMC rad hard process
- Designed by LBL/FNAL
- Some features:
  - 128 channels
  - 32 cell pipeline/channel
  - 8-bit Wilkinson ADCs
  - Sparsification
  - 53 MHz readout
  - 106 MHz digitization
  - 6.4 x 9.7 mm^2
  - ~ 85,000 transistors
  - noise: 490e + 50e/pF





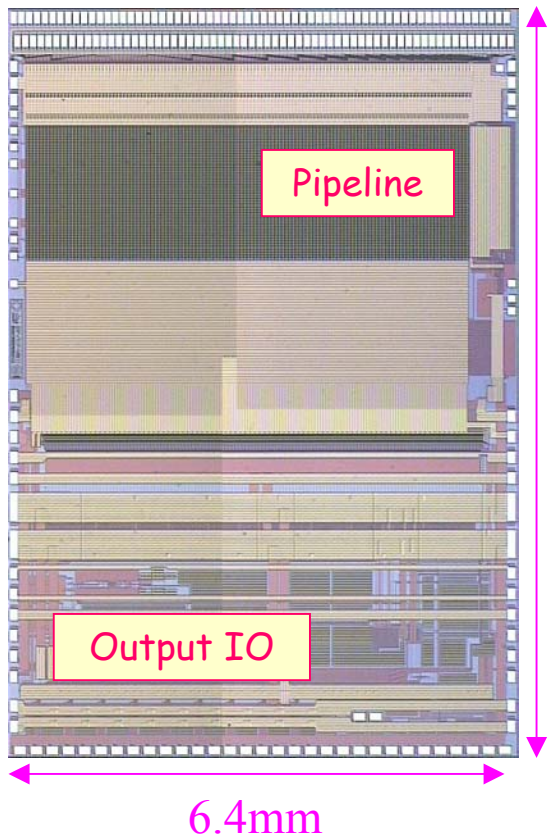
Readout



PowerPCs and Single Board Computers are accessed thru Ethernet

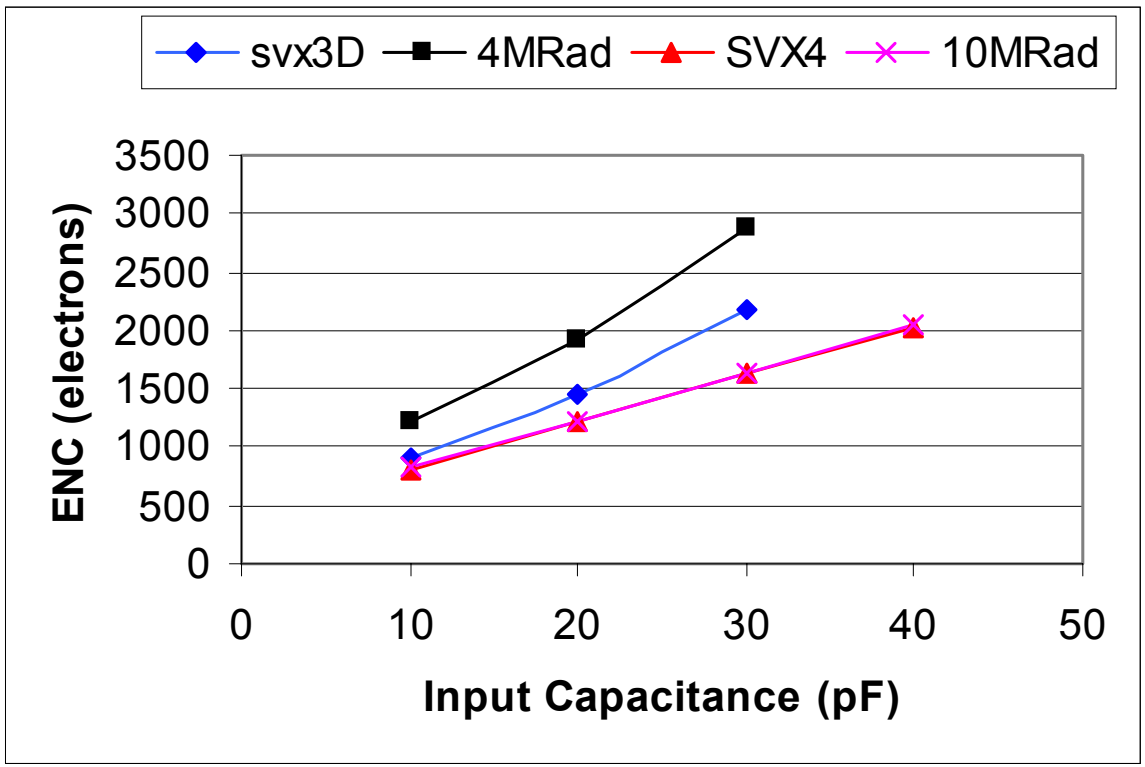
SVX4 Chip

- DZero and CDF (Fermilab and LBL) developed new readout chip SVX4
  - Successor of SVX2 and SVX3 chip
  - 0.25 μm technology, intrinsically rad-hard (>30Mrad)
  - 128 inputs and 46+1 pipeline cells
  - 8-bit ADC with sparsification
  - 53 MHz readout, 106 MHz digitization
  - Programmable test pattern for calibrations, ADC ramp, preamp bandwidth
  - Pinhole clamping
  - 2.5 V, power measured to 0.3 W/chip
- First version ready in June 2002
  - Fully functional chip, used for hybrid/module/full readout chain prototyping
- Second version ready in May 2003
  - Improved ADC design – good uniformity of pedestals
  - First test results all positive → accepted as a final version: 24 wafers ready
  - Ready for production → signoff completed

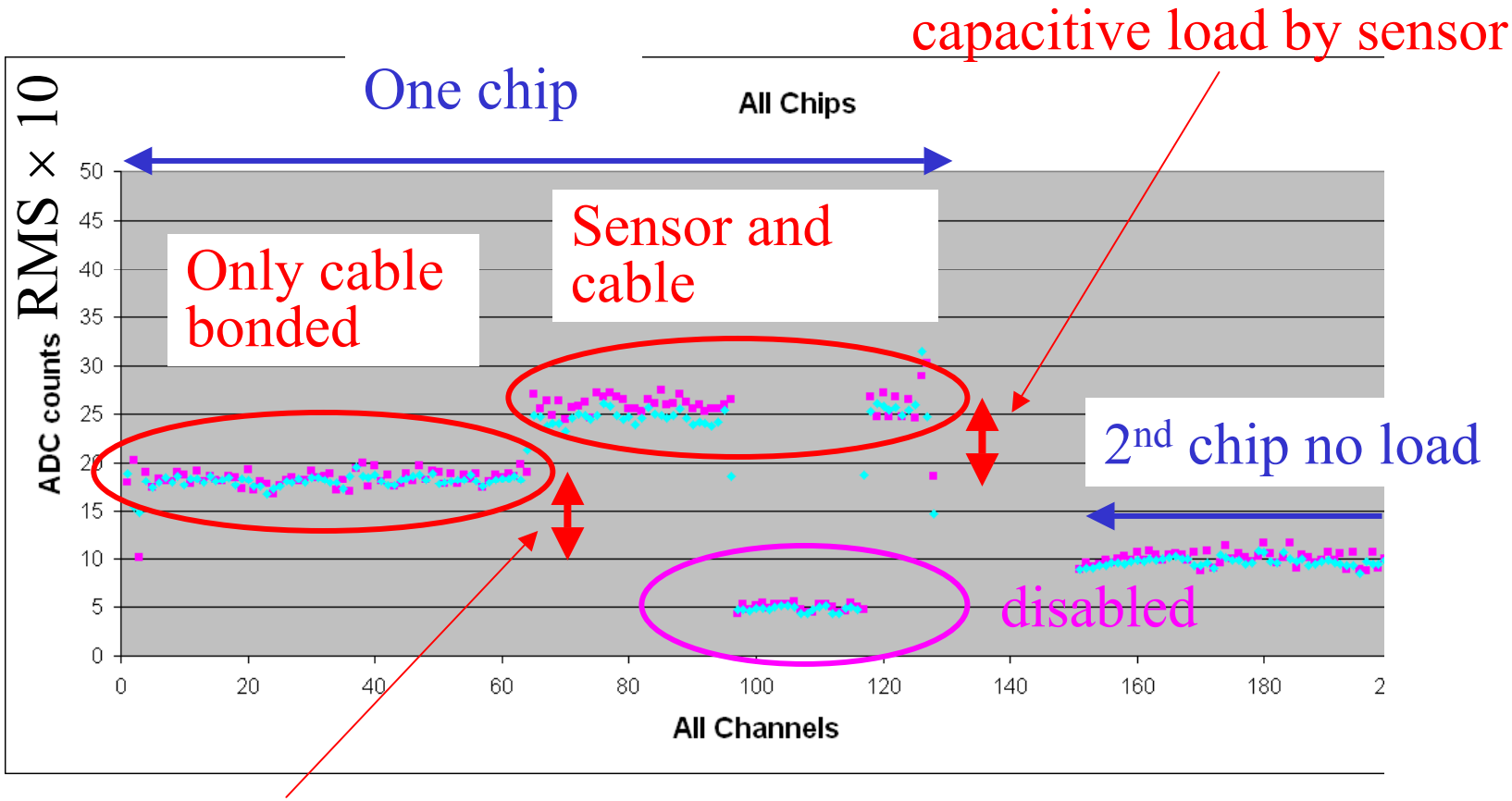


SVX4 Chip – continued

- Noise
  - For fixed rise time (69ns): ENC ≅ 300 + 41C (2025e⁻ @40pF)
  - Spec. < 2000e for 40pF @ 100ns rise time.
    ➔ very good noise performance.



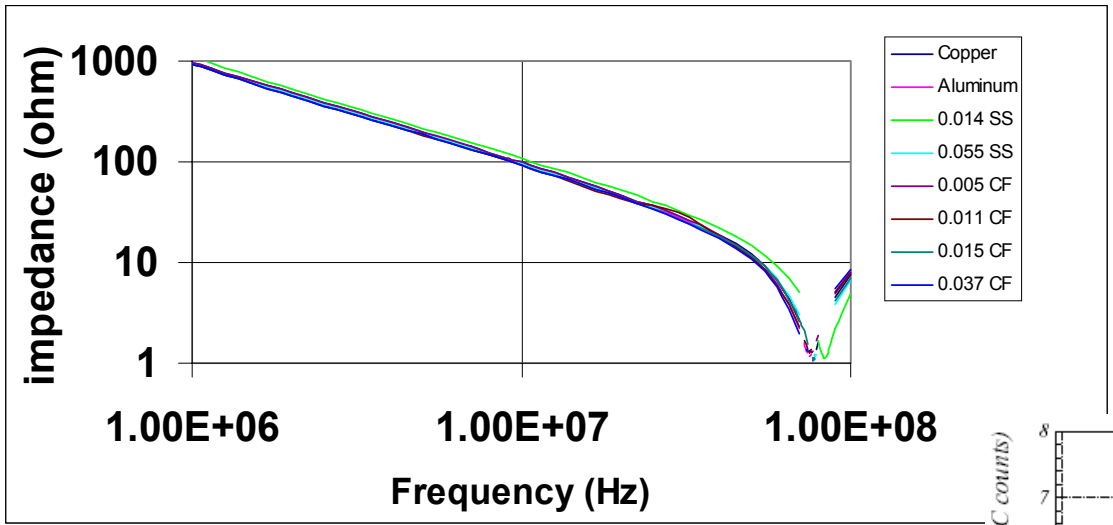
Noise of L0



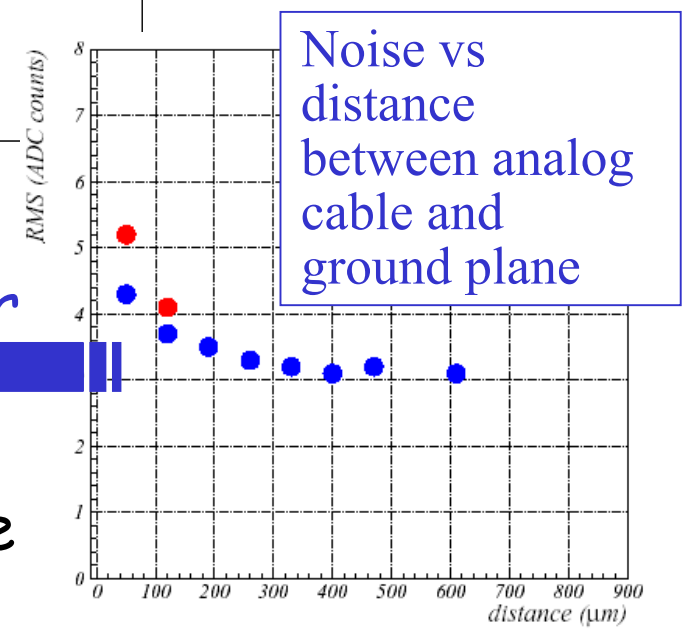
SVX4 ENC: const+41C ➔ 600e indicates C = 15pF for ~45cm

Application of Carbon Fiber

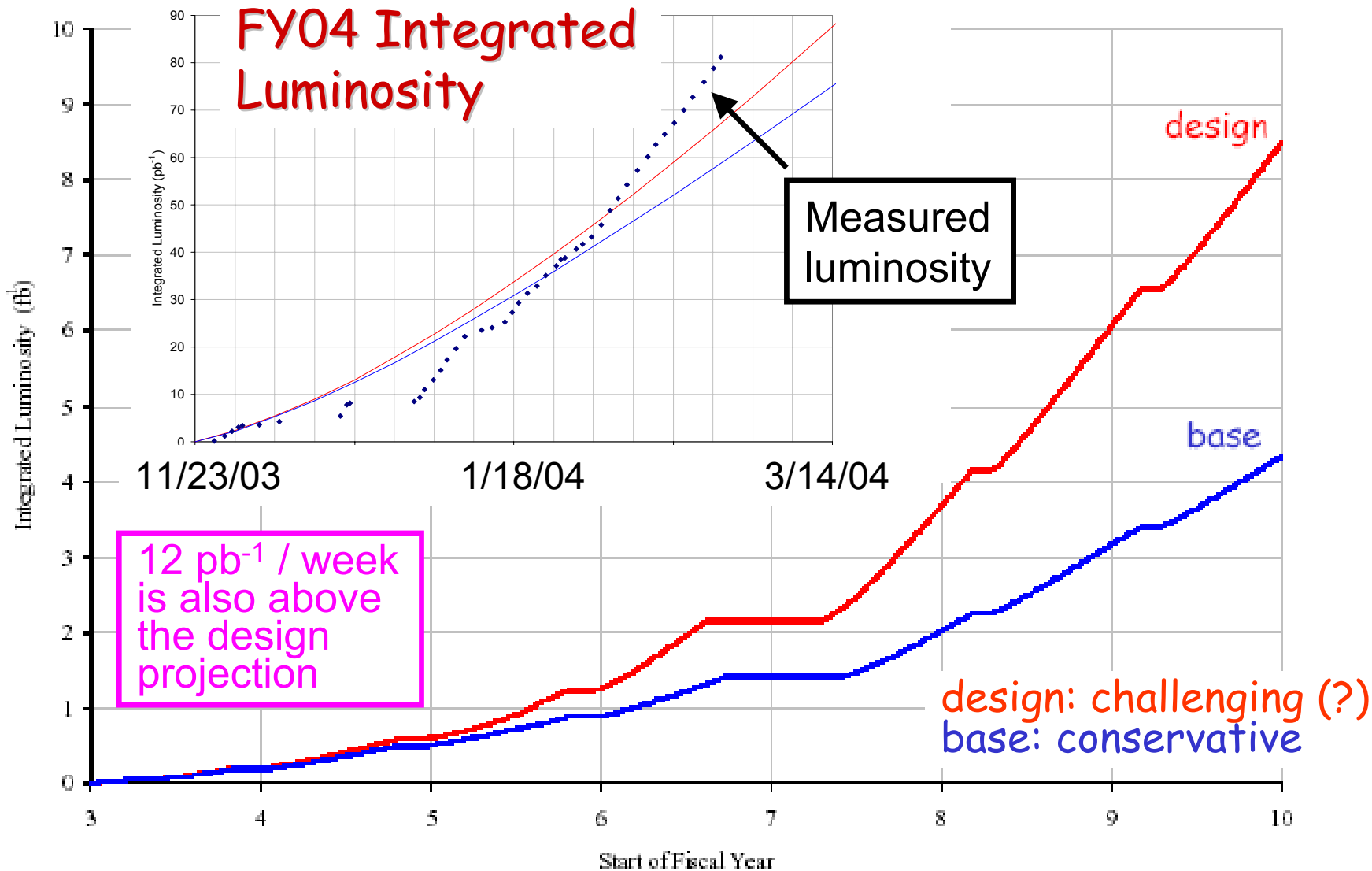
- Carbon fiber has high conductivity



➔ Special caution needed in grounding scheme



Noise vs distance between analog cable and ground plane

- Sensor/analog cable can be coupled to the support structur capacitively
- Controlling proximity between detector and support structure important

Projected Integrated Luminosity