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Hybrid production, assembly, and testing QC/QA

The silicon detector hybrids are electrical circuits that provide a platform for the SVX4 readout chips, which are coupled either directly via wirebonds (L1-5) or via analogue cables (L0) to the sensor strips. The hybrid circuits distribute power and control signals to the SVX4 chips and return the digitized data from the digital bus lines from the D0 data acquisition system through an AVX connector mounted to the hybrid, which connects to the external electronics system with a digital jumper cable. There are four flavors of hybrid: 2-chip used in L0, 6-chip used in L1, 10-chip axial and 10-chip stereo used in layers 2-5.

The hybrids consist of several parts, which are assembled to form the final readout unit. The hybrid substrate is a printed circuit on beryllia ceramic. Mounted on this are passive components, custom integrated circuit die called the SVX4 chip (two, six or ten depending on hybrid type) and a connector which allows the digital jumper cables to be attached to the circuit (AVX receptacle). Approximately 1200 production hybrids will need to be assembled and tested as shown in **Error! Reference source not found.**

Table 1. : Required hybrid quantities by type.

Hybrid Type	# chips/hybrid	# hybrids needed	# spares ordered	Total # of hybrids
L0	2	144	46	190
L1	6	72	28	100
L2A	10	336	104	440
L2S	10	336	104	440
TOTAL		888	282	1170

The sequence for the production, assembly, and testing of the hybrids includes the following steps:

1. Bare hybrid production (vendor)
2. Bare hybrid mechanical inspection (Fermilab)
3. Bare hybrid electrical testing (either Univ. of Kansas (KU) or California State Univ. at Fresno (CSUF))

4. Hybrid assembly including stuffing and wirebonding (vendor)
5. Initial Functionality test (KU or CSUF)
6. Burn-in (Fermilab)

A database tracks both the progress and quality of the hybrids throughout this process.

The database is accessible over the web for all institutions to track progress:

<http://dzero.phys.uic.edu/live/>. This database is the D0 Run2b silicon database managed by the Univ. of Illinois at Chicago (UIC). A paper traveler will accompany the hybrid as shown in Appendix I. There are repair loops that may be needed at various stages of the process. Figure 1 shows a diagram of this process. Each of these steps is described in more detail below along with the quality control steps taken. More information on these tests can also be found on the KU hybrid testing web page: <http://kuhep4.phsx.ukans.edu/~hep/run2b/>.

The hybrid is to be constructed of alternating thick film layers of gold and dielectric built up on a beryllia substrate. There are six conductor layers and five dielectric layers on the top side. Figure 2 shows a picture of a prototype L2A 10 chip hybrid. The hybrid circuits will be procured through vendors (a list of identified vendors is given in Table 2). The vendors must meet the following specifications:

- The gold on the top layer for wire bonding must be compatible with aluminum-wedge bonding.
- The plating on the top for the solder pads must be compatible with using solder paste with reflow temperatures of 205 to 220 °C (for example a Sn62Pb36/Ag2 solder paste by Qualitek such as Delta 792). A plating metal such as Dupont 4596 is recommended.
- The hybrid must be flat to within 0.05mm. (Layers of dielectric may be added to the backside of the substrate in order to meet this specification.)
- Total thickness of the finished hybrid must not exceed 1.0mm.
- Thickness of the metal trace layers is to be 7 to 9 um.
- Ground and power plane layer thickness is to be 4 to 6 um.
- Dielectric layer thickness is to be 40 to 60 um.
- The dielectric strength is to be 650V/mil or higher.
- Laser cutting of the final outline should be accurate to +/- 0.05mm
- Continuity testing of all pads will be performed at the production vendor, with a dual flying head probe test.

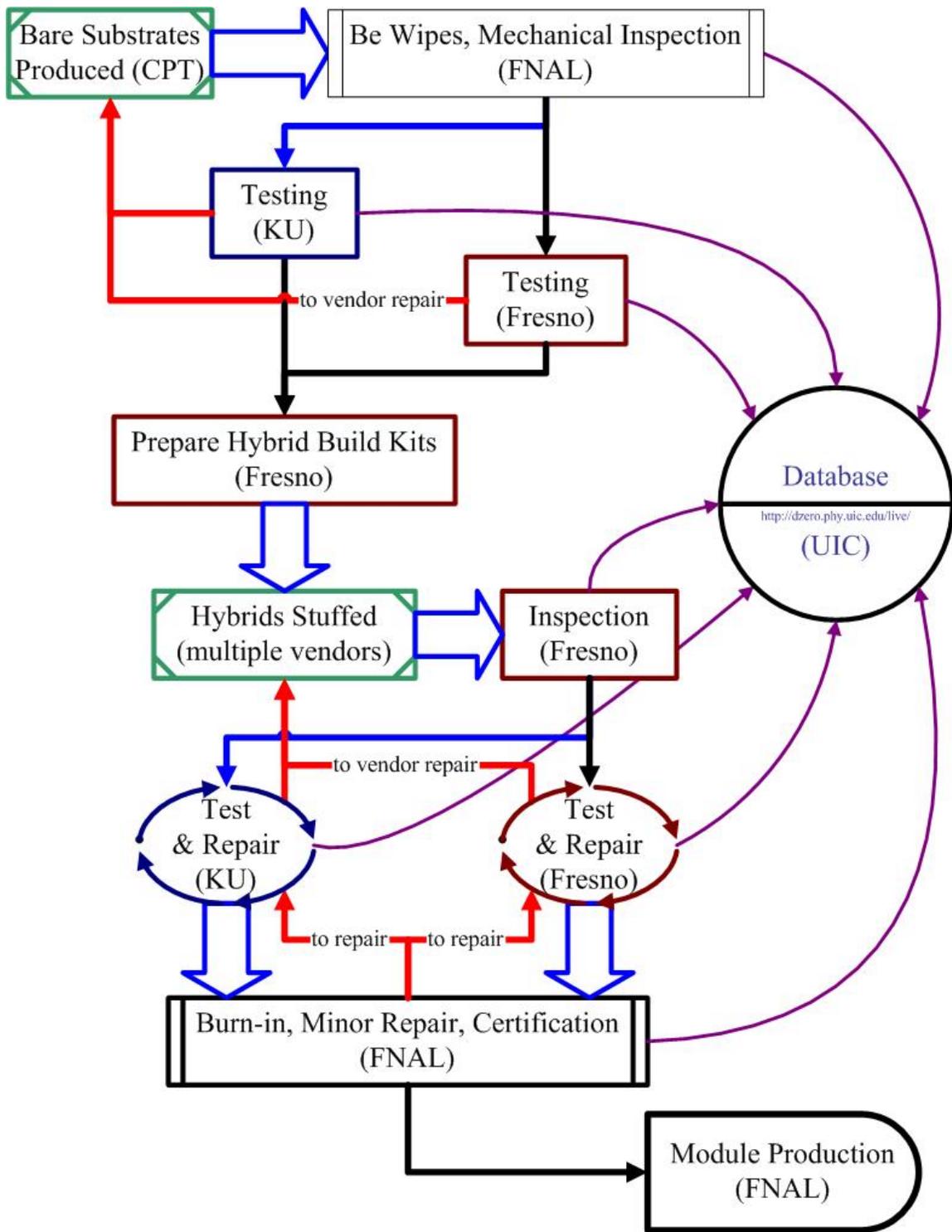


Figure 1: Hybrid production, assembly and testing flow diagram
Bare hybrid production

Figure 2. Layer 2 Axial 10 chip hybrid from vendor Amitron.
Approximately actual size.

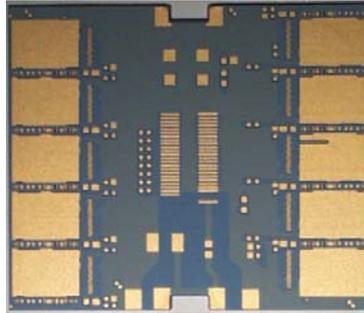


Table 2. Hybrid substrate vendor information

Identified Hybrid Production vendors			
Zentrix Technologies (formerly CPT)	Oceanside, CA	760 942-9811	
Amitron Thick Film Technologies	North Andover, MA	978 686-0622	

Bare hybrid mechanical testing at Fermilab

Bare hybrid substrates will be received at FNAL after production at vendors. A technician will be assigned to receive all hybrids at SiDet. The hybrids will be entered into the D0 database as well as the SiDet beryllium tracking spreadsheet. The hybrids will then be cleaned according to prescribed procedures and adhering to the associated JHA (Job Hazard Analysis). After this EH&S will be notified to take wipes of the hybrids for verification that they are not contaminated (beryllium). The results of these wipes are typically available is 1 week. If the wipes come back clean then EH&S approval will be entered into the D0 database and the SiDet beryllium tracking spreadsheet (name and date of approval). If any contamination is found the cleaning and wipes will be redone until the contamination is below the FNAL regulations.

Once the hybrid substrates are certified as non-contaminated they will undergo mechanical measurements to verify overall dimensional specifications. The primary measurement will be the flatness of the substrates. This measurement will be done on a CMM for each substrate and is expected to take about 5 minutes per part. The outside profile will be checked on a fraction of the parts using a machined gauge or a caliper. A small fraction may also undergo a more rigorous inspection using a CMM, depending on initial experiences with vendors. Mechanical certification (yes/no) will be entered in the D0 database for each substrate at this point. Substrates that meet all specifications at this point will be repackaged and shipped to either KU or Fresno for further visual and electrical inspection. Parts that do not meet specification will be reported immediately to the D0 personnel overseeing production at the vendor. Depending on the stipulations of

the production contract(s), these parts will either be returned to the vendor or retained for various purposes such as preproduction parts, personnel training etc.

Bare hybrid production quality control

A number of procedures will be used to ensure the hybrids meet all specifications and to minimize potential delays from the production vendor. These include:

- Visits to the vendor for consultation on the first runs of each type of hybrid, to check specifications, and fully understand production procedures.
- Require continuity and solderability testing at vendor including written verification of such testing and test results in contract.
- Each substrate will receive a unique identification number which will be used to track the part through production and testing, on travelers and in the database.
- The flatness of the bare hybrid will be checked with a go/no-go fixture, and some more extensively with a CMM.
- Visual inspection of all hybrids under the microscope looking for defects, specifically in bond pad and solder pad plating, and trace integrity.
- The vendor will test for continuity and shorts before shipping. University collaborators (at CSU Fresno and KU) will spot test samples of 10% or 10 of the lot (whichever is more) for verification.

Bare hybrid electrical testing

All of the prototype bare hybrids and 10% (or 10 hybrids whichever is larger) will be sent for further electrical testing at either KU or CSUF. The goal of these tests is to spot check the vendor. These tests include: a visual inspection, short to ground tests, continuity tests, and pad-to-pad short tests.

During the visual inspection, the quality of the visible top and bottom layers will be examined using a microscope. The size and appearance of the solder pads, AVX connector attachment pads, and SVX4 die pads will be examined.

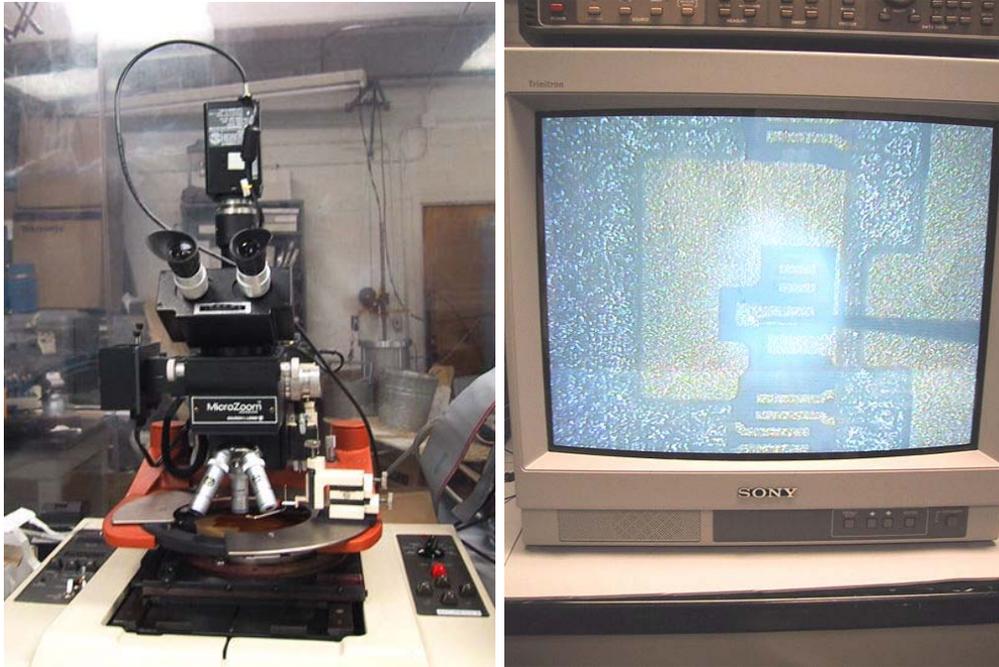


Figure 3. Rucker and Kolls 683A Semiautomatic wafer prober and display of L1 bare hybrid being tested at KU.

Both KU and CSUF have probe stations for conducting the electrical tests on bare hybrids. Figure 3 shows the KU probe station. These probe stations are controlled through a LabView program and allow an Excel spreadsheet describing the measurements of each hybrid to be written out. With the probe station the continuity and short tests are performed. The hybrid is aligned on the probe station and the testing procedures given on the KU hybrid testing web page are followed. The resistance of each pad to ground is measured and written out. Values below 300 Ohms are considered to be shorted and are flagged and that hybrid is retested manually for those pads. If the result is verified, the hybrid fails the test. For the continuity tests, values of the resistance less than 10 Ohms are required. Typical values of these resistances are less than 4 Ohms. Defects found in these tests are also verified manually before the hybrid is failed. Any open or short is considered to fail the hybrid. Failed hybrids are gathered and either sent back to the vendor or sent to Fermilab to be used as mechanical prototypes according to the purchasing agreements. Hybrid substrates which pass these electrical tests are shipped to CSUF where they will be combined with other components and documentation into build kits for delivery to hybrid assembly (stuffing) vendors.

Hybrid assembly

The assembly (stuffing) of the hybrid includes the attachment of the passive components, SVX4 chips (die), and connector. This work will be done by one or two vendors. The assembly must proceed in the following order: placement of the passive components (including AVX connector) with solder, attachment of the SVX4 die with epoxy followed by connection of the hybrid to each SVX4 die with aluminum wedge bonding. All bare

hybrid substrates and components are catalogued by CSUF and shipped directly from there to the assembly vendor.

Quality control adds a few more steps to the above. High yield and low volume characterize our project in comparison to how typical assembly vendors operate, which is high volume with less need for high yield. In validating our vendors we present to them the procedures outlined below. In addition to other documentation the vendor will record the identification number and location of each die for each hybrid, as well as data concerning the assembly of the batch of circuits (which are sent to the vendor in lots) in general, such as oven temperatures and wire bond adhesion measurements. One major request of the vendor is to check each hybrid with a simple ohmmeter continuity test to inspect for shorts to ground across the readout lines. This test occurs after the placement of passive components, where solder can sometimes cause shorts across components that are hard much harder to trouble shoot after full assembly. A fully stuffed and wirebonded L2A hybrid is shown in Figure 4.

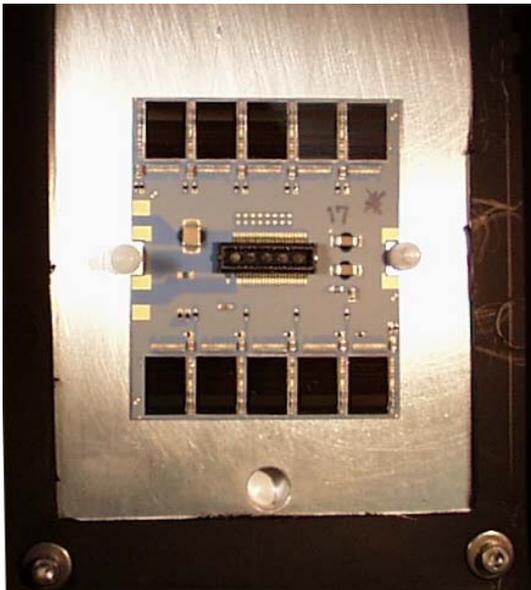


Figure 4. A L2A hybrid after all components have been placed onto it and wirebonds have been made.

Finally we have tight requirements on shipping. The wire bonds are quite delicate and we do not encapsulate them, as is standard practice in industry, due to the potential need for rework after assembly. The shipping containers will each contain one or two assembled hybrids and will be designed for easy access and loading, with special attention given to protecting the delicate wire bonds.

Table 1: Hybrid assembly vendor information.

Identified Hybrid assembly vendors		
Promex Ind. Inc.	Santa Clara, CA	408 496-0222
COB Solutions Inc	San Jose, CA	408 433-0200
Meltronix	San Diego, CA	858 292-7000

Table 4: Hybrid Assembly Process at Vendor

processing steps	description	documentation
Audit of kits to supplied BoM	Must supply Bill of Materials (BoM). Version numbers should be obvious on parts, and BoM should also have a version number. Vendor will verify all counts.	BoM, drawings, gerber files, shipping instructions, specifications
Visual inspection of hybrid circuits		
Wire Bond Pull tests	Test wire bonding on unused part of circuit (test one or two circuit boards from lot) Results will be included in run card documentation.	
<i>Surface mount (SMT)</i>		
apply solder paste w/screen	Vendor will make screen for solder paste using Gerber files produced from the CAD program. Specified solder paste is Sn62/Pb36/Ag2.	Gerber file
pick and place (automated)	Pick and Place machine uses Gerber file for part placement and denoting fiducial markers for the automated visual alignment. Machine also verifies value of each component placed (resistor or capacitor).	gerber file
put through oven	appropriate temperature profile is documented in run card. Reflow maximum temperature is 205 to 200 °C for approximately 20 seconds.	specifications
SMT visual inspection		
continuity test	test for shorts to ground of cable out pads. If short found send to rework technician to remove and hand replace component.	supply test board
<i>Die attach</i>		
visual inspection of die		

application of epoxy	Use conductive epoxy	specifications
hand placement of die	Die (chip) attachment is done by hand due to the close separation and need for documentation of position	
Wire Bonding	bake out epoxy	Specify oven temperature and duration
	Clean bond pads	Ar plasma
	wire bonding	
	visual inspection	
Packing	place in shipping containers supplied with kit (much care with open wire bonds!!)	detailed instructions
Shipping		

The selection of assembly vendor will depend on their ability to meet the specifications of assembly, to complete assembly with reasonable turn around (typically three weeks), and to be competitively priced. Table 3 lists identified assembly vendors and Table 4 lists the process control at the vendor.

Hybrid assembly quality control

Again we have procedures to ensure as best we can that the hybrid assembly meets all specifications and minimizes potential delays from the vendor. These include:

- Systematic organization of assembly documentation and revision numbers, along with an archive of changes in the database.
- Accounting practices on inventory of components and tracking of each hybrid by serial number.
- Redundant verification of assembly documentation before and after submission to vendor.
- Site visits by participating physicists to the vendors for consultation of assembly procedures and active monitoring of the initial assembly runs.
- Expanded Quality Assessment requirements on the vendor's assembly line, through requested additional tests during assembly and through extensive documentation of assembly line parameters, machine settings, and inspection results. (Please see **Error! Reference source not found.** for details).
- Testing at collaborating institutions (CSU Fresno and KU) including: extensive visual inspection for damage, assessment of workmanship and verification of component assembly against certified assembly drawings.

- Initial functionality testing at the Universities using SVX4 readout systems.
- Quick turnaround on these tests upon receipt of assembled hybrids and immediate feedback on problems or improvements to vendors.
- Careful recording of all inspection and test results in the database
- Concise recording and classification of found problems.
- Careful consideration in the design and use of shipping containers for the delicate assembled hybrids.

All the above rely on an open and collaborative relationship with the vendor, in terms of access to the vendor's floor, assembly line, and technical/engineering support.

Initial Functionality Testing

After CSUF receives the hybrids from the assembly vendor, they will either perform an initial functionality test there, or ship the hybrids to KU for the initial functionality test. CSUF and KU are responsible for all interaction with the vendors, for the performance of the initial functionality tests, and for minor repairs on the stuffed hybrids. These tests will use the SASEQ teststands described in the Run2b Silicon TDR. All test results will be entered into the database. The following steps will be performed on the stuffed hybrids. All tests will take place in a clean room environment.

The visual inspection is done using a high-powered microscope. The purpose is to obtain quick feedback for the stuffing vendors, including wire bonder general problems (too-long tails for example) and to attempt to ameliorate any problems before electrical tests. Typical "repairs" at this point may include manually straightening out crushed bonds, identify missing or broken wire bonds for repair in-house, locating SVX4 chips with obvious defects, and also to blow off or pick off debris from previous handling. A K&S manual wire bonder is available at both university hybrid testing sites for these quick repairs.

After the visual inspection, there will be a static electrical test to check for power shorts and to verify the connection of the platinum temperature measuring resistor. Hybrids with shorts will be set aside for possible debugging. The functional electronic readout tests are performed using 1 SASEq stands at each university. These stands are already in place from the Run2a detector and just need to be modified for use with the SVX4 chip. This is the basic test of download and readout. We require 100 successful downloads, and error free readout of 10,000 calibration and pedestal events. In addition one cycle (requiring about 15 minutes per hybrid) of the standard burn-in test as described below is performed.

Download failures, are if possible, localized to a single chip using a manual probe station in conjunction with an oscilloscope and logic analyzer, and defective SVX4 chips marked for replacement. Hybrids with problems are scanned at high magnification (50-250X) to search for chip and other defects. For the Run2a hybrids, in about 50% of the download and readout failures cases, a SVX2 chip flaw was visible. For the Run2a production:

- Debugging success was anecdotally stated to be >70%, meaning that at least 70% of download and readout failures, when localizable to a single chip, could be recovered.
- About 30% of the hybrids with shorts were recovered, in some cases by burning off debris at "high" current (less than 1A in order not to melt wire bonds), or by manipulation of hybrid tails.

The initial yield of working hybrids that were stuffed for Run2a was 70% and varied significantly between different hybrid types and batches. This yield implied that it was cost effective to ship the stuffed and wirebonded hybrids to universities for the initial functionality test. The university collaborators would then debug the non-functional hybrids. The eventual yield for working hybrids that were stuffed was around 90%. The plans for testing are being prepared assuming yields such as those found in Run2a for the stuffing and wirebonding vendors.

Burn-in Tests for hybrids

The burn-in test is a part of the standard testing procedure during module production. It is the primary Quality Assurance testing suite used to certify and "rate" hybrid quality. It will be performed first on the stuffed hybrids after they pass the initial functionality test. At this point the goal of the test is to select good hybrids for module assembly. The idea of the initial burn-in test is to run every component for a period of 60-72 hours at elevated temperature and monitor its performance. In particular, measure pedestals, total noise, random noise and gain and examine occupancy in the sparsification mode. Other parameters that will be monitored include temperature and chip current. Typical problems that are revealed by the burn-in test are SVX chip failures, broken and shorted bonds, grounding problems, noisy strips, etc. Physicist shifters will do the hybrid burn-in tests. These shifters will be supervised and trained by a lead physicist who will oversee the operation. The lead physicist will grade the hybrids according to the number of dead and noisy channels after the burn-in test.

We plan to set up two hybrid burn-in stations, with a capacity of 16 chains each, and two module burn-in stations, with a capacity of 32 channels each. This gives us a total capacity of 96 channels per burn-in cycle, which we consider adequate to accommodate an expected production rate of 60 detectors per week. For comparison, our production rate during Run2A was 20 modules per week, and our burn-in capability was 32 channels. We expect to have two burn-in cycles per week, per station, on average. Note that the module burn-in stations can be used both for modules and for hybrid burn-in.

The large volume of information coming from the burn-in test and the necessity to run the test for many devices using non-expert shifters imposes the requirement that the burn-in test software must be user friendly. The Run2A software was based on a user-friendly Graphic User Interface written in the TCL/TK scripting language with the graphical toolkit in the Windows environment. This choice of software interface created a flexible system for performing a variety of tests using executables written in different

programming languages for data taking, monitoring and data analysis. We plan to reuse the Run2A burn-in software, modifying it for our new modules, and reducing the amount of human intervention in processing the data and storing the information. Given the factor of three increase in our production rate compared to Run2A, we will do most of the processing of data and storage of summary plots in the database automatically.

The different tests performed during burn-in are the following:

- Temperature sensor test: performed at room temperature, before the SVX chip is powered.
- Data integrity check: tests the stability of the SVX chip downloading and the correctness of the individual chip identification number (ID) and channel numbers in the SVX data.
- Long burn-in test consists of a number of runs with an idle interval between them in which the chips remain powered. In each run, the SVX chips are tested in “read all” and “read neighbor” modes. In “read all” mode, chip pedestals are read out to evaluate the noise in each SVX channel and then chip calibration is performed. In sparsification (“read neighbor”) mode, where only the channels whose response exceeds the preset threshold and their immediate neighbors have to be read out, the frequency of false readouts is studied.

For a detailed description of the tests performed during burn-in in Run2A, see d0note 3841. We plan to run the same tests during Run2b.

Hybrid Traveler

Hybrid # _____

Type (circle one) L0 L1 L2A L2S

Manufacturer _____

Stuffing Vendor _____

Build Kit # _____

Procedure	Name	Date	Comments
Received at Fermilab			
Be wipe OK			
Mechanical meas.			
Bare hybrid probe			
Shipment to Stuffing Vendor			
Short test at stuffing vendor			
Wirebond pull test			
Shipment from Stuffing Vendor			
Received at CSUF			
Shipped for I.F.T			
Initial Functionality Test (IFT)			
Shipped from IFT			
Received at Fermilab			
Fermilab Initial Test			
Burn-in			
Certify & Rate			

SVX4 chips used: