

Silicon Electronics & Readout

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April 16th 2002, Temple Review

- Overview of Run 2B readout
- SVX4 chip
- Analog flex cable
- Hybrids
- Interfacing to Run 2A readout
- Plans for 2002
- Summary

Introduction

- Run2B Silicon readout is based on
 - new SVX4 chip
 - Run 2A readout with minimal modifications
 - Conservative, low risk solutions with minimum R&D
- Baseline established in September 2001
 - Reviewed in December 2001, found in good shape
 - Steady progress last 4 months
 - Conceptual design stage evolved to detailed design & prototyping stage
- In the following will concentrate on latest developments
 - Supporting documentation

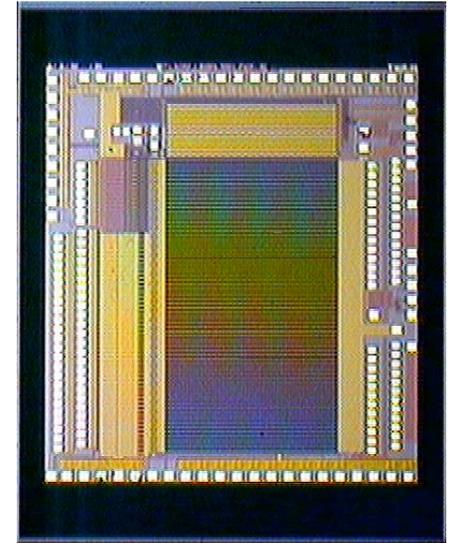
<http://d0server1.fnal.gov/projects/run2b/Silicon/www/smt2b/readout/readout.html>

SVX4 Chip

- New chip : SVX4
 - Designed by Fermilab/LBNL/Padua
 - Based on SVX3, compatible with SVX2. We proved that D0 DAQ can operate with SVX3
 - 0.25 μm technology, intrinsically radiation hard
 - Several new schematics solutions (back-end)
 - D0 will use differential readout
 - ❖ Same chip for D0 and CDF
 - ❖ Same pad ring
 - ❖ Difference between D0 and CDF defined by one bond (GND or DVDD)
 - ❖ A lot of similarities with CDF in chip testing and hybrid design

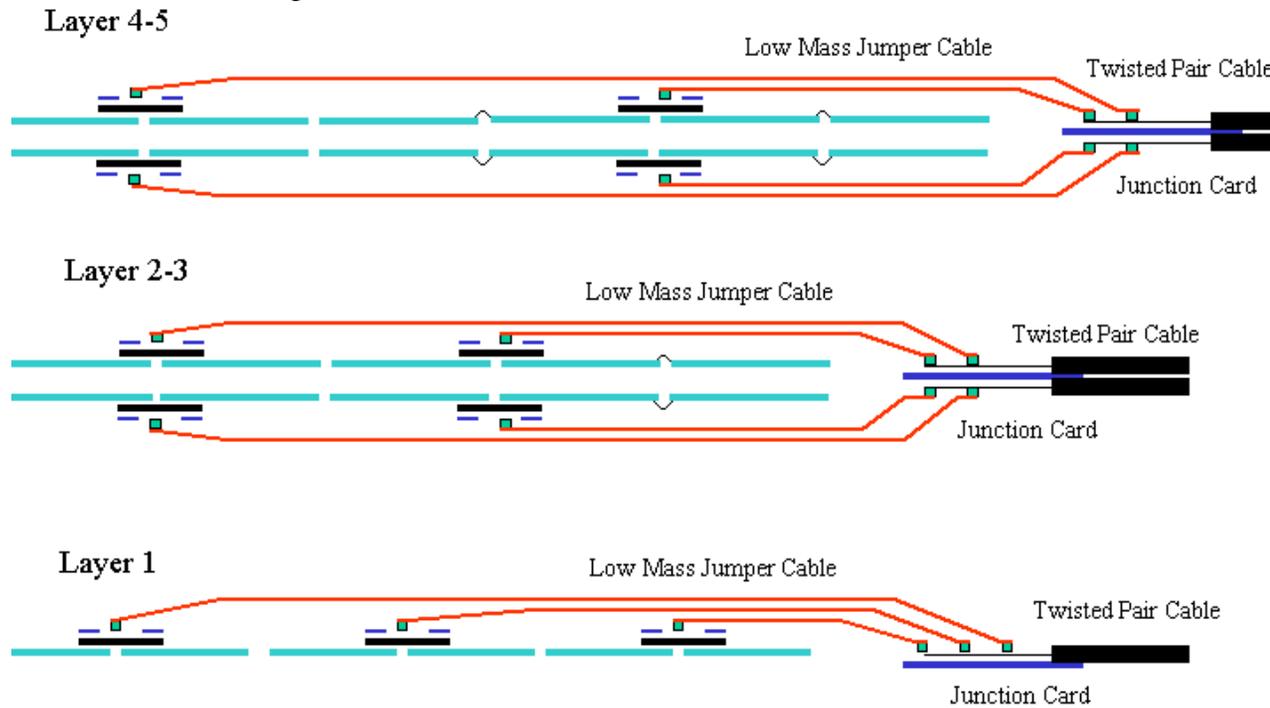
SVX4 Chip

- Front End design completed in June 2001
 - FE test chip tested in September 2001
 - Optimum preamp ENC = $450e + 43.0e/pF$
 - Pipeline validated
 - Excellent radiation hardness
- Full chip layout and simulation completed in March 2002
 - Prototype submitted to MOSIS on March 28 2002
 - Two versions for prototyping
 - ❖ Conservative
 - ❖ On-chip bypassing of analog voltage
 - Chip dimensions 9.17 mm x 6.42 mm, power < 0.5W/chip
 - Chips available for tests in June 2002
- Joint test effort of CDF & D0 at LBL and Fermilab
 - Important to test prototypes as extensively as possible to minimize extra submissions
- Production run planned in April 2003
 - Second prototype submission is assumed in the schedule



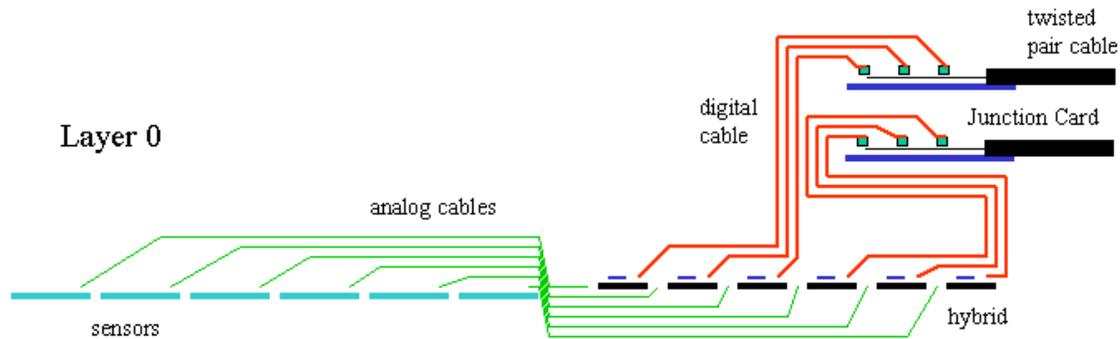
FE test chip

Layers 1 - 5 Readout



- On-board double-ended beryllia hybrid
- Reduction of readout cables is achieved by
 - Analog ganging : connected strips in L2-5
 - Digital ganging : chips bonded to different sensors are daisy chained on hybrid in L1-5
- Low mass digital flex (jumper) cable with connectors on both sides

Layer 0 Readout



- small radius & minimal material => flex analog cables
- flex length is equalized
- two-chip hybrids, no ganging
- beyond hybrid : identical to L1
- challenging :
 - noise performance
 - manufacturing and assembly

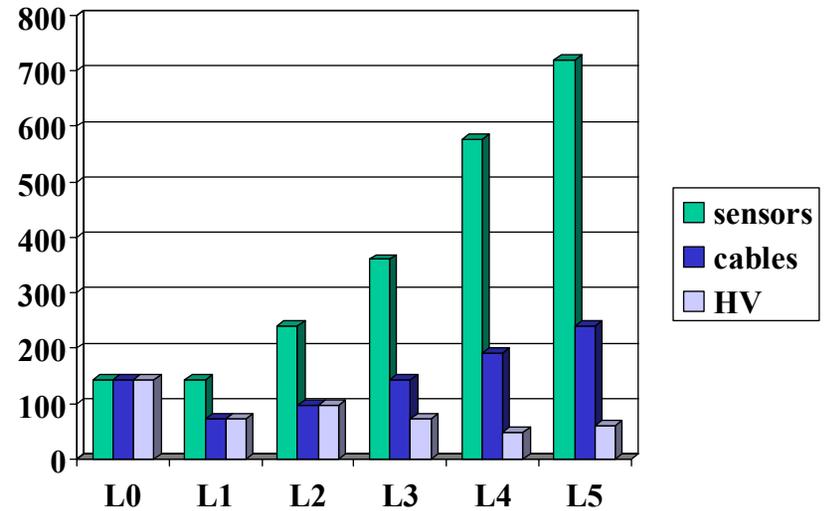
Cable Count

Layer SVX4/Hybrid # readout # HV cables

Layer	SVX4/Hybrid	# readout cables	# HV cables
0	2	144	144
1	6	72	72
2	10	96	96
3	10	144	72
4	10	192	48
5	10	240	60

all layers 888 492

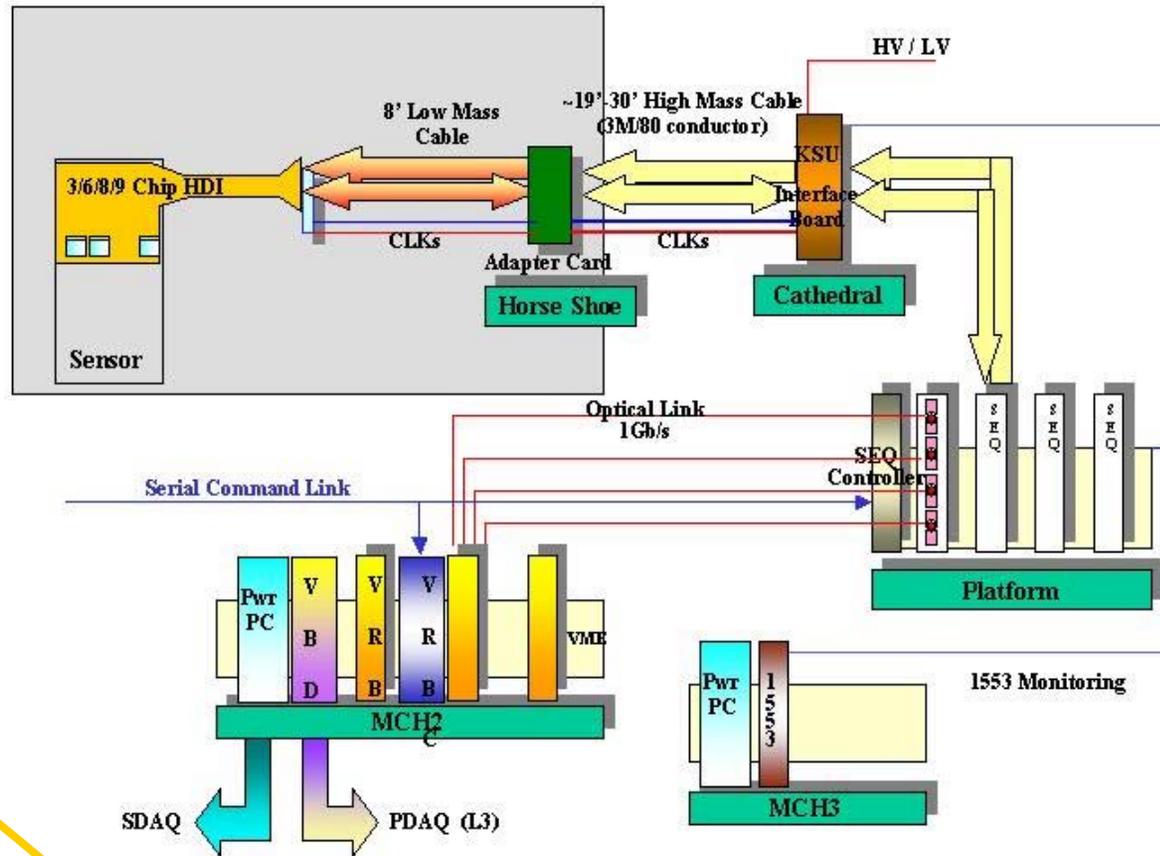
Run 2A 912



of sensors and cables per layer

Run 2B cable count is smaller than Run 2A cable count

Changes of Run 2A Readout

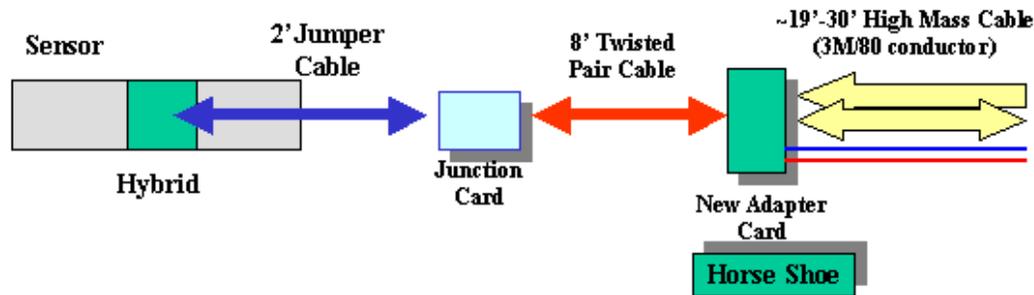


Modifications

- Signal level translation 5 V – 2.5 V
- Tight spec on 2.5 V (2.25 – 2.75 V) => Voltage regulation
- Mapping between SVX4 and SVX2
- Differential / Single-Ended translation
- Some changes in LV / HV power supplies, Interface Crates

Run 2B Readout

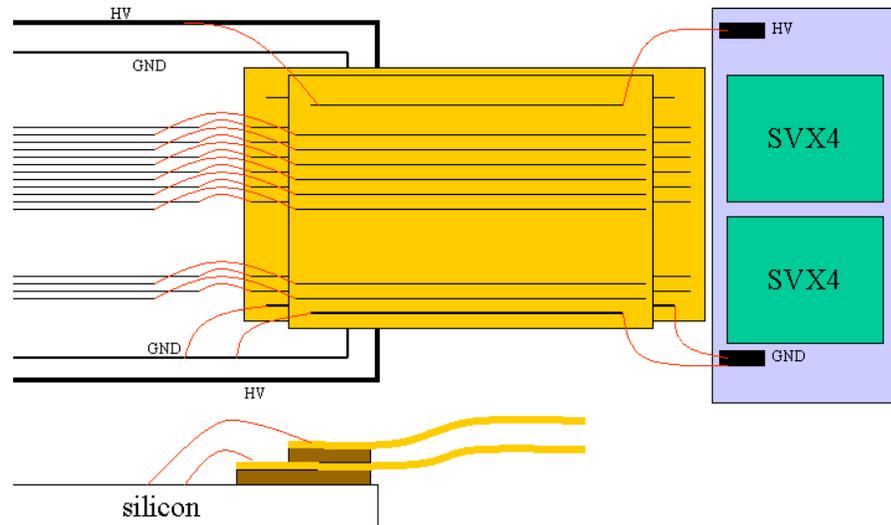
- Preserve Run 2A segmentation of readout :
 - One hybrid is an independent unit (separate cable) up to an accessible region.
 - ❖ Proven to be successful during Run 2A commissioning.



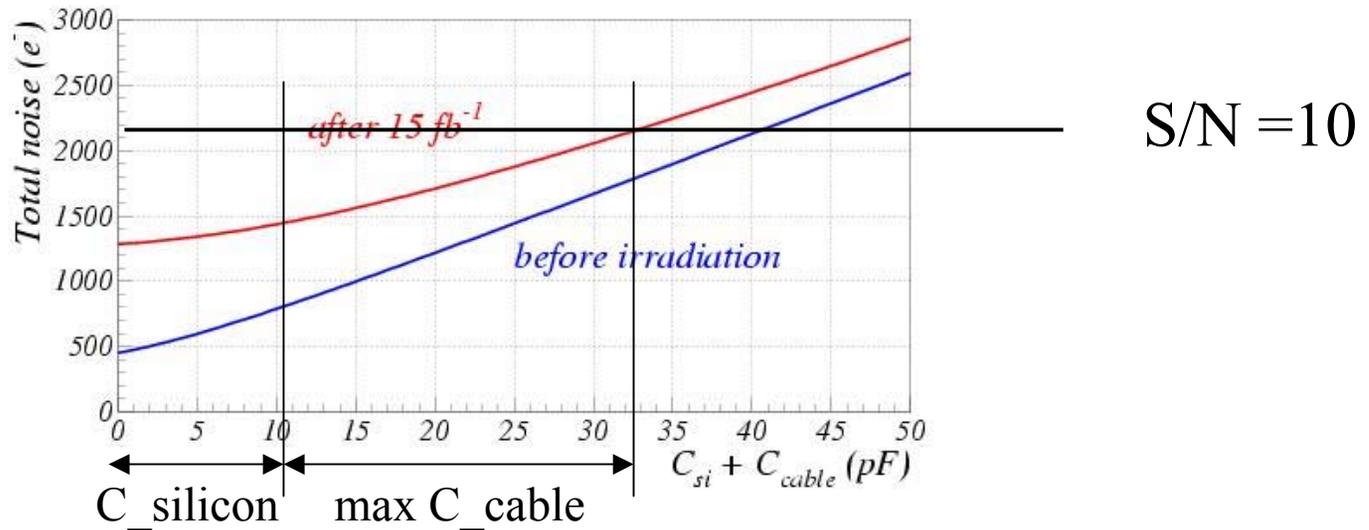
- Jumper Cable - Junction Card - Twisted Pair Cable – **Adapter Card**
- New Adapter Card is active, implements necessary modifications
- Junction Cards are located in an accessible area
- Twisted Pair Cable is well suited for differential SVX4 readout

Analog Flex Cables

- Low mass, fine pitch cables for Layer 0
 - CDF L00 design :
 - ❖ 50 um pitch
 - ❖ 6-8 um trace width
 - ❖ Fan-in/fan-out region
 - Adopted less aggressive design
 - ❖ Wider traces 15-20 um
 - ❖ Constant 100 um pitch without fan-out region
 - ❖ Two cables shifted by 50 um, effective pitch 50 um



Layer 0 noise

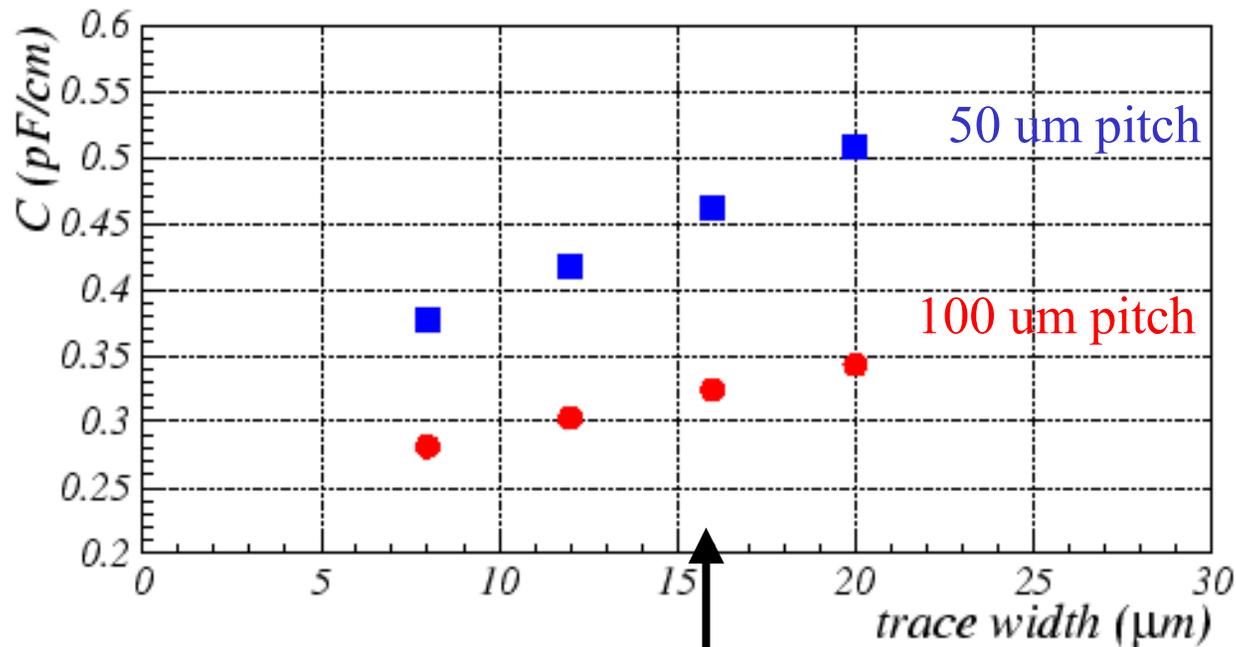


Acceptable cable capacitance is determined by noise performance

$S/N = 10$ after 15 fb⁻¹ $\Rightarrow C_{cable} < 0.55$ pF/cm for 42 cm long cable

L0 Analog Cable Capacitance

- FE calculations (ANSYS) agree with measurements within 10%
- 50 μm thick substrate with $\epsilon_r = 3.5$
- Settled on 91 μm pitch and 16 μm trace width



16 μm \Rightarrow 0.32 pF/cm

Analog Flex Cables

- Dyconex

- Second prototype run (March 2002)

- ❖ pitch 91 μm , trace width 16 μm
- ❖ Used regular etching technology
- ❖ 15 mechanical grade cables
- ❖ 12 good cables
- ❖ More cables ready in April

- Results on the 12 good cables:

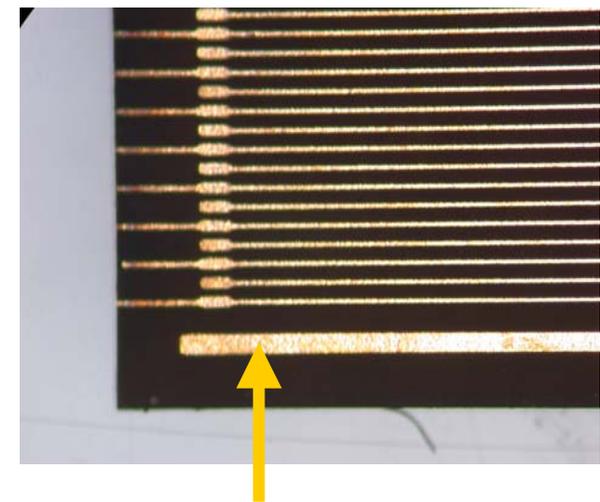
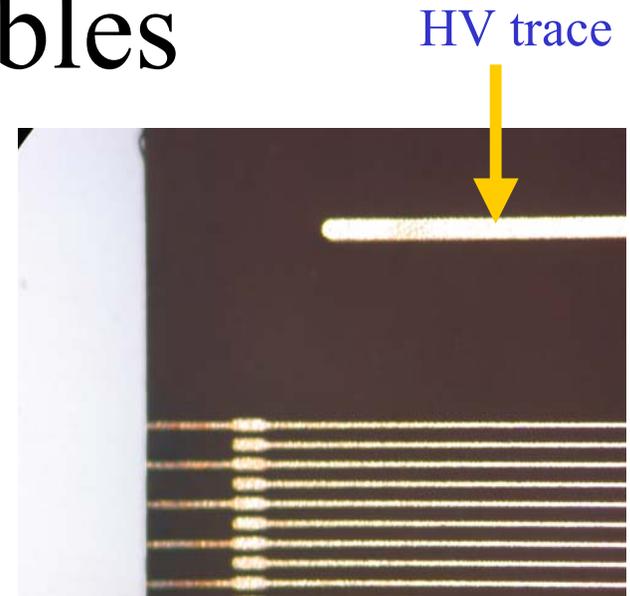
- ❖ Good quality of imaging
- ❖ Allow one open trace out of 129

Open traces	0	1	2	>2
cables	6	4	2	0

- ❖ Checked trace width : 9-14 μm
- ❖ Capacitance, resistance measurements under way

- Compunetics

- Run2A SMT HDI & CFT VLPC cable vendor
- Placed order for 20 cables, same design
 - ❖ Ready in May



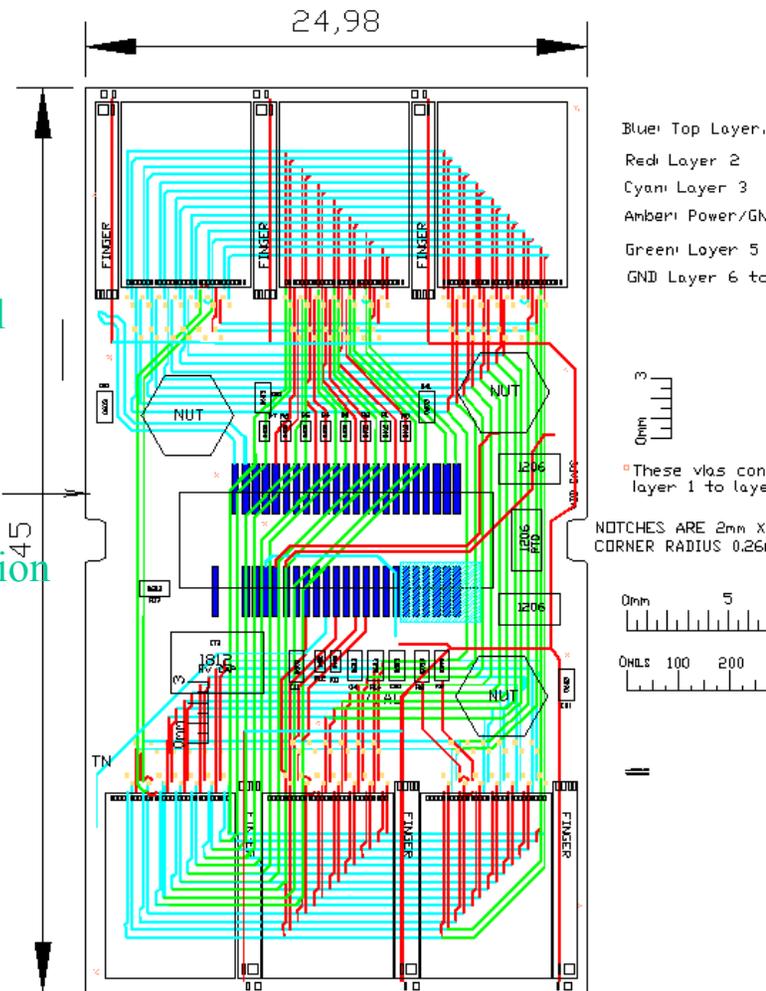
GND trace

Hybrids

- Based on Beryllia ceramic, 0.38 mm thick
 - Minimize material
 - Good heat conductor
 - Established technique
- Multilayer structure on the substrate
 - six Au layers
 - ❖ GND & power planes, 4 um thick
 - ❖ Traces, 8 um thick, 100 um wide
 - five 40 um dielectric layers, total thickness 0.8 mm
 - Two technologies for vias in dielectric
 - ❖ Etching (Fodel dielectric), min via size 4 mils
 - ❖ Screen printing, min via size 8 mils
 - Screen printing is our baseline
 - ❖ Cost effective
 - ❖ More vendors capable to screen print on BeO
 - CPT, Oceanside CA - used by CDF
 - ALDEN, Alden NY
 - AMITRON, North Andover MA
 - Hybrid Microcircuits, Blue Earth MI – used by CLEO

Hybrids

- Four types of hybrids
 - Layer 0 : 2 chips
 - Layer 1 : 6 chips, double-ended
 - Layers 2-5 : 10 chips, double-ended
 - ❖ Axial
 - ❖ Stereo, different width, electrically identical to axial
- For all types of hybrids
 - ~10 mil spacing between vias
 - 50 pin AVX 5046 connector, 3 mm high
 - ❖ Allows for easy testing during all phases of production and assembly
 - ❖ Used by CDF for Run 2A SVX
 - Fingerless design
 - bypass capacitors, termination resistors
 - temperature sensor
 - HV routed to side pin with 4 neighbors removed, tested to 1600 V
 - Reserved space (“nuts”) for assembling purposes

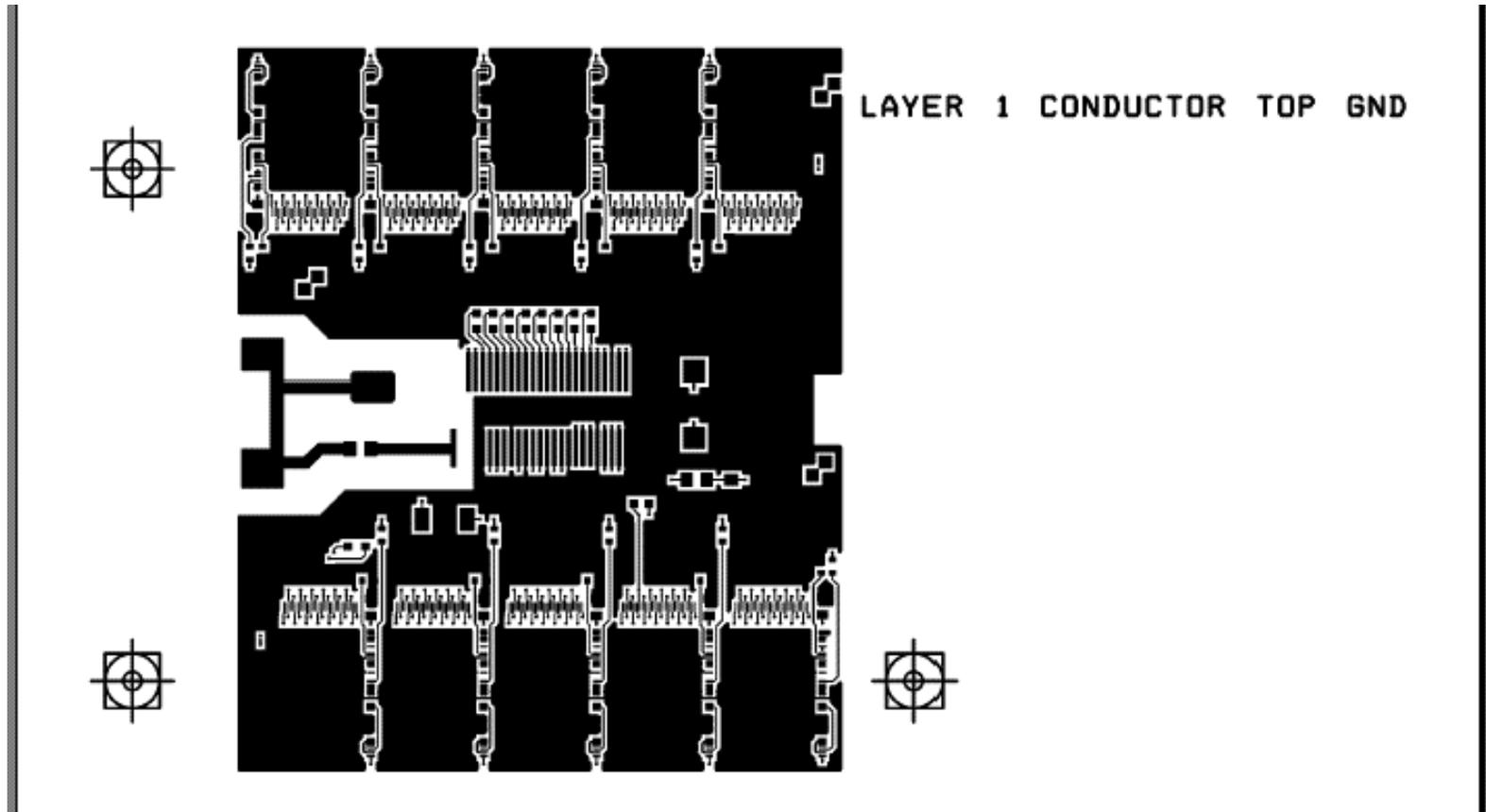


Layer 1 hybrid layout

Hybrids

Layers 2-5 10-chip hybrid :

Design similar to Layer 1 6-chip hybrid



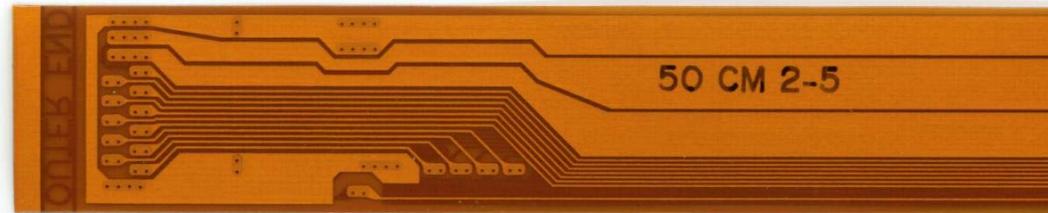
Hybrids

- Ordered prototypes for Layer 1, CPT Oceanside CA
 - 18 hybrids are ready, will be shipped shortly
 - Prepared to perform tests
 - ❖ Mechanical (thickness, flatness, dimensions, gluing)
 - ❖ Stuffing and bonding
 - ❖ Electrical
 - ❖ Probing to validate the layout and quality
 - ❖ Other tests when SVX4 are available
- L2A and L2S hybrids will be ordered in April 2002
 - L2A layout is ready, L2S layout ready this week
 - Two vendors : CPT and AMITRON
 - Two hybrids (one L2A & L2S) per BeO substrate
 - Prototypes ready in July

Digital Jumper Cable

Hybrid - **Jumper Cable** - Junction Card - Twisted Pair Cable – Adapter Card

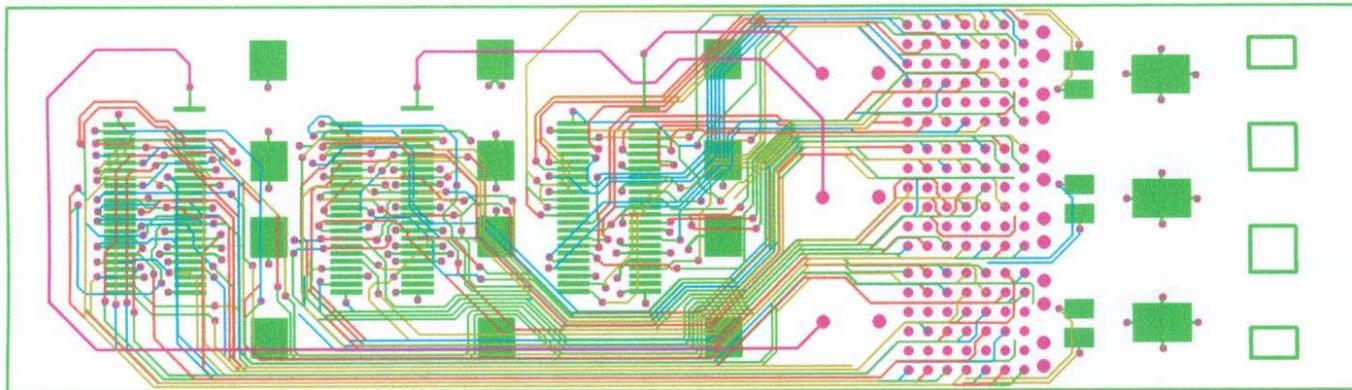
- Same design for all layers
 - 10-12 different lengths, max length ~ 1 m
 - Kapton substrate
 - HV on the same cable
 - AVX 50-pin connector on both sides
- Prototypes ordered in January
 - From Honeywell (Run2A low mass cables)
 - Back in March, look good
 - Electrical tests proceeding
- Second vendor :Basic Electronics
 - Placing order



Junction Card

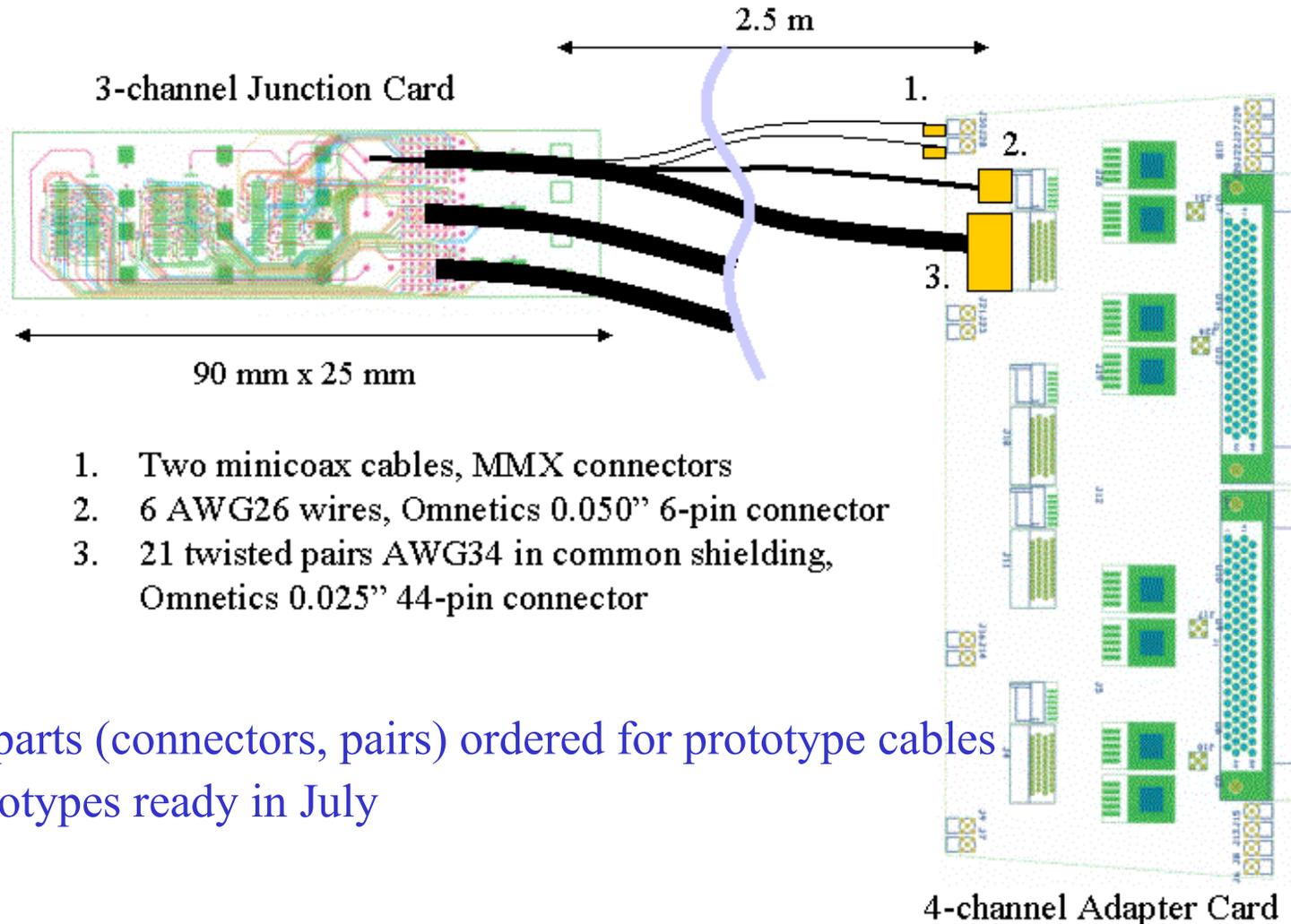
Hybrid - Jumper Cable - **Junction Card** - Twisted Pair Cable – Adapter Card

- L0-1 : 3 hybrids → junction card
L2-5 : 2 hybrids → junction card
 - 50-pin AVX connectors,
three(two) receptacles heights: 3.0,
3.5, (3.0) mm
 - Twisted pairs are soldered to JC,
cards are extensions of cable bundles
 - Dimensions 97 (70) mm x 25 mm
- prototypes ordered in April
 - ready for testing in May



Twisted Pair Cable

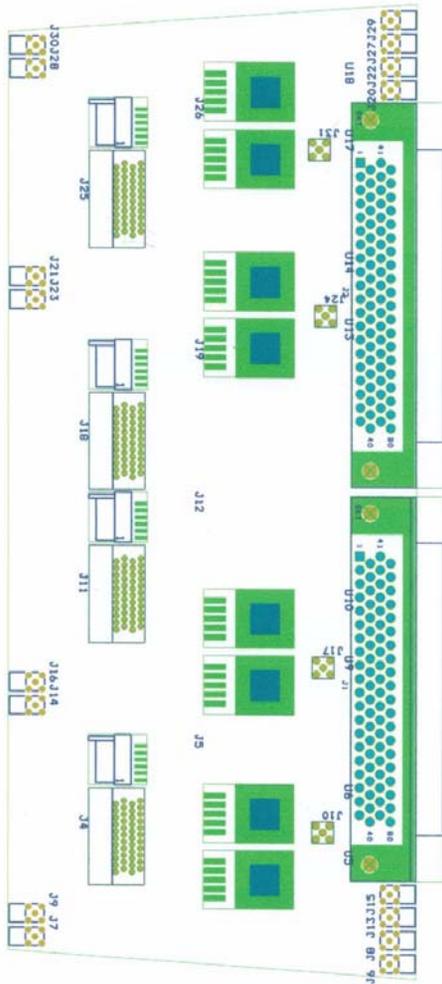
Hybrid - Jumper Cable - Junction Card - **Twisted Pair Cable** – Adapter Card



- All parts (connectors, pairs) ordered for prototype cables
- Prototypes ready in July

Adapter Card

Hybrid - Jumper Cable - Junction Card - Twisted Pair Cable – **Adapter Card**



- Adapter Card is active :
 - Two voltage regulators per hybrid: analog and digital voltages
 - Differential-to-Single-Ended 2.5-to-5 V translation for SVX4 Data
 - 5-to-2.5 V translation for SVX4 Controls
 - Routing of Clock and HV
- Three rings of Adapter Cards at two ends of calorimeter
 - Option A : 37 x 3 4-channel ACs
 - Option B : 34 x 3 4- and 6-channel ACs
- Design will be reviewed on April 22

Top view of 4-channel Adapter Card

Interface Board & Power Supplies

- Baseline : retain Run 2A IB's, use in full functionality
 - Signal regeneration and termination
 - LV distribution
 - LV voltage/current monitoring
 - HV distribution for L2-5 (< 300 V)
 - Hybrid Enable/Disable
 - Hybrid temperature monitoring
 - Current & temperature protection
- Will need small modifications of IB inputs.
- Note: Present IB fixes several SVX2 “features”
 - Assumption : SVX4 will not have new “features” which cannot be recovered with present IB
 - Otherwise will need new IB
- LV power supplies and Grounding issues are topics of April 22nd workshop

High Voltage

- Current caused by radiation damage
 - Assume 15 fb⁻¹, -10 deg C

Layer	Radius,mm	uA/strip	uA/hybrid	uA/stave	Hybrids/HV ch
0	18	1.2	310	NA	1
1	35	0.46	360	NA	1
2	54	0.28	530 max	1790	1
3	86	0.12	230 max	770	2
4	116	0.06	180 max	550	4

- Max current < 0.6 mA
- Total HV channel count of 492
- Will keep the present HV system : Bira 2000 V, 3.2 mA
- Currently have 10 crates, 440 HV channels (out of them 248 are positive)
- Will have 11 crates; 528 positive channels
 - ❖ Mexican collaborators (CINVESTAV) are buying the balance between Run2A and Run2B in 2002

Status

Component	Vendor	Design	First Prototype		Second Prototype	
			Ordered	Delivered	Ordered	Delivered
SVX4	TSCM	✓	✓			
Analogue Cable	Dycx	✓	✓	✓	✓	✓
	Comp	✓	✓			
L0 Hybrid		50%				
L1 Hybrid		✓	✓			
L2A Hybrid		✓				
L2S Hybrid		✓				
Digital Cable	Honey	✓	✓	✓		
	Basic	✓				
Junction Card		✓	✓	✓		
Twisted Pr. Cable		✓	✓			
Adapter Card		75%				
Test Stand Elctr.		✓				
High Voltage		✓				
Low Voltage		0%				

Performance issues

- Readout time is important issue in deadtime accounting

- Simulations :

- Two-jet events
- Run 2B GEANT
- Realistic clustering
- Neighbors and noise contribution

Layer	S/N	Max # strips	Readout Time, usec
0	8	95	3.8
1	15	85	3.4
2	15	70	2.8

- Maximum # of strips read out per cable
 - Allows for comparison between layers
- Readout time is comparable for first three layers
 - Assumes low S/N in Layer 0 after radiation damage
 - Justifies 2-chip readout for Layer 0
- Deadtime is still dominated by digitization and pipeline reset (~ 7.2 usec).
 - Unavoidable in D0 DAQ architecture
 - Total deadtime, ~ 11 - 12 usec, is acceptable.

Electronics & Readout in 2002

- Major milestones in 2002
 1. SVX4 tests
 - ❖ Bare chip tests
 - ❖ Hybrid & full chain tests
 2. L0 prototype with Analog cable
- Result : sign-off on all components for production
 - Alternative : going to production without full chain tests – increased risk for the project
- Risks & Worries
 - SVX4 second submission : chip on the critical path
 - ❖ Second submission is quite probable
 - ❖ Even partly functional chip (after 1st submission) may allow to perform a lot of critical tests
 - Expedient ordering of all prototype materials
 - ❖ a lot of requisitions
 - To reduce schedule risk will have second vendor for most items
 - Manpower
 - ❖ Good contributions from universities (KSU, KU)
 - ❖ So far Fermilab EE manpower is not adequate

Summary

- Have a baseline for Run 2B Readout
- Excellent progress last 4 months
- Detailed design exist for (almost) all components
- Moved on to prototyping
 - Have some prototypes in hand (L1 hybrid, Digital flex cable)
 - All prototype components for full readout chain test ready by September 2002
- SVX4 schedule and performance is crucial for the project
 - Testing effort very important
- Readout project could benefit from extra EE manpower