



DO RunIIB Trigger Upgrade

WBS 1.2

L2 managers:

Hal Evans, Columbia Univ.

Darien Wood, Northeastern Univ.



Outline

- Run IIa Trigger System
- Trigger Strategies for Run IIb
- Upgrade Design
 - ◆ Level 1
 - ▲ WBS 1.2.1: Calorimeter trigger
 - ▲ WBS 1.2.2: Calorimeter-track matching
 - ▲ WBS 1.2.3: Track trigger
 - ◆ Level 2
 - ▲ WBS 1.2.4: L2 Beta processors
 - ▲ WBS 1.2.5: Silicon Track Trigger upgrade
- Organization of Trigger Upgrades
- Cost and Schedule



The Run IIa Trigger System

Level-1

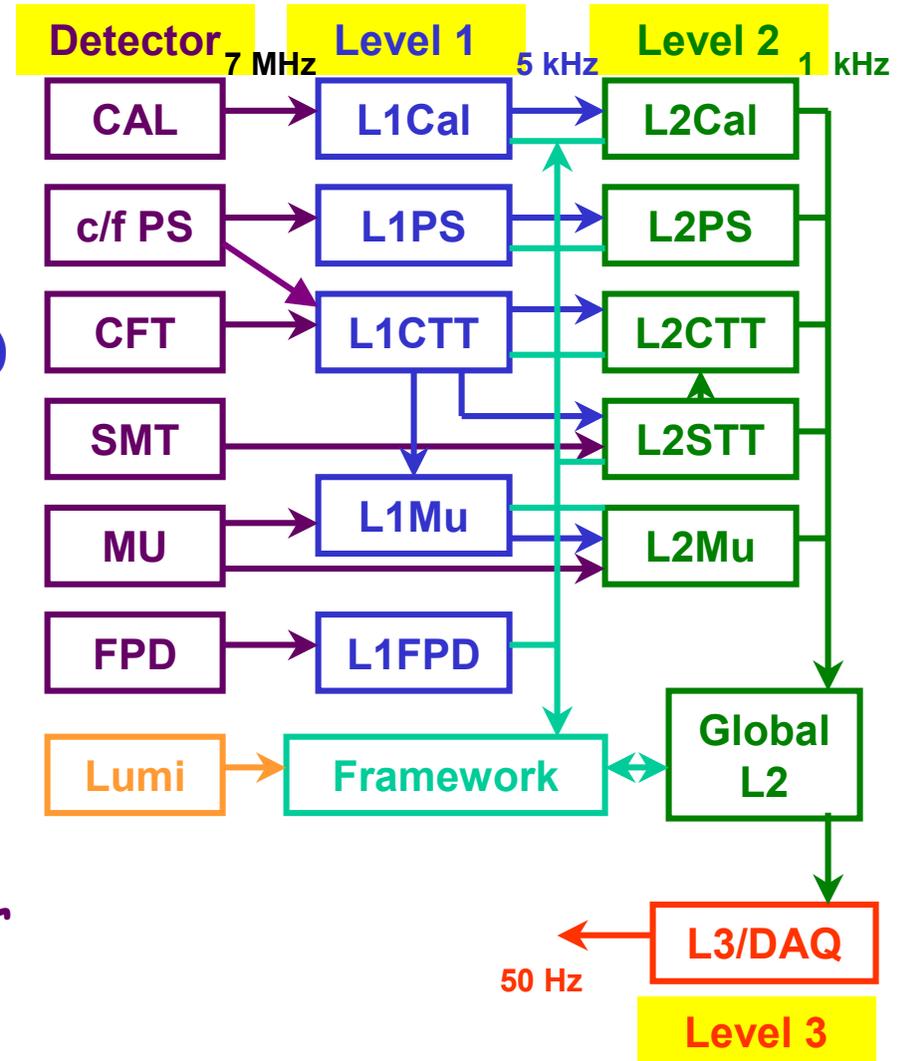
- ◆ Mainly single-detector-based
- ◆ Correlations
 - ▲ Cal-Trk: quadrant level
 - ▲ Mu-Trk: L1trk info → L1Mu
- ◆ **Out rate ~5 kHz** (r'dout time)

Level-2

- ◆ Calibrated data
- ◆ Extensive correlations
- ◆ Physics objects out (e, μ, τ, j, \dots)
- ◆ **Out rate < 1 kHz** (cal r'dout)

Interdependence

- ◆ High level of connectivity
- ◆ All elements must function for system to work





Run I Ib Trigger Priorities

- Main physics driver for Run I Ib: Higgs search
 - ◆ Need efficient triggers for Higgs production/decay in all major modes
 - ◆ Trigger objects:
 - ▲ Leptons
 - ▲ b-jets
 - ▲ taus
 - ▲ Missing E_T
- SUSY
 - ◆ Trigger objects
 - ▲ Leptons
 - ▲ Missing E_T
 - ▲ taus
- Top, W, Z
 - ◆ Trigger objects:
 - ▲ Leptons
 - ▲ Jets
 - ▲ Missing E_T
 - ◆ precision mass measurement to understand EWSB
 - ◆ Also important for background & calibration for Higgs search
- Other background/calibration channels (e.g. $Z \rightarrow b\bar{b}$)
- Some trigger load can be relieved by elimination of low-pt physics menu (lower energy QCD, b-physics, ...), but this is not sufficient.

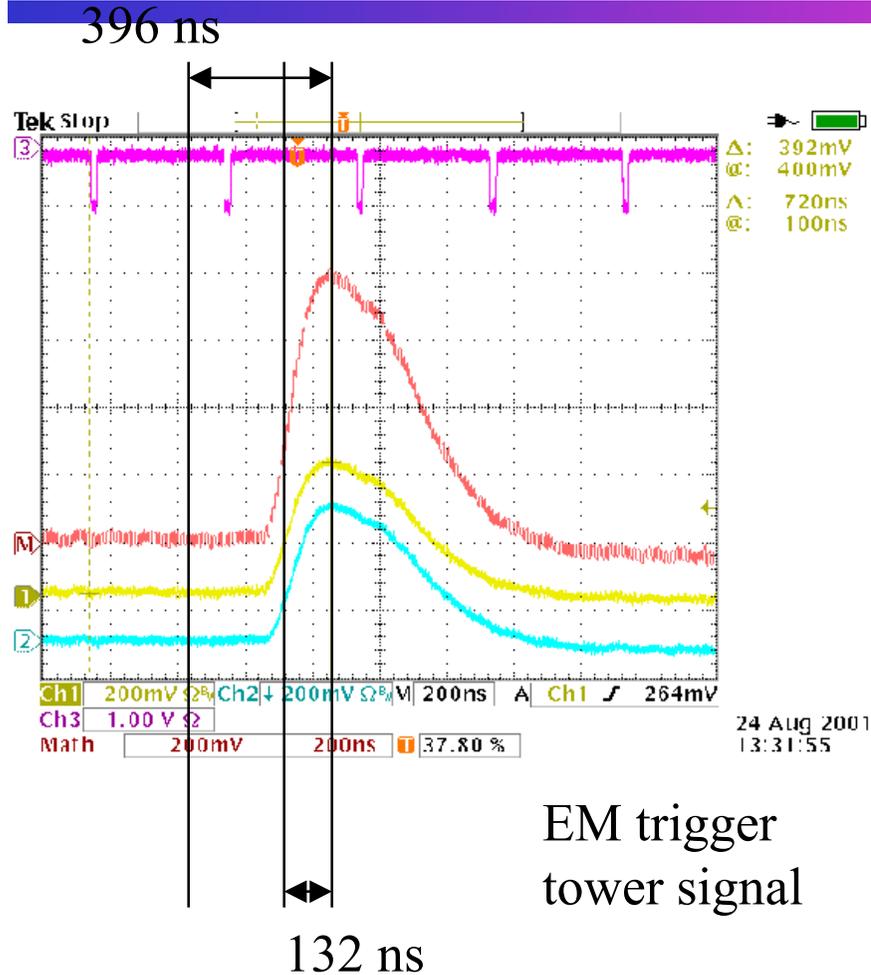


Strategies for Trigger Upgrades

- Increase trigger rejection at Level 1
 - ◆ L1 Calorimeter trigger upgrade to sharpen thresholds
 - ◆ L1 Tracking trigger upgrade to maintain rejection
 - ◆ Additional rejection from cal-track matching
- Combat backgrounds at Level 2
 - ◆ L2 Processor upgrades
 - ◆ Expand Silicon Track Trigger (STT) for new silicon detector geometry
- Upgrade/maintain DAQ/Online systems to support data collection through Run II (see talk from S. Fuess)



Calorimeter Trigger Upgrade

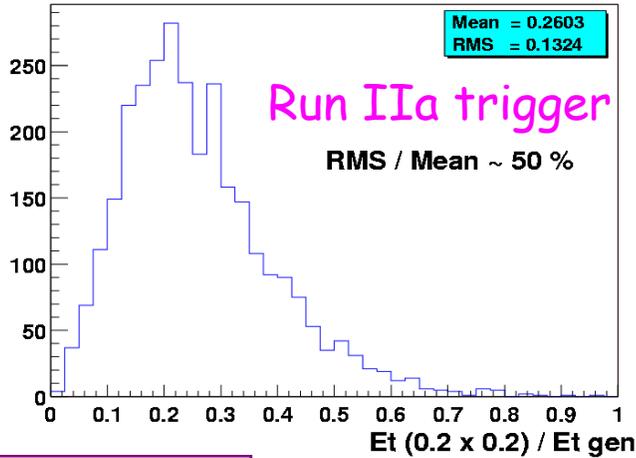


- Introduce digital filter on trigger tower signals
- Suppress pile-up effects
- Improve energy resolution
- Avoid triggering on wrong crossing (signal rise time > 132 ns)
 - ◆ Sample at peak to avoid timing variations
 - ◆ Previous crossing will often be above threshold
 - ◆ It would be the highest energy events (most interesting) which are mis-assigned

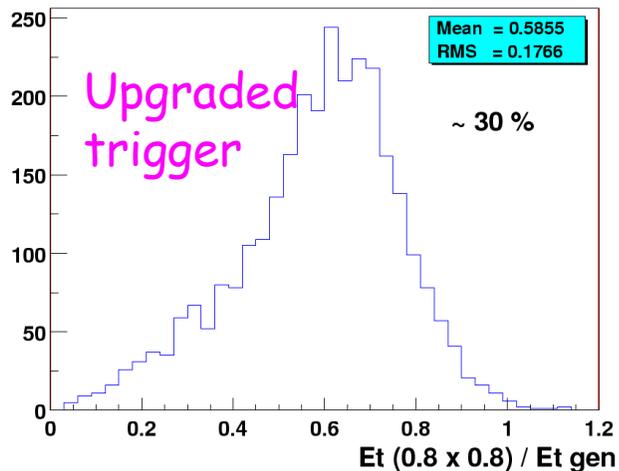
WBS 1.2.1: L3 managers: M. Abolins (MSU), H. Evans (Columbia), P. LeDu (Saclay)



Calorimeter Trigger Upgrade



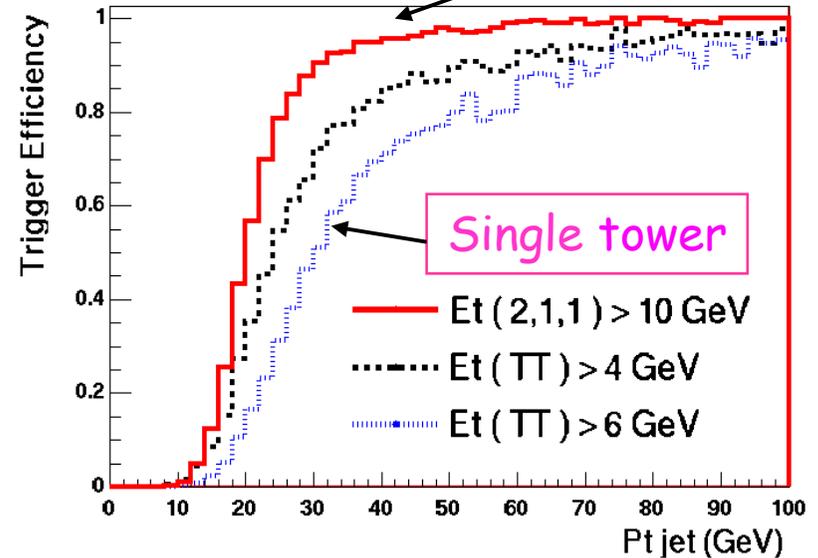
40 GeV jets



- Sharpen thresholds by introducing EM, Jet clustering

Large window

Turn-on curves : 2,1,1 algo vs current trigger

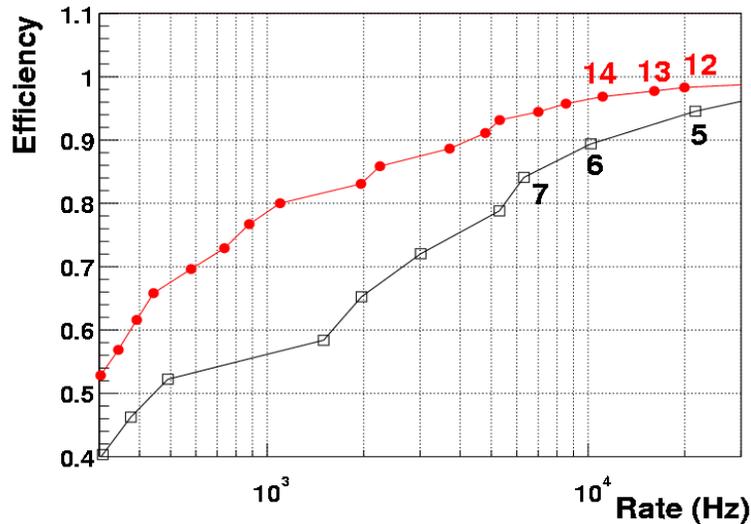




Calorimeter Trigger Upgrade

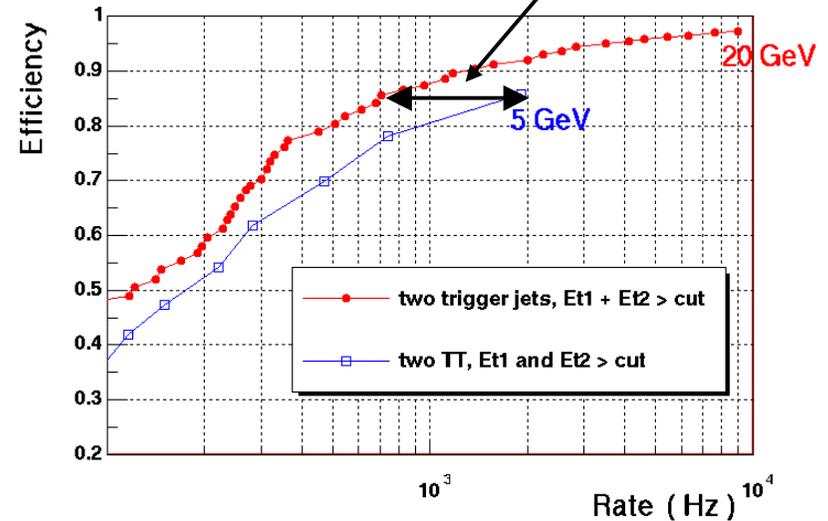
- Rate improvements from cluster thresholds vs. tower thresholds

Selectivity for $P_{\text{that}} > 40 \text{ GeV}$, $\text{mb} = 5$



Single jet

Selectivity on $ZH \rightarrow \nu\nu + \text{jets}$ ($\text{mb}=7.5$)

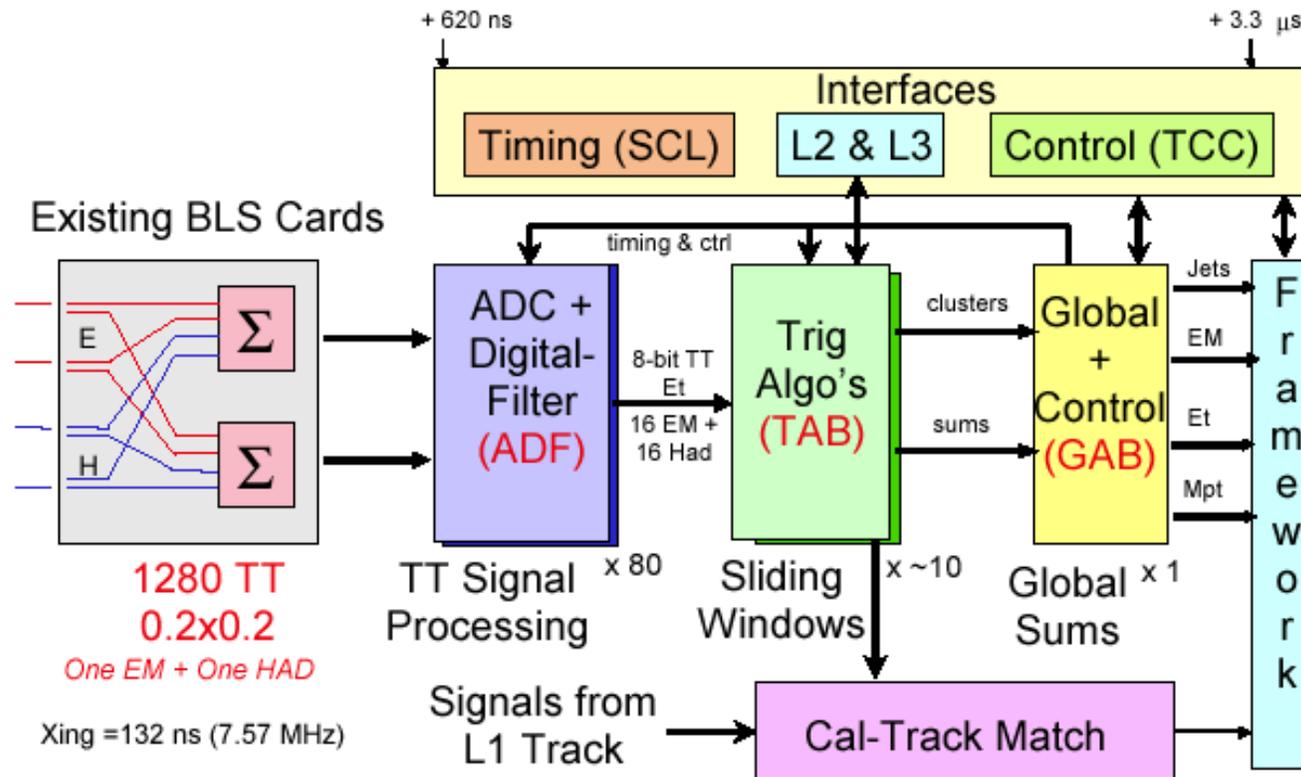


$$ZH \rightarrow \nu\bar{\nu}b\bar{b}$$



Calorimeter Trigger Upgrade

- Clustering algorithm gets implemented in FPGA's
- Similar to ATLAS sliding-window algorithm





L1Cal-Track Trigger

- Exploit new L1Cal and new L1CTT triggers
- Improve Run IIa ϕ matching granularity x8
- Needed in triggers for Higgs searches
 - ◆ electrons in WH and $H \rightarrow W^*W$ modes
 - ◆ taus in $H \rightarrow \tau\tau$ and $H^+ \rightarrow \tau\nu$
- Fake EM rejection is improved by $\sim x2$
- Fake τ rejection is improved by $\sim x10$

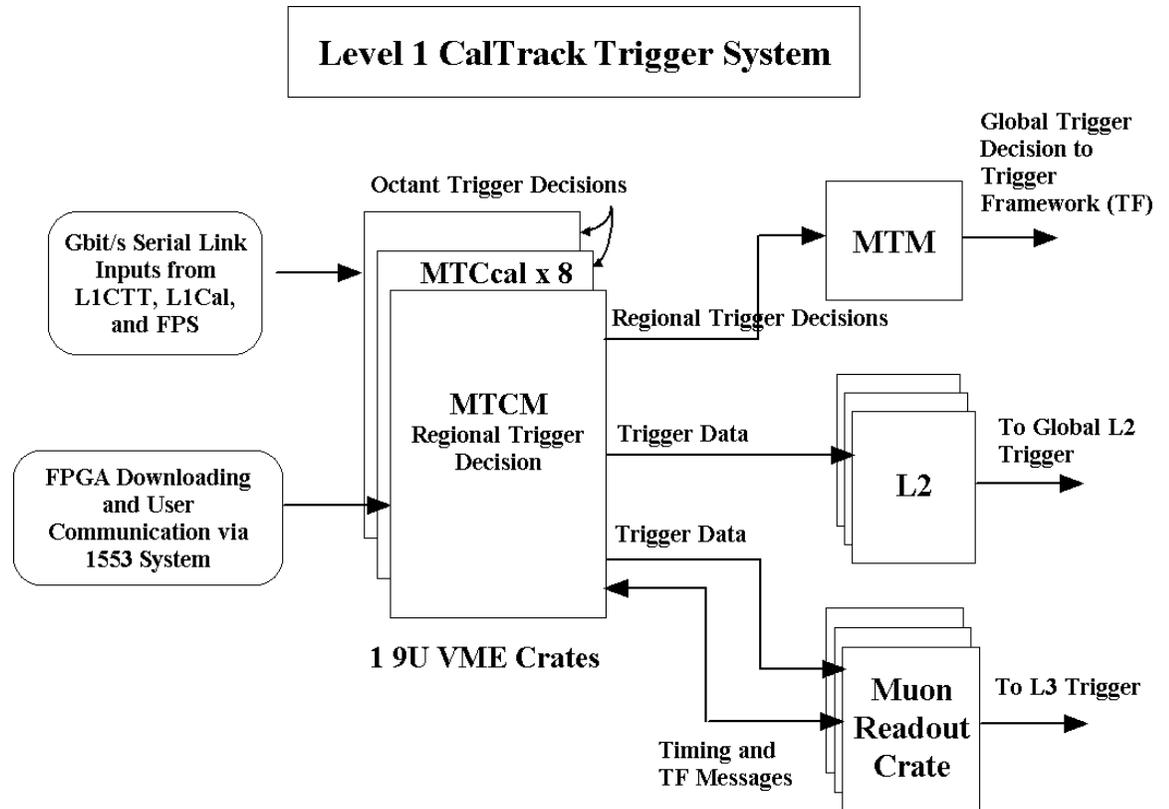


WBS 1.2.2: L3 manager: K. Johns (Arizona)



L1 Cal-track matching

- Can use same hardware design (Muon Trigger Cards) that presently does Level1 muon-CTT match (with minor modifications)
- Modest cost and effort



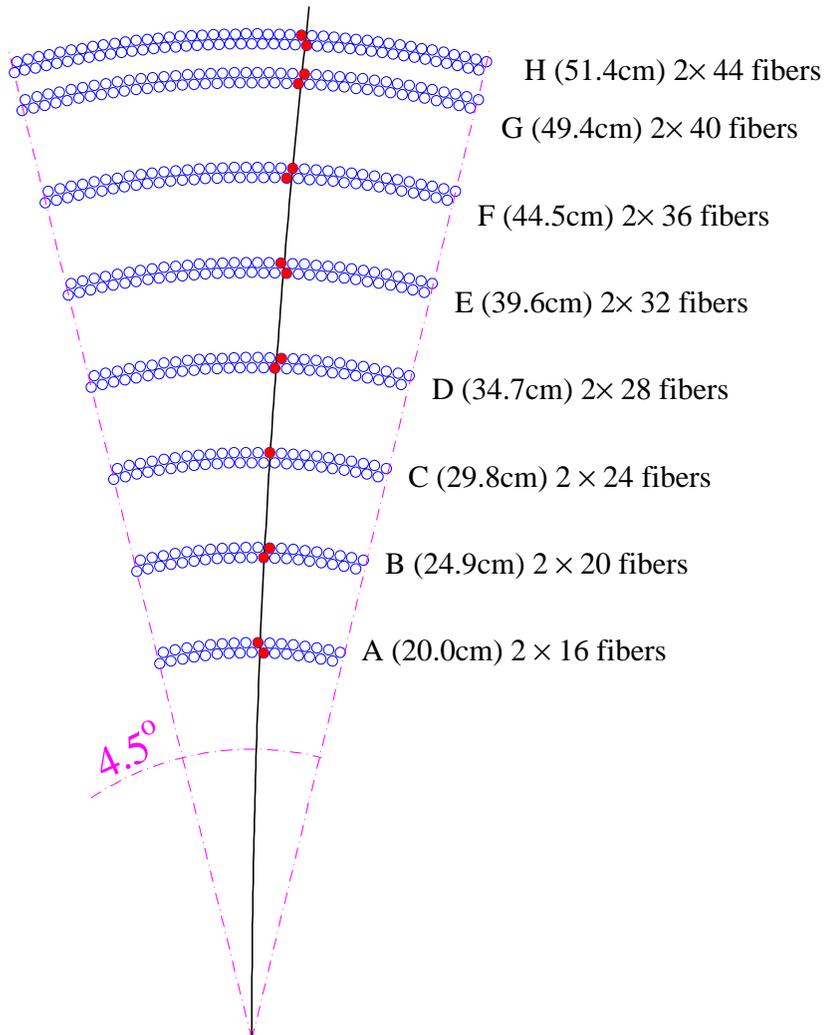


L1Cal-Track Latency

ELEMENT	Δ TIME (ns)	TOTAL TIME (ns)
BC to ADF	650	650
ADF processing	1147	1797
TAB processing	374	2171
L1CFT processing	1592	
MTCxx processing	729	2900
MTM processing and transfer	589	3489
Run IIb L1 decision time		4092
Difference		-603



Level 1 Central Tracking Trigger (CTT)

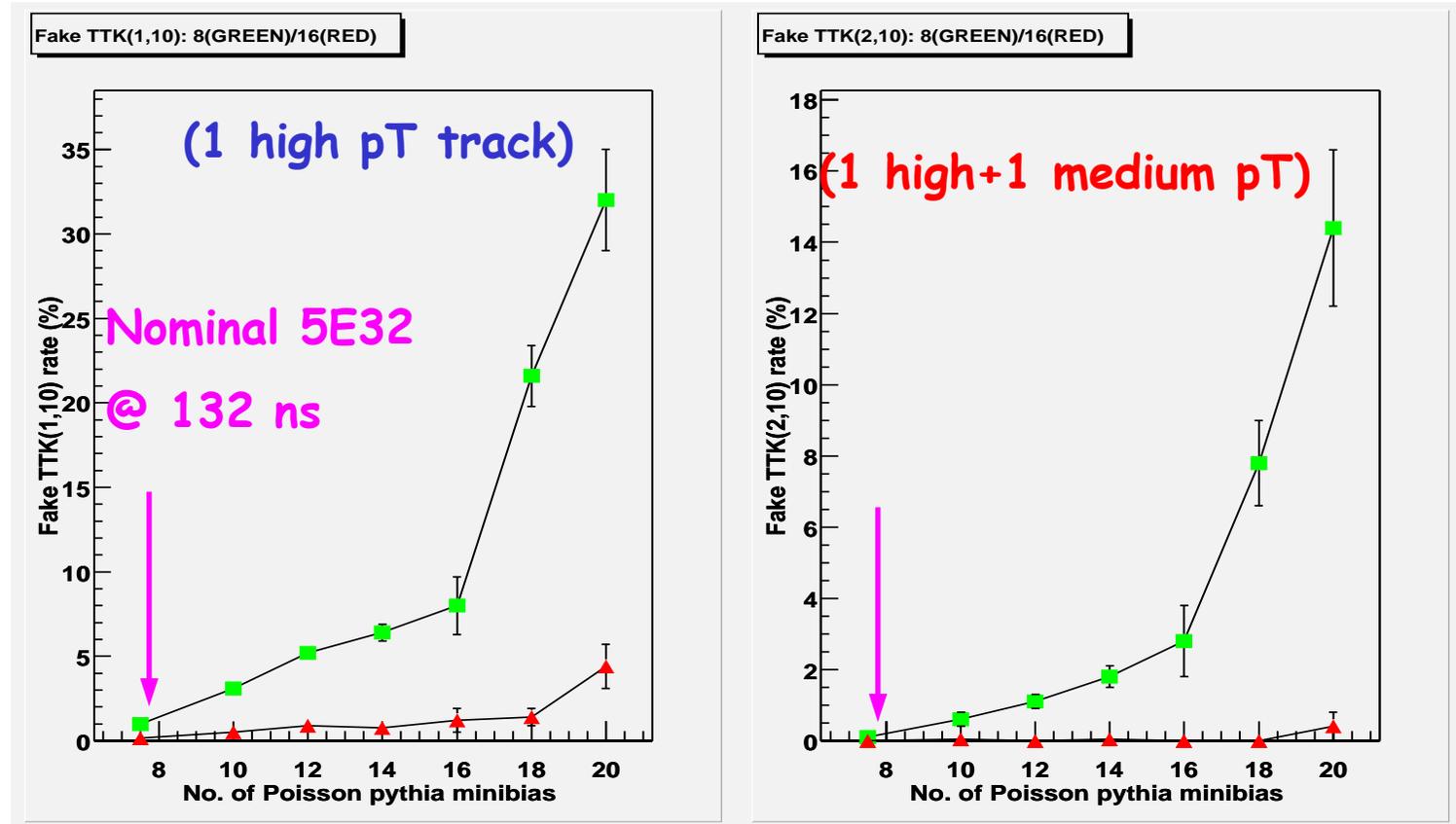


- Level 1 Central Track Trigger (CTT) essential for electrons, muons, taus ($WH \rightarrow l\nu jj$)
- Tracking trigger rates sensitive to occupancy
- Upgrade strategy:
 - ◆ Narrow tracker roads by using individual fiber hits (singlets) rather than pairing adjacent fibers (doublets)
 - ◆ Cal-track matching

WBS 1.2.3: L3 manager: M. Narain (Boston U.)



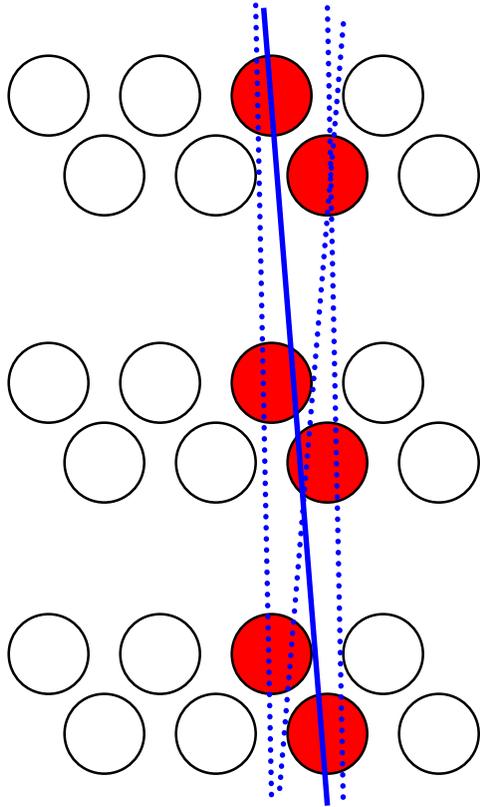
Run IIa at high luminosity



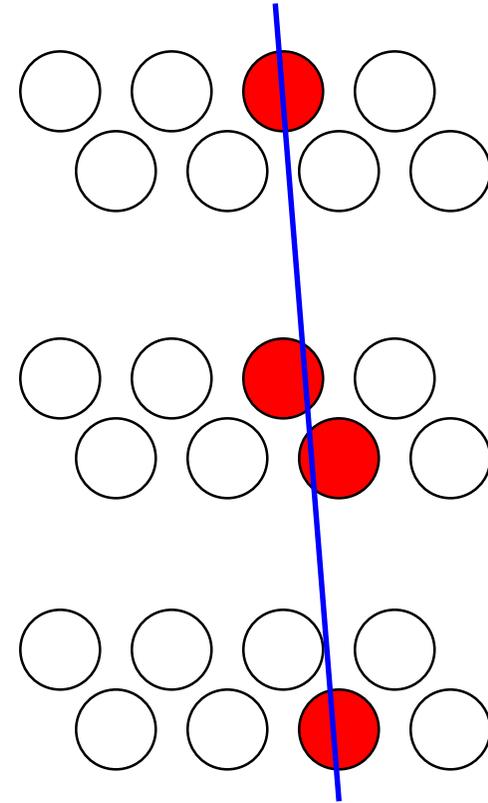
- Even at modest occupancies, the high- p_T single track trigger would fire at $>50\text{kHz}$



Run IIb L1CTT: Granularity



Run IIa



Run IIb

- Use full fiber resolution to restrict roads



L1CTT Algorithm Results

- With baseline version of new L1CTT:

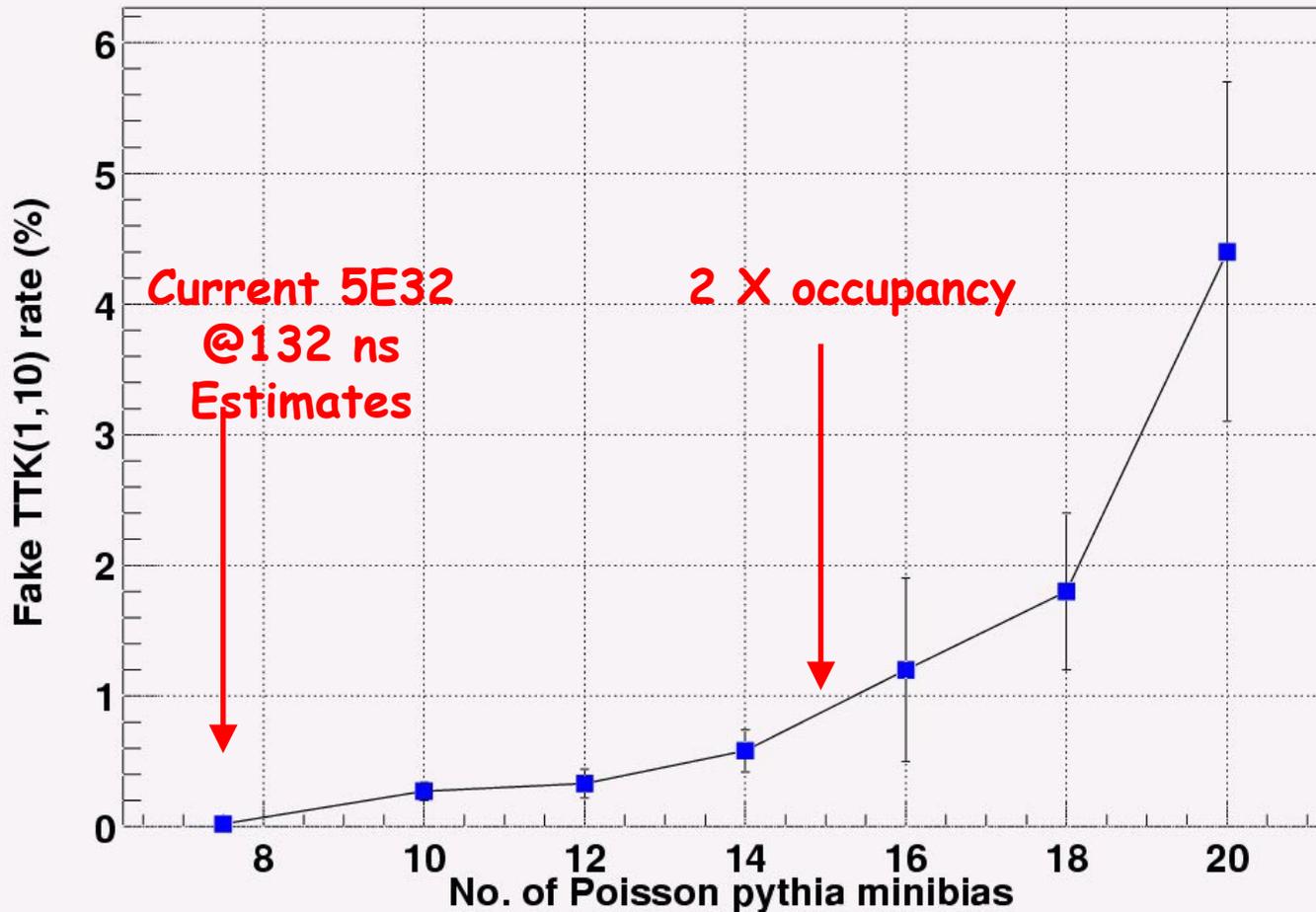
Scheme/ p_T range	Tracking Efficiency (%)	Rate of Fake Tracks (% events)	Resources
ABCDEFGH (RunIIa) ($p_T > 10$ GeV)	96.9	1.02 ± 0.10	11k X 8
abcdefgh ($p_T > 10$ GeV)	98.03 ± 0.22	0.056 ± 0.009	9.4k X 16
abcdEFGH (5 GeV $< p_T < 10$ GeV)	99.20 ± 0.14	0.89 ± 0.11	8.9k X 12
abcdEFGH (3 GeV $< p_T < 5$ GeV)	98.40 ± 0.20	4.5 ± 0.2	11.3k X 12
abcdEFGH (1.5 GeV $< p_T < 3$ GeV)	95.15 ± 0.32	25.4 ± 0.2	15.5k X 12



Performance vs. Luminosity

- Rate of fake high- p_T tracks vs. Luminosity:

v5acc200rr, with ADC \geq 25,50

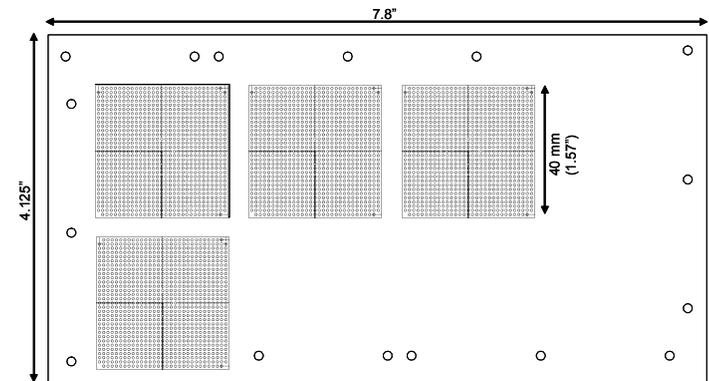
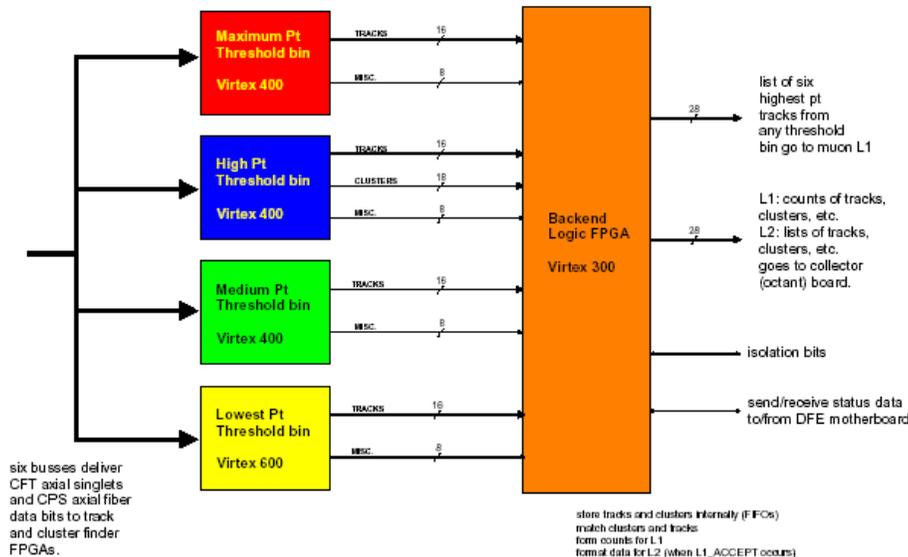




L1 CTT Implementation

- Digital Front End Axial (DFEA) daughter cards get replaced with new layout with larger FPGA's (Xilinx Virtex-II XV2C6000)
- Baseline algorithms compiled; occupy ~40% of the resources of the XV2C6000's.

CFT/CPS AXIAL Trigger Daughter Board Dataflow



DFEA layout with new FPGA footprints



Comments on L1CTT Results

- New equations yield better efficiency, factor of 5-20 fewer fakes at high p_T
 - ◆ lack of explicit fiber vetos renders efficiency luminosity-independent
- x2-x3 Run IIa L1CTT resources required
- Use of doublets at lower p_T reflects balance between resources and physics:
 - ◆ number of equations increase with $1/p_T$
 - ◆ multiple scattering makes singlets inefficient
 - ◆ fine granularity in inner layers with more occup.



Additional features

- Muon triggers - No change needed to muon trigger system, but most muon triggers would gain needed rejection from upgrade of the CTT trigger that feeds muon L1. Higher p_T threshold possible.
- Global calorimeter sums - better missing E_T with incorporation of intercryostat detector and massless gaps
- EM shape and isolation - these cuts can be implemented in Level 1 after cluster finding, giving an additional factor of 2 rejection for electron & photon triggers
- Topology - flexibility to require acoplanar jets, etc.
- Flexibility: New clustering and tracking algorithms can be implemented with FPGA downloads



Run I Ib Level 1 Trigger rates with upgrade

- Run I Ib: $\Delta t = 132 \text{ ns}$, $L = 5 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$

Trigger	Rate (no upg.)	Cal upg.	Trk upg	Cal+ trkmtch	Cal +track	Cal + trk + trkmtch
EM Trigger (1 EM tower > 10 GeV)	9 kHz	4 kHz	3 kHz	1.5 kHz	1 kHz	0.5 kHz
Jet Trigger (2 trigger towers > 4 GeV)	2 kHz	0.5 kHz	2 kHz	0.5 kHz	0.5 kHz	0.5 kHz
Track Trigger (2 trk > 10, 5 GeV, iso, EM)	60 kHz	60 kHz	7 kHz	7 kHz	7 kHz	0.7 kHz
Muon Trigger (muon > 10 GeV)	6 kHz	6 kHz	2 kHz	6 kHz	2 kHz	2 kHz
Sum	77 kHz	70 kHz	14 kHz	15 kHz	10 kHz	3.7 kHz
Sum w/o 2-trk	17 kHz	10 kHz	7 kHz	8 kHz	3.5 kHz	3.0 kHz

Total rate into Level 2 limited to 5 kHz



Level 2 Trigger

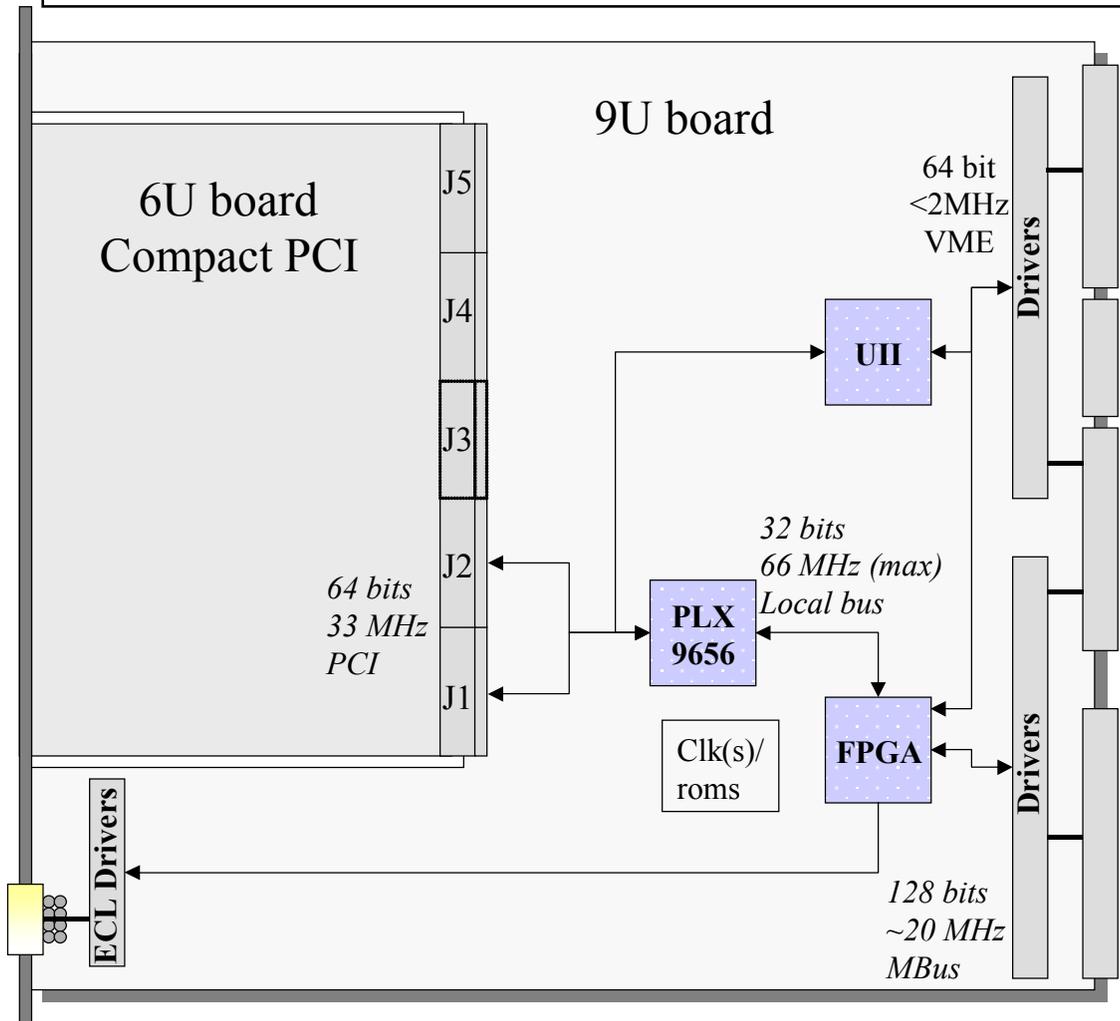
- Level 2 β processors
 - ◆ Add 12 additional processors for higher RunIIB luminosity
 - ◆ This additional processing power (X 2-3 increase over RunIIa) is needed to take advantage of the increased power at Level 1
- Silicon Track Trigger (STT)
 - ◆ Run IIa STT available Fall 2002
 - ◆ Vital for triggering on b-quarks
 - ▲ $ZH \rightarrow \nu\nu b\bar{b}$
 - ▲ $Z \rightarrow b\bar{b}$
 - b-jet energy scale
 - di-b-jet mass resolution
 - ◆ Improves track trigger
 - ▲ Sharper p_T turn-on
 - ▲ Reduced fake rate
 - ◆ Run IIB STT upgrade needed to accommodate design of new silicon detector



L2βeta Block Diagram

WBS 1.2.4: L3 manager: R. Hirosky (Virginia)

- PIII Compact PCI card
- 9U card with “custom” devices (3 BGA’s)
- Universe Chip VME interface
- commercial 64-bit PCI interface chip
- MBus and other logic in FPGA





L2βeta

Examples of upgraded processing:

- Add vertex information to sharpen calorimeter triggers (30-60%) rate reduction for jet triggers (Eta dependent) with $\sim 10\text{cm}$ vertex resolution.
- Multi-track displaced vertices
- Sharpen calorimeter resolutions through application of improved calibrations at L2. Current processors would take 35-70 μs to processing time complete this task.
- Develop NN scheme for improved Tau recognition, etc
- Trigger branching at L2 Global

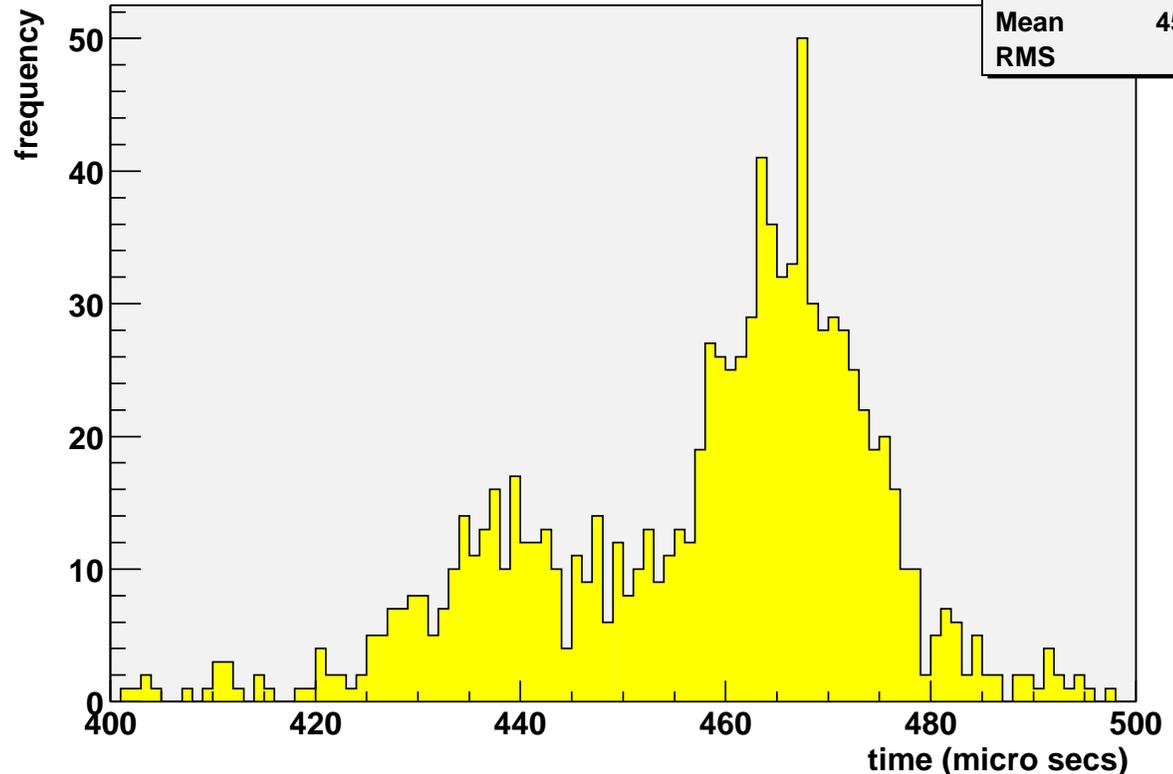


L2 β eta

Timing for track-based vertex finder in L3 using 1.5GHz CPU

Such algorithms will be accessible at L2 as CPU performance increases and by parallelizing work between nodes...

Timing for track based vertexing



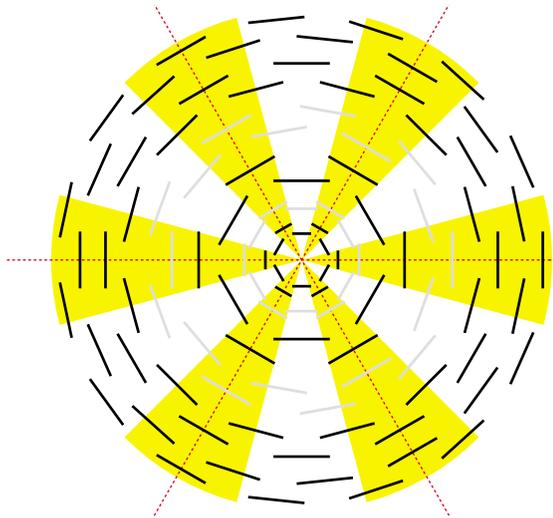


Silicon Track Trigger for Run IIb

- **SMT detector replacement: 6 axial barrel layers**
 - ◆ **Modest STT upgrade (5-layer readout) requires small quantity of same boards that are used in Run IIa. This is now the baseline design.**
 - ◆ **The full 6-layer implementation is not being pursued in order to reduce cost**

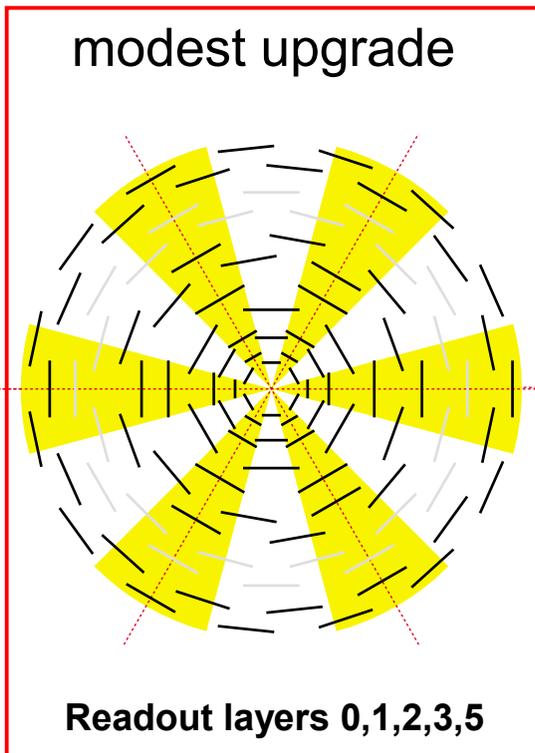
WBS 1.2.5: L3 manager: U. Heintz (Boston U.)

no upgrade



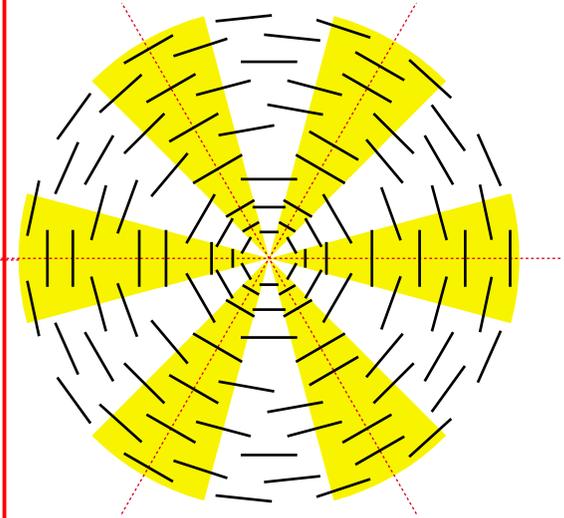
Readout layers 0,2,4,5
Use existing Run IIa hardware

modest upgrade



Readout layers 0,1,2,3,5

full upgrade

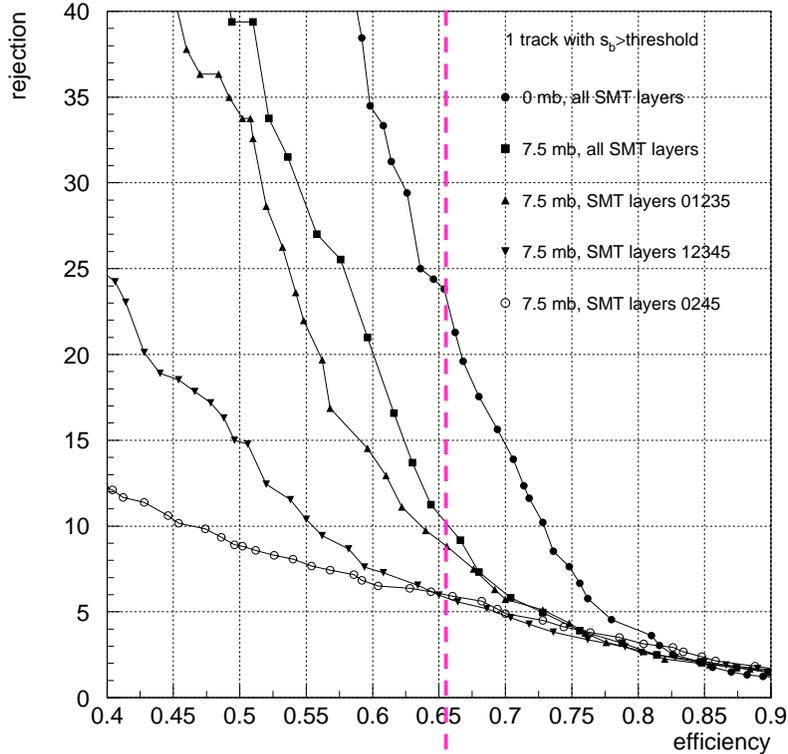


Readout all layers (0-5)



L2 STT Layer Study

$$WH \rightarrow \mu\nu b\bar{b}$$



65%

SMT layers used	N_{mb}	rejection for 65% efficiency
012345	0	22
012345	7.5	11
01235	7.5	9
12345	7.5	6
0245	7.5	6



Rejecting at Level 2

- RunIIB: $\Delta t=132\text{ns}$, $L=5 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1}$

Trigger	Example Physics Channel	Rate (no upg.)	Rate (L1 upgrade)	L2 tools
EM Trigger (1 EM tower > 10 GeV)	$W \rightarrow e\nu$	9 kHz	0.5 kHz	STT (trk)
Jet Trigger (2 trigger towers > 4 GeV)	$ZH \rightarrow \nu\bar{\nu}b\bar{b}$	2 kHz	0.5 kHz	STT (b-tagging), z-vertex (jet thresh)
Track Trigger (2 trk > 10, 5 GeV, iso, EM)	$H \rightarrow \tau\tau$	60 kHz	0.7 kHz	STT (trk)
Muon Trigger (muon > 10 GeV)	$W \rightarrow \mu\nu$	6 kHz	2 kHz	STT (trk), muon fits
SUM		77 kHz	3.7 kHz	

STT provides tracking rejection at level 2:

- Sharper momentum threshold
- Reduction of fake tracks



Trigger upgrade: Limited scope

- Studied and eliminated several upgrade options in favor of lower schedule-risk and/or cost:
 - ◆ Level 1 stereo tracking
 - ◆ Preshower as 9th tracking layer
 - ◆ Finer granularity of calorimeter towers (0.1x0.2)
 - ◆ 6-layer Silicon Track Trigger
- Use existing hardware (or minor modifications thereof) for new applications
 - ◆ Muon Trigger Cards for calorimeter-track matching
 - ◆ Existing DFE motherboards with daughter board replacement for tracking upgrade
 - ◆ Reuse L2Beta interface boards
 - ◆ Increase RunIIa STT production order to accommodate upgrade



Trigger Upgrade Project

- **Summer 2001:** DØ Trigger Task force studies upgrade options for trigger
- **October 2001:** Conceptual Design Report for trigger upgrade presented to the Fermilab PAC
- **December 2001:** Reviewed by Director's Technical Review Committee.
- **Jan 2002:** MRI proposal submitted for trigger upgrade
 - ◆ \$2.6 M requested (\$2.0 M from NSF)



Trigger Upgrade Project (cont.)

- **March 2002:** All WBS Level 3 project managers identified
- **April 2002:** Technical design report draft, cost estimate, resource-loaded schedule prepared for Director's Review Committee.
- **April 2002:** PAC review and Director's Review
- **July 2002:** PAC gives Stage I approval (with requests for additional studies & specification)
- **July 2002:** Trigger MRI awarded by NSF
 - ◆ \$446k + \$113k matching for L1 tracking subproject
 - ◆ Complements ~\$400k Saclay in-kind contribution for L1cal
- **August 2002:** TDR substantially revised to reflect significant process in developing detailed design.



Trigger Upgrade Project

Sub-project	Institution(s)
Calorimeter: ADF	Saclay, MSU
Calorimeter: TAB	Columbia
Track trigger	Boston U., FNAL
Cal-Track match	U. of Arizona
Simulation & algorithms	Notre Dame, Saclay, Kansas, Manchester, Brown
Online software & integration	MSU, Northeastern, FSU, Langston
Level 2 β	Orsay, Virginia, MSU
STT upgrade	Boston, Columbia, Stony Brook, FSU

- Strong, active institutions
- Largely University-driven
- Combination of RunIIa experience and new ideas

- Engineering, technical and physicist manpower identified for delivering upgraded trigger
- Other institutions expressing interest



Trigger Upgrade Project

WBS 1.2: Trigger Upgrade

H. Evans (Columbia), D. Wood (Northeastern)

WBS 1.2.1: Level 1 Calorimeter

M. Abolins (MSU), H. Evans (Columbia), P. LeDu (Saclay)

WBS 1.2.2: Level 1 Cal-track match

K. Johns (Arizona)

WBS 1.2.3: Level 1 Tracking

N. Narain (Boston)

WBS 1.2.4: Level 2 Beta upgrade

R. Hirosky (Virginia)

WBS 1.2.5: Level 2 STT upgrade

U. Heintz (Boston)

WBS 1.2.6: Trigger Simulation

M. Hildreth (ND), E. Perez (Saclay)



M&S Cost Estimates (\$k)

(FY02 k\$, not including FNAL labor, nor G&A)

project	Total M&S	Contingency	Total M&S+ contingency
WBS 1.2.1: L1 calorimeter	933	43%	1,333
WBS 1.2.2: L1 cal-track match	197	31%	257
WBS 1.2.3: L1 tracking	774	52%	1,181
WBS 1.2.4: L2 beta	49	30%	64
WBS 1.2.5: L2 STT	230	43%	329

ID	WBS	Task Name	M&S Cost \$	M&S Cont \$	FNAL Labor Cost \$	Labor Cont \$	Total Cost
1	1.2	Run IIB Trigger Upgrade	\$2,189,008.40	\$984,205.06	\$71,039.97	\$20,820.00	\$2,260,048.37
2	1.2.1	Level 1 Calorimeter Trigger	\$933,400.10	\$399,271.88	\$4,799.96	\$0.00	\$938,200.06
93	1.2.2	Level 1 Calorimeter Track Matching	\$196,702.84	\$60,511.85	\$19,200.00	\$9,600.00	\$215,902.84
140	1.2.3	Level 1 Tracking	\$774,160.47	\$407,362.58	\$44,880.00	\$11,220.00	\$819,040.47
197	1.2.4	Level 2 Beta Processor	\$49,450.00	\$14,860.00	\$0.00	\$0.00	\$49,450.00
231	1.2.5	Silicon Track Trigger Upgrade	\$229,795.00	\$99,448.75	\$2,160.00	\$0.00	\$231,955.00
325	1.2.6	Trigger Simulation	\$0.00	\$0.00	\$0.00	\$0.00	\$0.00
337	1.2.7	Administration	\$5,500.00	\$2,750.00	\$0.00	\$0.00	\$5,500.00

(Detailed cost estimate provided to committee)



Baseline Schedule: Level 1

project	Milestone Date
WBS 1.2.1: L1 calorimeter •ADF prototype shipped to Fermilab •TAB prototype complete •Production & Testing complete	5/03 5/03 2/05
WBS 1.2.2: L1 cal-track match •Prototype MTFB complete •Production & Testing complete	5/03 6/04
WBS 1.2.3: L1 tracking •Target FPGA algorithm coded •Prototype tested at Fermilab •Production & Testing complete	7/03 4/04 3/05

- Detailed resource-loaded schedule included in material provided
- Installation begins after start of shutdown (5/25/05)



Level 1 Schedule Contingency

scenario	All production and testing complete	Trigger slippage (days)
default	3/9/05	0
extra ADF prototype revision & test	5/2/05	54
extra TAB prototype revision & test	6/8/05	91
extra GAB prototype revision & test	3/9/05	0
double time for all in-situ and integration tests	4/12/05	34
3 rd prototype cycle for DFEAs	6/30/05	113
Cal-trk redesign after internal review	3/9/05	0
All of the above	8/4/05	148

Note: Shutdown period = 5/25/05 - 12/21/05

All scenarios leave at least 4 months for installation and commissioning



Baseline Schedule: Run IIb Level 2

project	Milestone Date
WBS 1.2.4: L2 RunIIb beta •L2 beta prototype testing complete •L2 beta Production Complete	10/04 1/05
WBS 1.2.5: L2 Run IIb STT •Place parts order •Production & Testing complete	4/03 10/04

ID	WBS	Task Name	Duration	Start	Finish	2000	2001	2002	2003	2004	2005	2006
1	1.2	Run IIb Trigger Upgrade	167.2 w	Thu 11/1/01	Tue 3/22/05							
2	1.2.1	Level 1 Calorimeter Trigger	153.2 w	Wed 1/2/02	Tue 2/1/05							
93	1.2.2	Level 1 Calorimeter Track Matching	93 w	Thu 8/1/02	Wed 6/16/04							
140	1.2.3	Level 1 Tracking	114 w	Tue 11/12/02	Wed 3/9/05							
197	1.2.4	Level 2 Beta Processor	47 w	Fri 4/9/04	Tue 3/22/05							
230	1.2.5	Silicon Track Trigger Upgrade	93.1 w	Mon 12/2/02	Fri 10/15/04							
324	1.2.6	Trigger Simulation	110.6 w	Thu 11/1/01	Mon 2/2/04							
336	1.2.7	Administration	120 w	Tue 10/1/02	Tue 3/8/05							

- Detailed resource-loaded schedule included in material provided
- L2 beta processors could be ordered up to 2 years earlier—virtually no schedule risk



Summary

- **DØ trigger upgrade**
 - ◆ Designed to preserve triggering on critical physics processes at high-luminosity operation
 - ◆ Baseline design is complete and documented in TDR
 - ◆ Detailed schedule shows completion compatible with shutdown for installation of silicon detectors
 - ◆ Strong collaboration in place for prototyping, production, simulation, installation and commissioning
- **Much more technical detail available in breakout sessions**