



# ‘The DØ Run 2b Silicon Tracker Project’

## A Technical Overview

Director’s Baseline Review  
August 12-15, 2002

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For the Run 2b Silicon Group



# Outline

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- Physics Motivation and Overview of Silicon Detector Design
  - ◆ Required Performance
  - ◆ Design considerations
  - ◆ Summary of design
  - ◆ Expected Performance
- Overview of Design and status of design and prototyping
  - ◆ Sensors, Mechanical, Electrical, ...
- Testing and Silicon production and assembly choreography
- Summary and Conclusions



# Run IIb: Higgs Boson Potential

## Fermilab Workshop on Higgs Opportunities:

### ◆ Production

- Dominant production channel  $gg \rightarrow H$
- Observable production channel  $qq \rightarrow WH, ZH$

### ◆ Decay

- Dominant decay to  $b\bar{b}$

### ◆ Higgs potential:

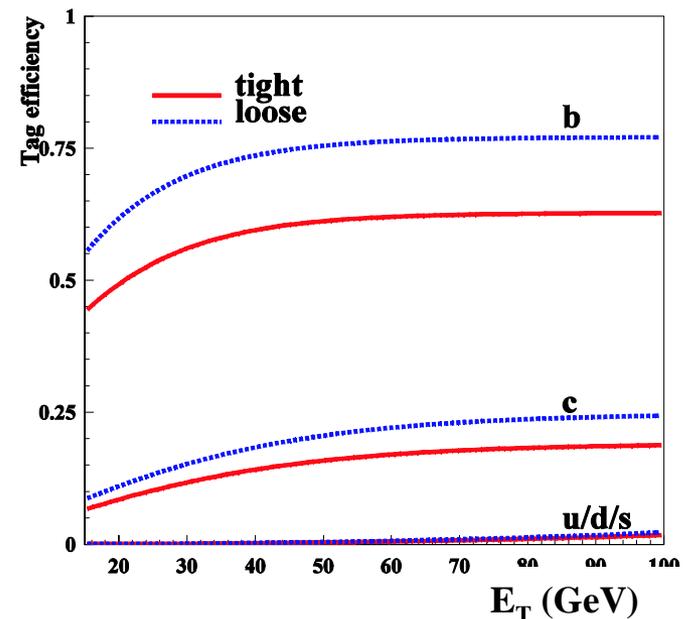
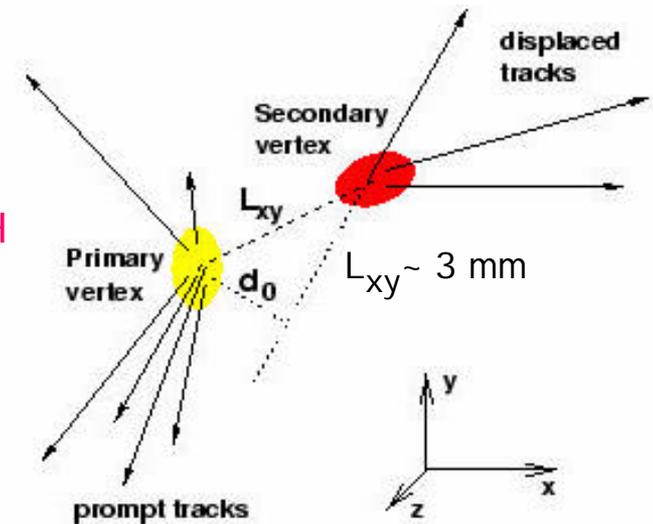
- Luminosity of  $8 \text{ fb}^{-1}$ 
  - $3\sigma$  discovery for  $m_H < 122 \text{ GeV}$
  - exclusion at 95% CL for  $m_H < 135 \text{ GeV}$  or  $150 < m_H < 180 \text{ GeV}$

### ◆ Assumptions of Working Group:

- Loose b-tag:  $\epsilon_b \sim 75\%$  per jet
- Tight b-tag:  $\epsilon_b \sim 60\%$  per jet

## • Requirements

- ◆ Need a replacement Silicon Tracker with
- ◆ Excellent b-tagging efficiency
  - $\epsilon_b > \sim 65\%$  per jet at mistag rate  $< \sim 1\%$
- ◆ Radiation hard to at least  $\sim 15 \text{ fb}^{-1}$





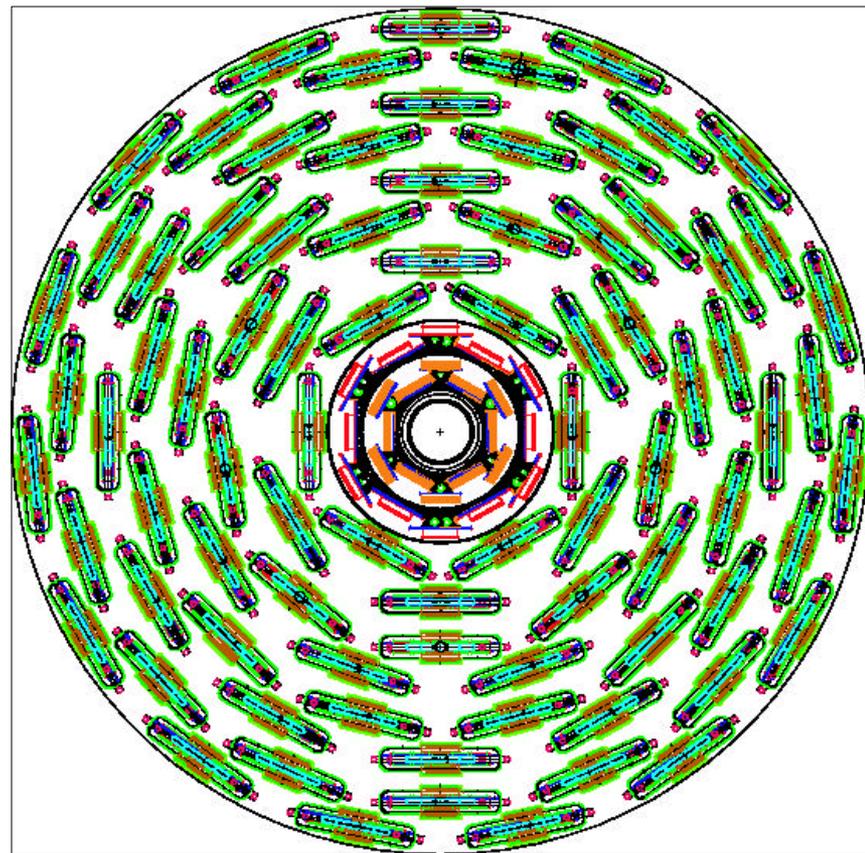
# Design Considerations

- Guiding Principles
  - ◆ Able to build expeditiously
  - ◆ Minimal cost and minimal shutdown time
- Benefit from Run I I a experience
  - ◆ Choose design adequate to achieve physics goals, but do not over-design
  - ◆ Modular design, minimize the number of different elements
  - ◆ Use established technologies: single sided silicon only
- Spatial
  - ◆ Installation within existing fiber tracker, with inner radius of 180 mm
  - ◆ Full tracking coverage
    - Fiber tracker up to  $|\eta| < 1.6$
    - Silicon stand-alone up to  $|\eta| < 2.0$
- Data Acquisition
  - ◆ Retain readout system outside of calorimeter
  - ◆ Current cable plant allows for ~912 readout modules
  - ◆ Total number of readout modules cannot exceed 912
- Silicon Track Trigger
  - ◆ Respect 6-fold symmetry



# Detector Design

- Six layer silicon tracker, divided in two radial groups
  - ◆ Inner layers: Layers 0 and 1
    - $18\text{mm} < R < 39\text{mm}$
    - Axial readout only
    - 50/58  $\mu\text{m}$  readout for L0/L1
    - Assembled into one unit
    - Mounted on integrated support
  - ◆ Outer layers: Layers 2-5
    - $53\text{mm} < R < 164\text{ mm}$
    - Axial and stereo readout
    - 60  $\mu\text{m}$  readout
    - Stave support structure
  - ◆ All sensors intermediate strips
- Employ single sided silicon only, 3 sensor types
  - ◆ 2-chip wide for Layer 0
  - ◆ 3-chip wide for Layer 1
  - ◆ 5-chip wide for Layers 2-5
- No element supported from the beampipe

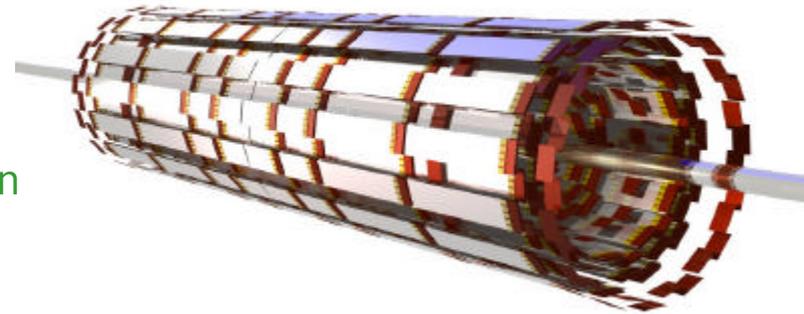




# Performance of Proposed Detector

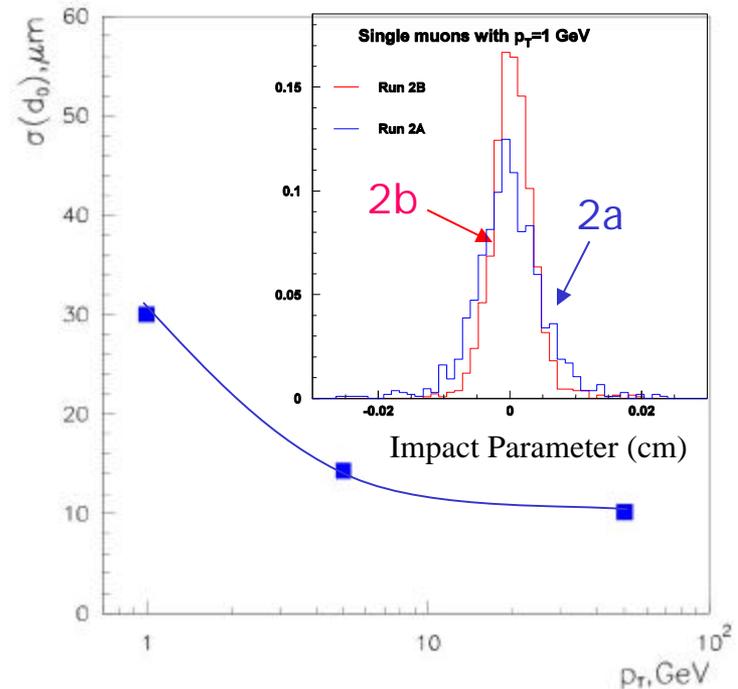
- Performance studies based on full Geant simulation

- ◆ Full model of geometry and material
- ◆ Model of noise, mean of 2.1 ADC counts
- ◆ Single hit resolution of  $\sim 11 \mu\text{m}$
- ◆ Longitudinal segmentation implemented
- ◆ Pattern recognition and track reconstruction



- Benchmarks

- ◆  $\sigma(p_T)/P_T \sim 3\%$  at 10 GeV/c
- ◆  $\sigma(d_0)^2 = 5.2^2 + (25/p_T)^2$ 
  - $\sigma(d_0) < 15 \mu\text{m}$  for  $p_T > 10 \text{ GeV}/c$





# Performance of Proposed Detector

- b-tagging

- ◆ Loose b-tag algorithm: signed impact parameter,  $E_b > 20$  GeV

- Track selection

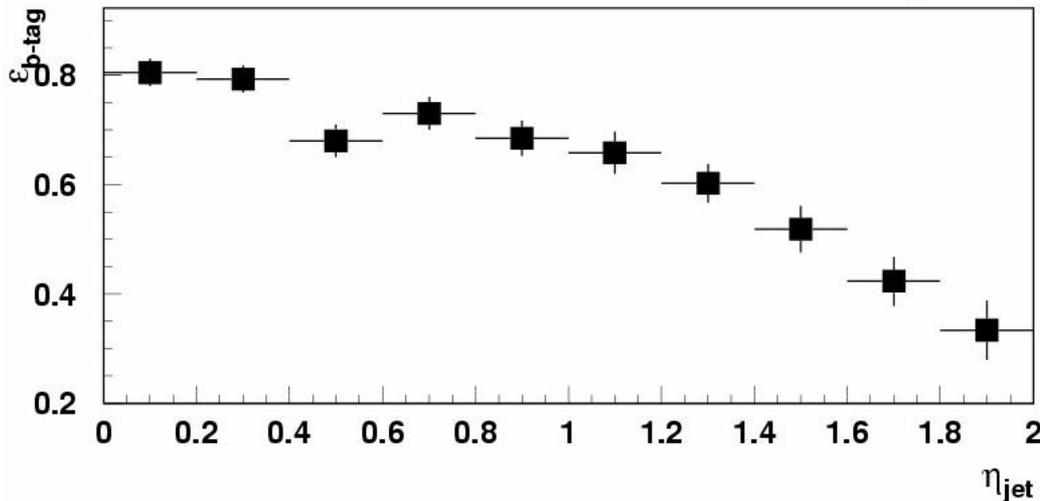
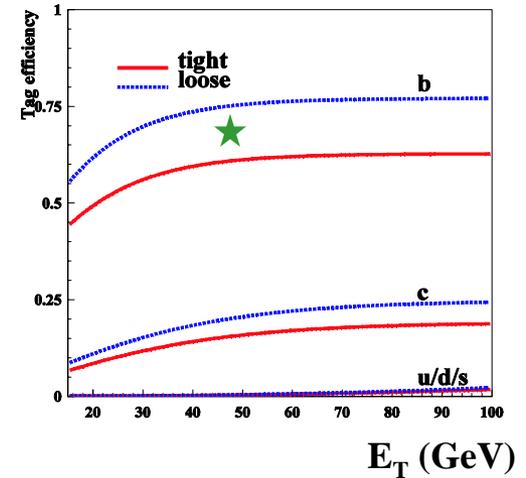
- within cone  $\Delta R < 0.5$  of b-jet
- $p_T > 0.5$  GeV/c, good  $\chi^2$ , hits in silicon  $\geq 2$

- Impact parameter significance

- 2 tracks:  $d_0/\sigma(d_0) > 3$
- 3 tracks:  $d_0/\sigma(d_0) > 2$

- ◆ b-jet tagging efficiency of  $\sim 65\%$  per jet

- Compare to Higgs working group assumptions



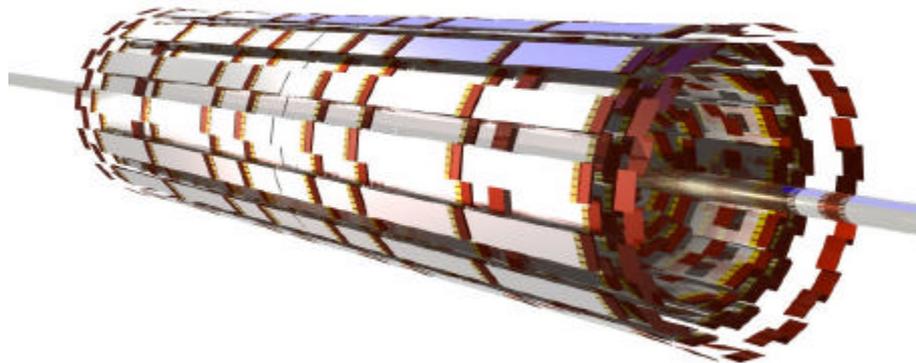
	TDR
$P(n_b \geq 1)$	76%
$P(n_b \geq 2)$	29%
Mistag Rate	$< 1.5\%$

Based on WH-events, with b's falling within acceptance



# Proposed Detector

- Alternate designs and other options have been considered and were found not to be compatible with the constraints and physics motivation for Run II b
  - ◆ b-tagging efficiencies would fall below 50%, especially if analyses would require tighter tagging algorithm
  - ◆ 20% loss in luminosity on  $15 \text{ fb}^{-1}$  would be a 5 GeV reduction in reach on  $m_H$  (115-135 GeV)
- Baseline Design:
  - ◆ Six Layer device
    - Two inner layers with axial readout only
    - Four outer layers with axial and stereo readout
  - ◆ b tagging efficiency of ~65%

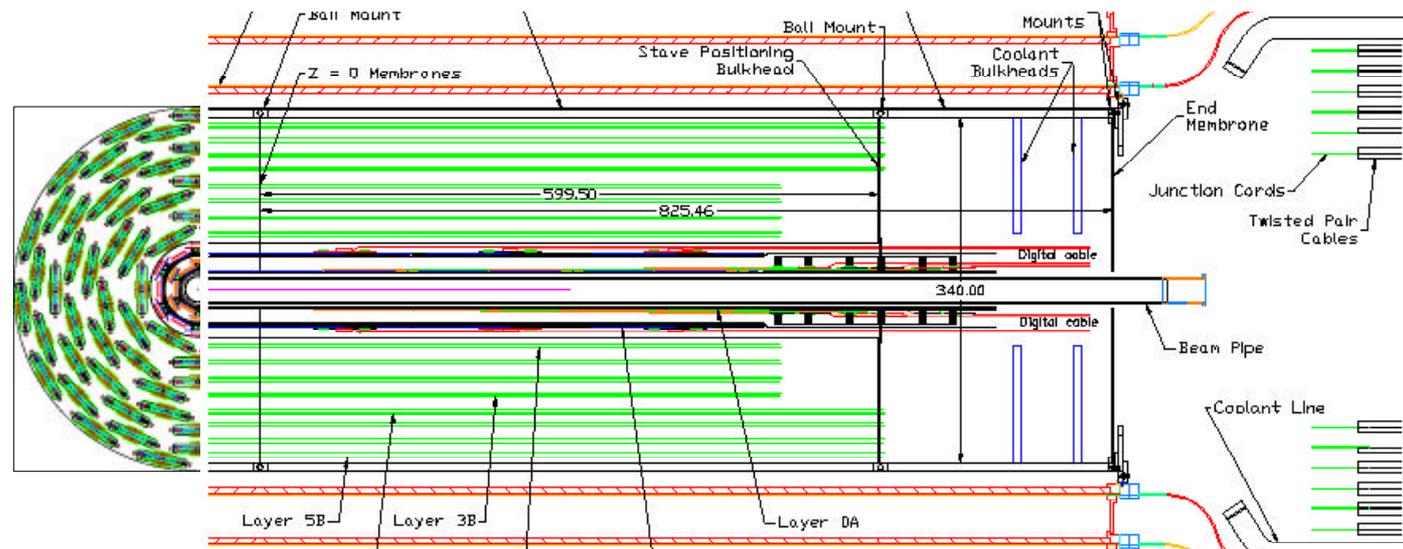


- Baseline Design has received Stage I approval from Fermilab PAC



# From Basics to Details

- Overview of nearly all elements of the detector following the signal path
  - ◆ Sensors
  - ◆ Support Structures
  - ◆ Hybrids
  - ◆ Downstream Electronics
- And how we are setup for testing and production
  - ◆ ...







# Sensors

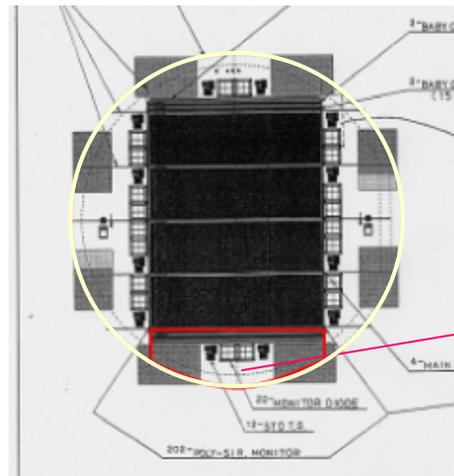
- ELMA (Layer 1)
  - 13 sensors produced; currently being tested. Mechanical sensors are being used for module prototypes

- Layers 2-5

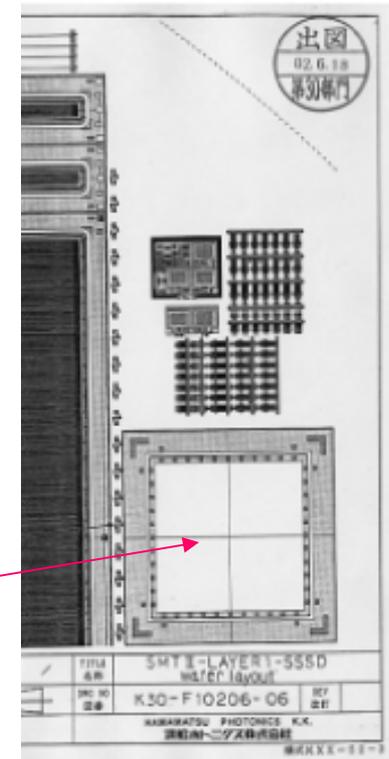
- ◆ 5-chip wide, 60 $\mu$ m pitch, intermediate strips, 41.1x100 mm cut dimension
- ◆ Order being placed with HPK this week; although the order is still being placed, very interactive dialogue with HPK; engineering complete
- ◆ Sensors very similar to CDF outer layer sensors

- Silicon Diodes

- ◆ Needed for radiation monitors
- ◆ Diodes are part of our specifications and are implemented in the test structures
- ◆ Test structures allow for tests of wafer



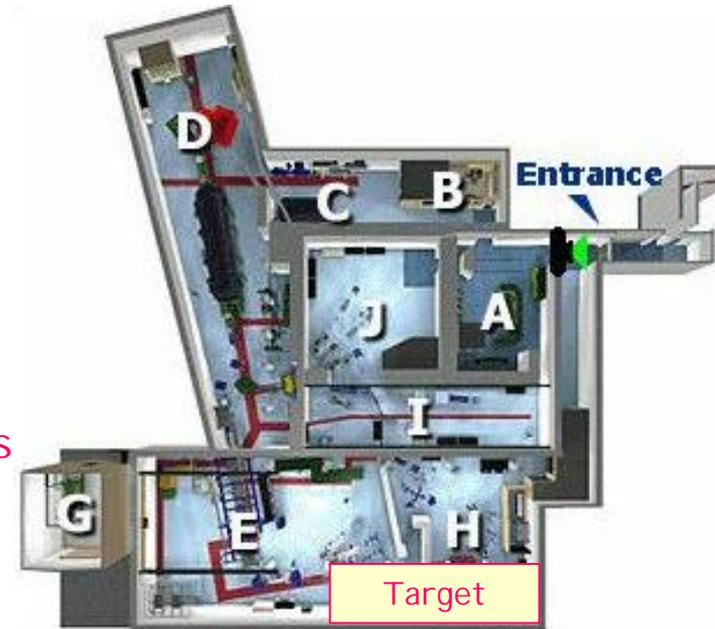
HPK Layer 1 Wafer Layout





# Sensor Testing and Probing

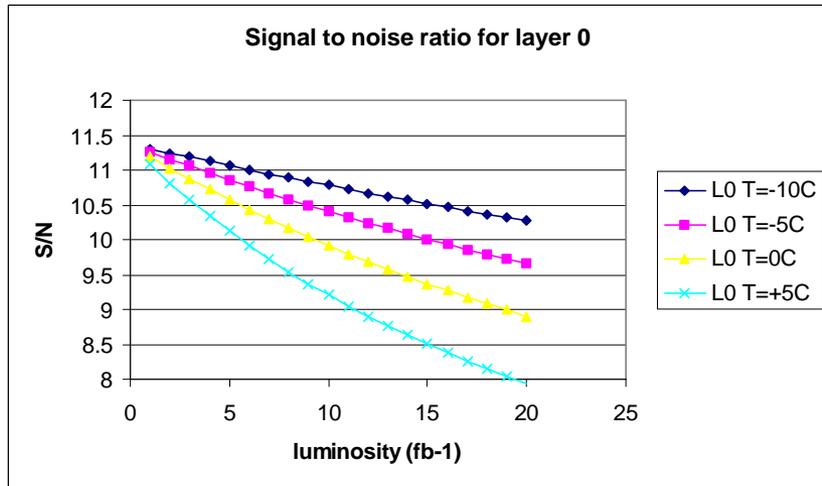
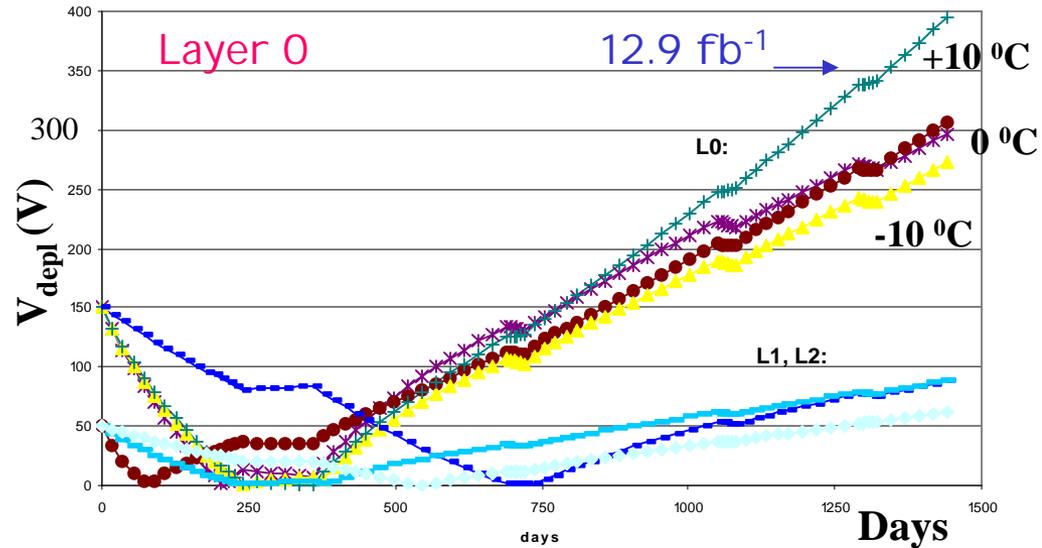
- Irradiation Tests can be performed at KSU (McDonald Lab) and Booster
  - ◆ Tandem p-beam at 10 MeV
  - ◆ Currents at 1 and 10 nA.
  - ◆ 3 mm beam spot
  - ◆ Independent x,y raster
  - ◆ Advantages
    - Well-controlled dosages
    - Flexible scheduling
    - Easy and quick access to irradiated targets
  - ◆ Setup being exercised with prototype ELMA sensors
- Commitment from University groups and Fermilab to probe sensors
  - ◆ KSU, Stony Brook, Cinvestav (Mexico)
  - ◆ All probe station setups in place and being commissioned





# Radiation Damage Requirements

- Sensors will be subjected to fluence of  $2 \cdot 10^{14}$  1 MeV neutron equiv./cm<sup>2</sup>
- Parameters for detector
  - ◆  $V_{\text{depl}}$  after irradiation
  - ◆ Signal to Noise ratio
- Requirements
  - ◆ S/N ratio > 10 after 15 fb<sup>-1</sup>
  - ◆  $V_{\text{depl}} \ll V_{\text{break}}$  to allow for over-depletion for full charge collection

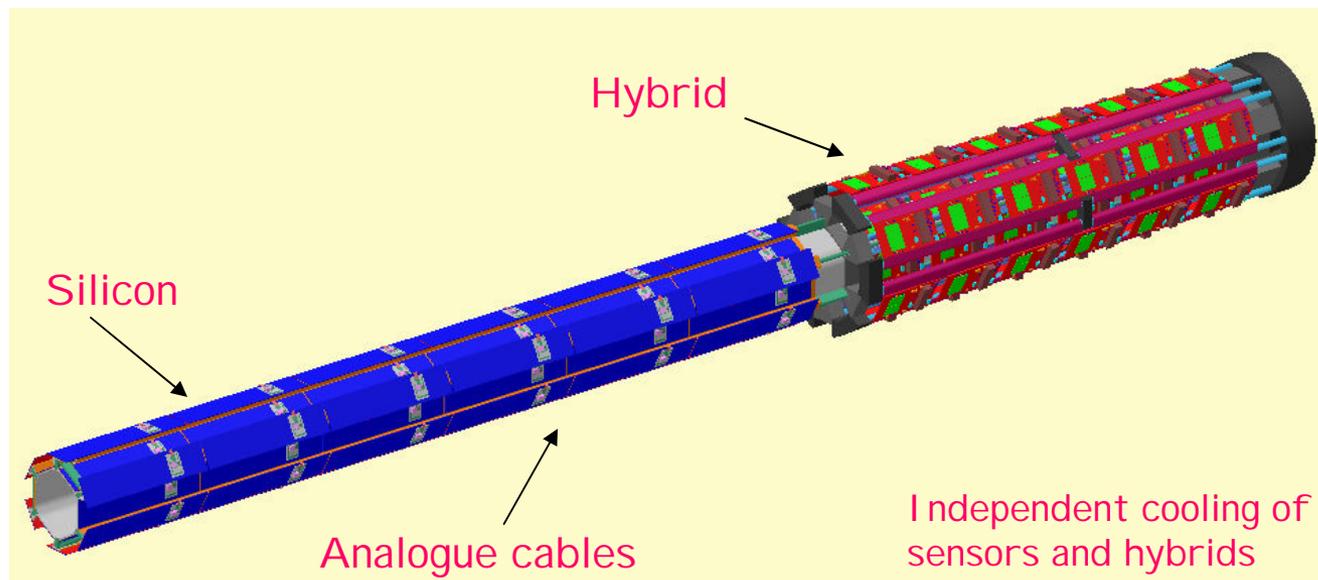
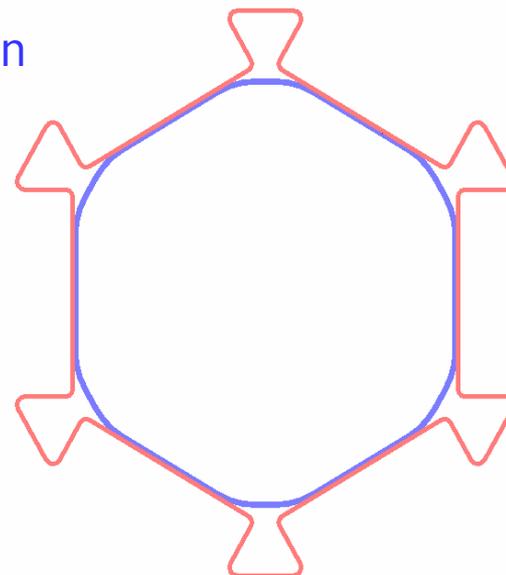


Layer	T_silicon ( C )
Layer 0	-10
Layer 1	-5
Layer 2	0
Layer 3	>0
Layer 4	>0
Layer 5	>0



# Layer 0 and Layer 1

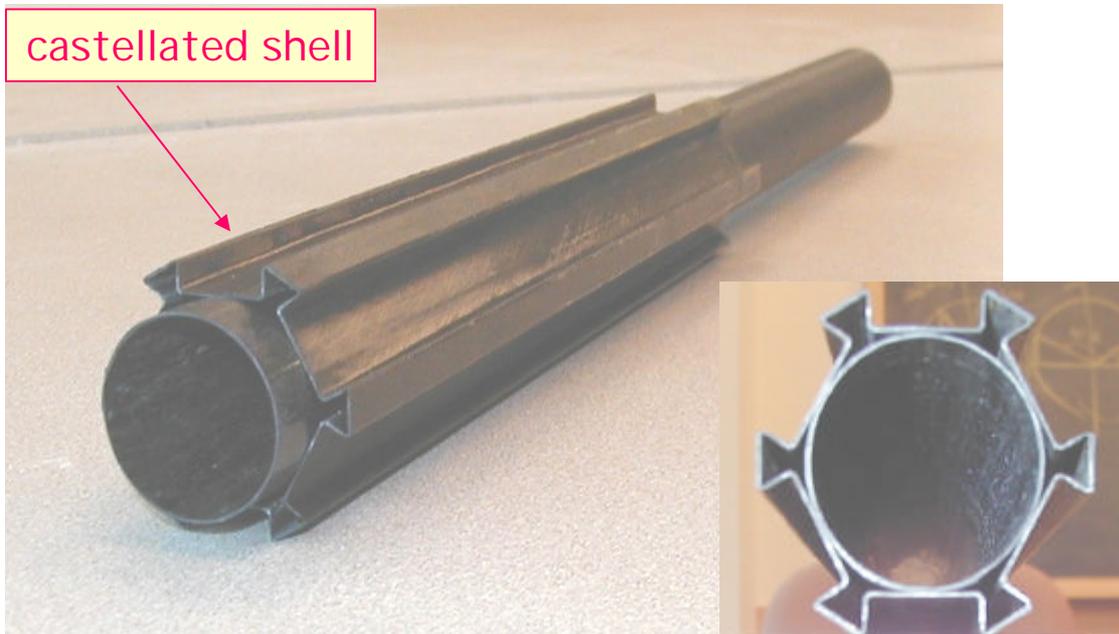
- Support Structure by University of Washington
  - ◆ Inner shell, carbon fiber
    - 12-sided
    - 12 layers  $[0,90]_s$  lay-up
  - ◆ Outer shell, carbon fiber
    - 12-fold crenellated geometry
    - Possible use of pyrolytic graphite
    - Sensors cooled to  $T=-10$  °C
    - No hybrids mounted on sensors for L0: analogue cables





# Layer 0 Support Structure

- Prototype support structure made by University of Washington
  - ◆ Crenellated mandrel of K13C Carbon fiber epoxy prepreg
  - ◆ RTV pressure strips, vacuum bag to remove air bubbles
  - ◆ Pressured to 85 psi
  - ◆ Cured in autoclave at 275 °F

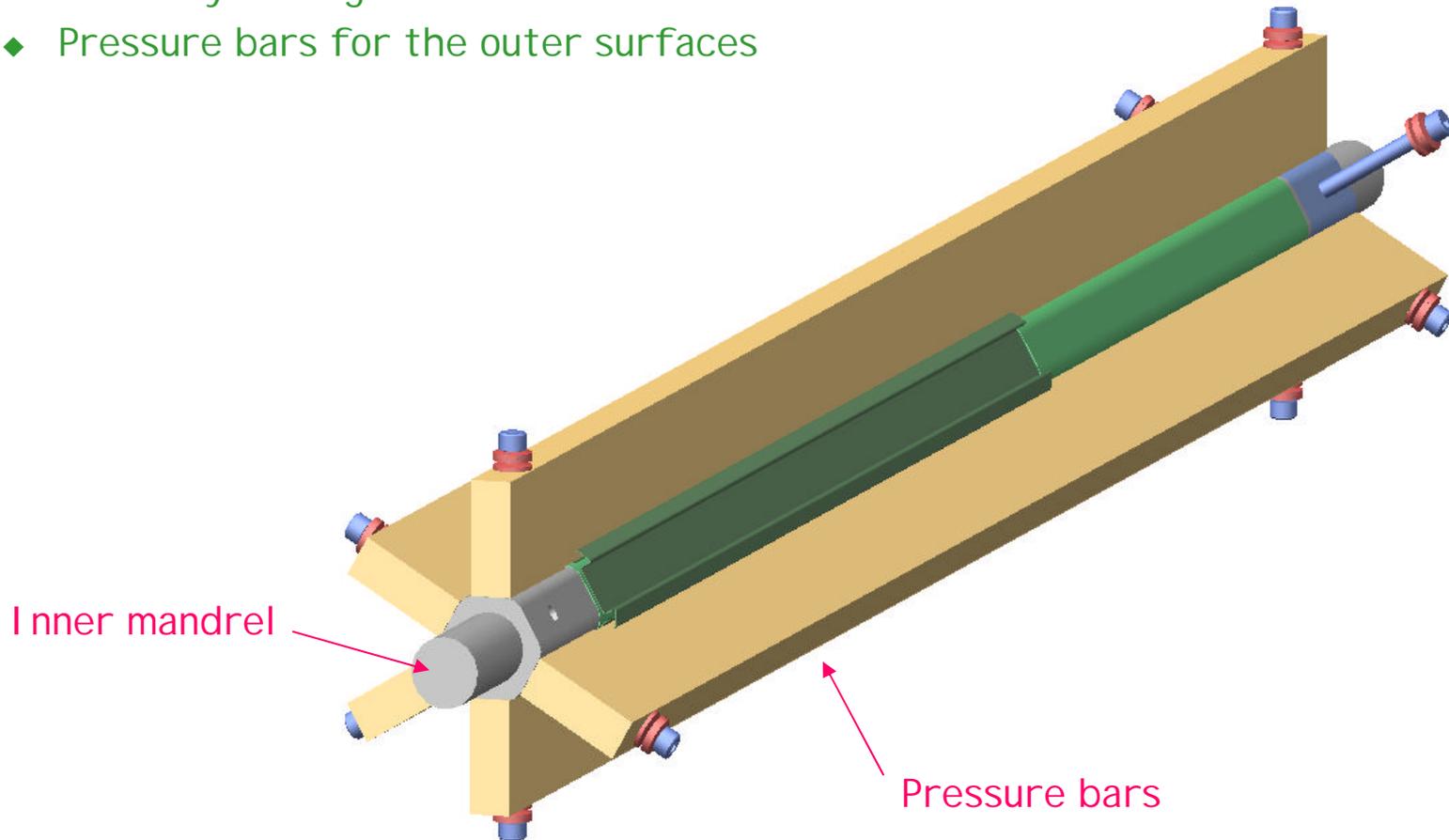


Measurements and comparisons of elastic properties of prepreg. laminates



# Assembly of Shells

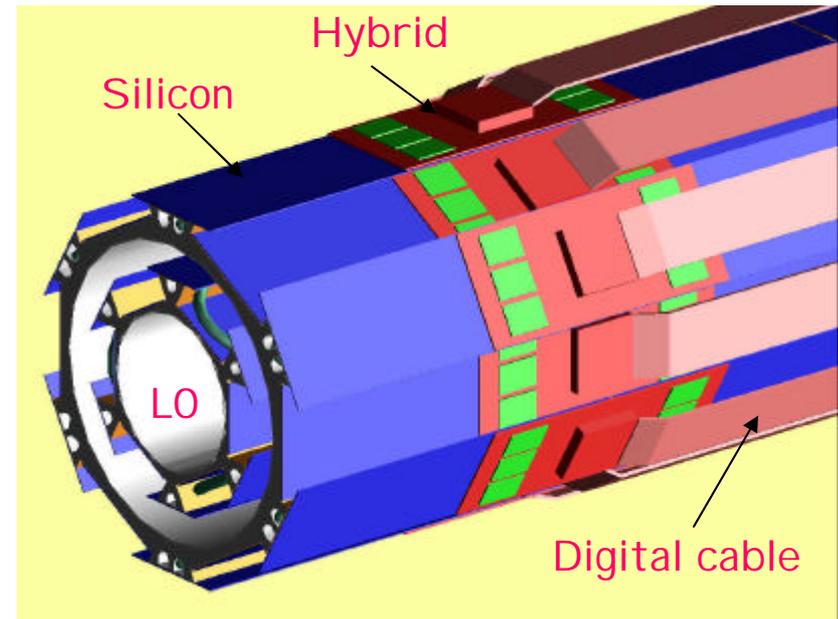
- Tooling being developed for assembly of carbon fiber shells
  - ◆ Inner mandrel will provide support for CF parts, and reference surfaces for assembly tooling
  - ◆ Pressure bars for the outer surfaces





# Layer 1

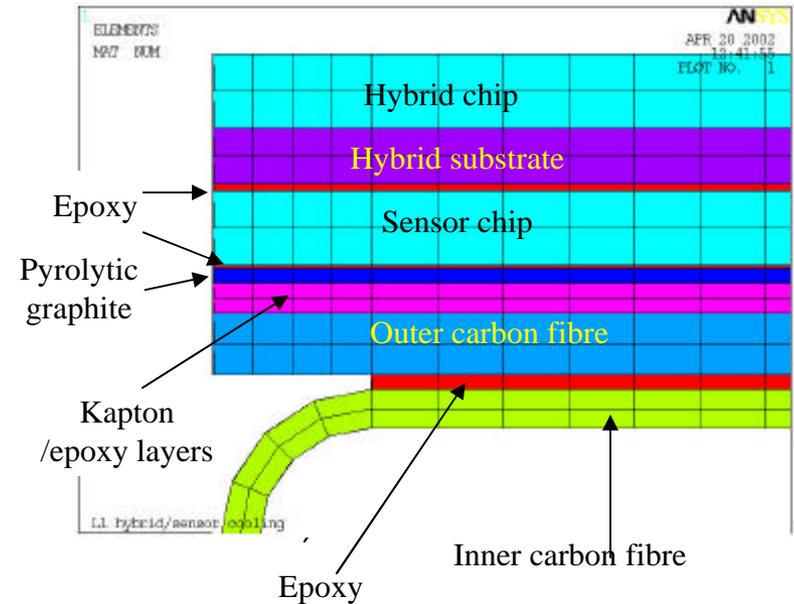
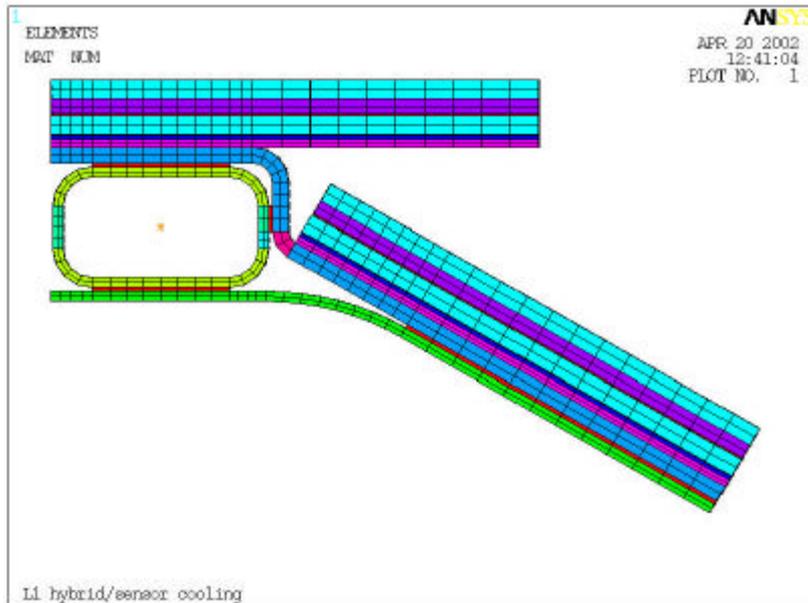
- Support structure similar to Layer 0, also done by U. of Washington
- Readout electronics mounted on the sensors:
  - ◆ Power dissipation of 0.5W/chip
  - ◆ Power dissipation of  $< 0.1$  W/sensor after  $15 \text{ fb}^{-1}$
- To minimize radiation damage,  $T_{\text{Si}} < -5 \text{ }^{\circ}\text{C}$
- Cooling:
  - ◆ Layer 0
    - Hybrids outside tracking volume
    - Independent cooling of sensors and hybrids
  - ◆ Layer 1 toughest: hybrids mounted on sensors, radial position
    - Modestly conservative power dissipation of svx4 chips assumed
    - Possible to run coolant at  $-20 \text{ }^{\circ}\text{C}$
- FEA analyses





# Layer 1 FEA analysis

- Parametrized Model of Layer 1 structure for FEA analysis

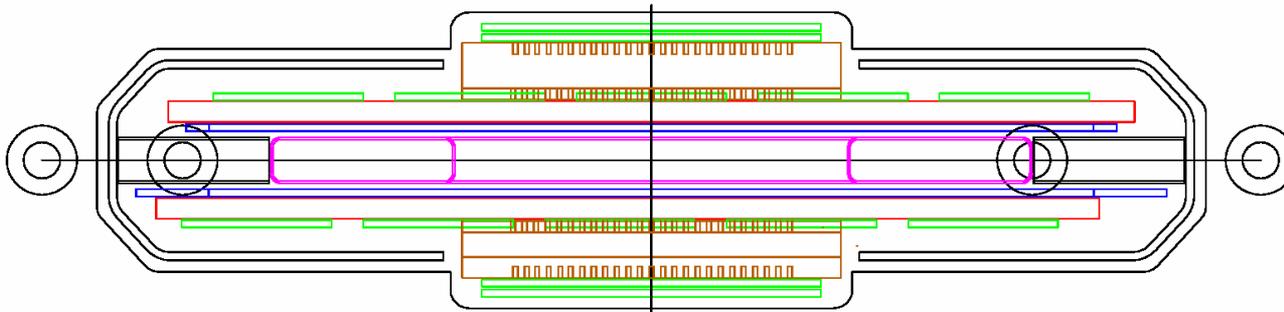


- ◆ Model incorporates all layers in the assembly
- ◆ Maximum temperature of the Silicon is -4 °C from FEA analysis



# Layers 2-5: Staves

- Basic building block of the outer layers is a stave



- Stave is:
  - ◆ two-layer structure of silicon sensors
  - ◆ One layer of axial only and only layer of stereo only readout
    - stereo angle obtained by rotating the sensor
  - ◆ Layers separated by a “core” with positioning and reference pins and cooling tubes
  - ◆ Total of 168 staves
- C-shells at edge of stave provide stiffness
- Staves are positioned and supported in carbon fiber bulkheads at  $z = 0$  and  $z = 605$  mm.
  - ◆ Locating features on stave provide the alignment



# Readout Modules

- Each stave has four readout modules
- Readout module lengths vary with layer and z-position.
  - ◆ For all layers, the modules closest to  $z = 0$  are 200 mm long
  - ◆ Those furthest from  $z = 0$  are 300 mm long in L2-L3 and 400 mm long in L4-L5.
- Six Readout module types
  - ◆ 10-10 (axial, stereo)
  - ◆ 10-20 (axial, stereo)
  - ◆ 20-20 (axial, stereo)
  - ◆ Ganged sensors will have traces aligned (sensors are 10cm long)
- Module configuration



Layer 4-5

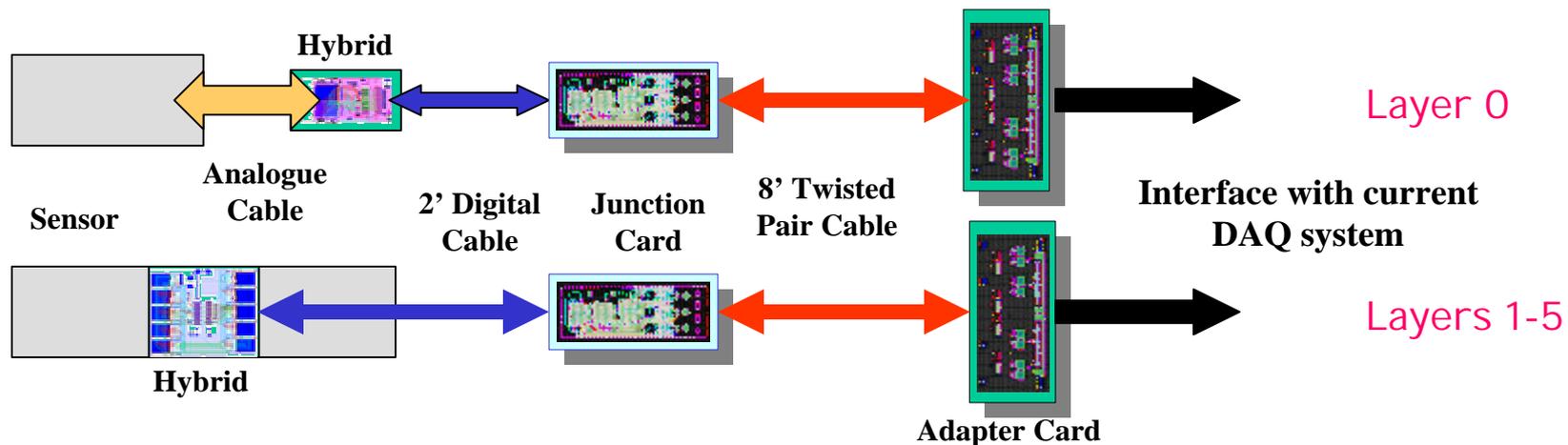


Layer 2-3

- Each readout module serviced by double-ended hybrid
  - ◆ Each hybrid has two independent readout segments



# Readout Schematics

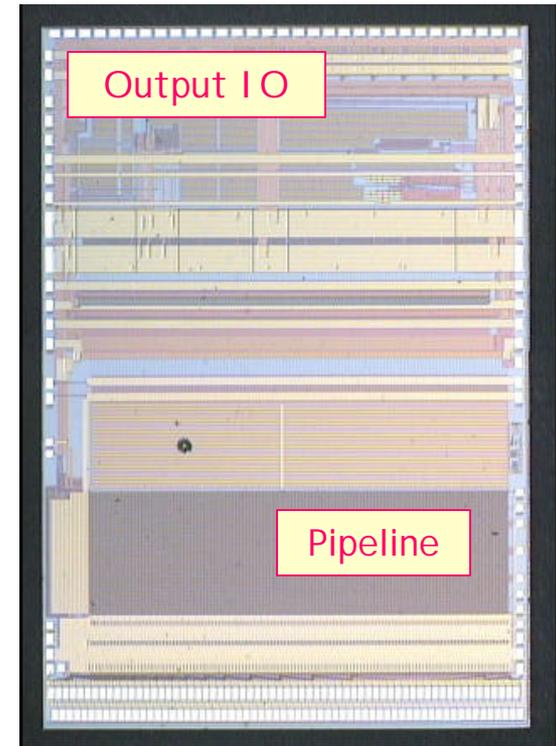


- Layers 1-5: Hybrids mounted on silicon
  - ◆ Hybrid -> digital cable -> junction card -> twisted pair -> Adapter Card
- Layer 0: Hybrids mounted off-board
  - ◆ Analogue Cable -> Hybrid -> digital cable -> junction card -> twisted pair -> Adapter Card
- SVX4 chips mounted on hybrid; employed in SVX2 readout mode



# SVX4 Chip

- SVX4 full prototype chip received and being tested
  - ◆ 0.25  $\mu\text{m}$  technology, intrinsically rad-hard
  - ◆ Successor of SVX2 and SVX3 chip
  - ◆ Both experiments use the same chip
  - ◆ Major success in commonality between CDF and DØ
  - ◆ DØ operates the chip in DØ-mode (dead-time)
  - ◆ Preproduction versions
    - Pre-amp (MOSIS 11/25/00)
    - Pre-amp and pipeline (MOSIS 06/04/01)
- SVX4 chip works !!
  - ◆ Major success and gives both projects an excellent headstart for full-scale testing of all elements of the detector
  - ◆ Tests at LBL
  - ◆ Tests at Fermilab
    - Stimulus setup





# SVX4 Chip

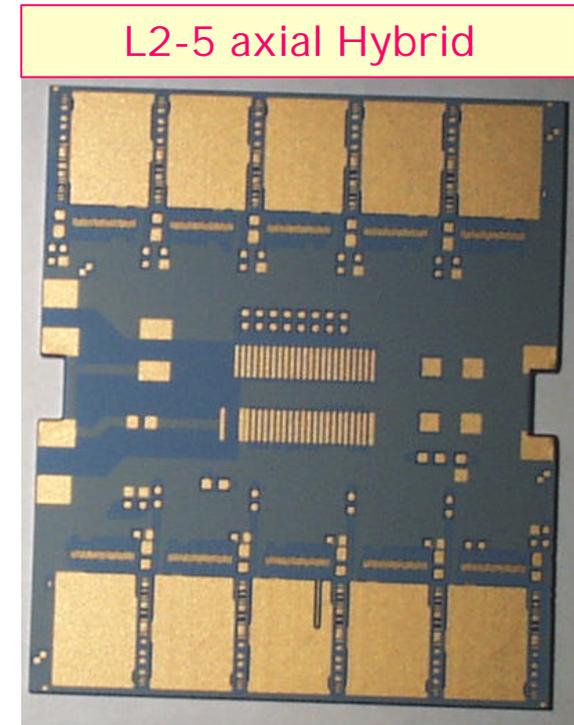
- Sample list of verifications done so far
  - ENC = 300e + 41e/pF C (Fermilab)
  - ENC = 600e + 32e/pF C (LBL)
- Known problems:
  - ◆ Add pull-up to USESEU
  - ◆ Add pullup or pulldown to DØ-mode
  - ◆ Pull MSB of ChipID high.
  - ◆ Logic changes to FECLK gating/ADC control/FE control in DØ-mode
- Tests to do
  - ◆ Frequency & duty cycle margin
  - ◆ Systematic test of all SVX4 specifications
  - ◆ Power consumption in various modes
  - ◆ SVX4 with silicon - black hole clamping feature, behaviour with various cables
  - ◆ Irradiation
- Both experiments plan to study SEU at UC Davis during the second week of September; irradiation of chip with <sup>60</sup>Co-source in Sacramento at the same time

	Parameter	Spec	Met
Preamp	Gain	3mV/fC	✓
	Gain Unif.	< 5%	✓
	Risetime	60-100 ns	✓
	Rise adjust.	4 bits	✓
	Noise	2000e @ 40pF	✓
	Dyn. range	> 200 fC	✓
	Cal inject		✓
Pipeline	Reset time	< 20ns	✓
	Ped. Uniformity	<500e	✓
	Linearity	<0.25%	✓
	Diff. non-lin.	<0.5 LSB	
Output	Risetime	2ns - 4ns	✓
	Bus	bi-directional	✓
	Priorities In-Out		✓
Regstr/Cnt	Cells	SEU tolerant	
	Bit assignments		✓
	Resets		✓
	ch. 63 latch		✓
	D0 mode		



# Hybrids

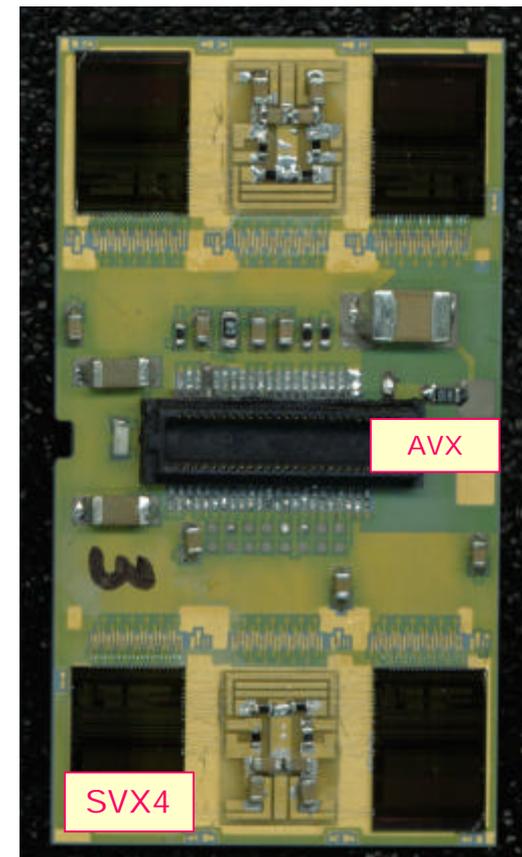
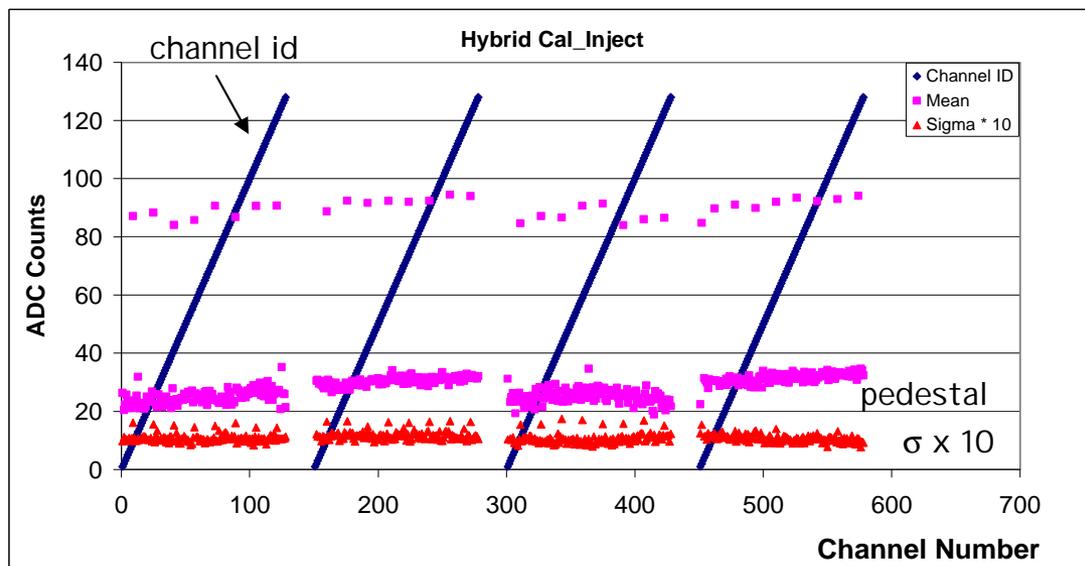
- Design:
  - ◆ BeO substrate with multi-layer circuit on substrate
    - 6 Au layers and 5 di-electric layers
    - Use screenprinting, min. via size 8 mils, ~10 mil spacing
  - ◆ Four types of hybrids
    - Layer 0: two-chip
    - Layer 1: six-chips, double-ended
    - Layer 2-5: ten-chips, double-ended
      - axial and stereo (only different in width)
  - ◆ Use 50 pin AVX 5046 connector, 2.5 mm high
- Prototypes
  - ◆ Layer 1
    - 18 hybrids received from CPT (California)
  - ◆ Layer 2-5
    - 23 axial received from Amitron (Massachusetts)
    - 50 axial, 50 stereo ordered from CPT
      - to arrive early September
  - ◆ In the process of qualifying both vendors





# Layer 1 Hybrid

- One Layer 1 hybrid mounted with four SVX4 chips
- Readout with current DØ stand-alone readout system
  - ◆ All channels readout
  - ◆ Cal-inject set pattern of channels



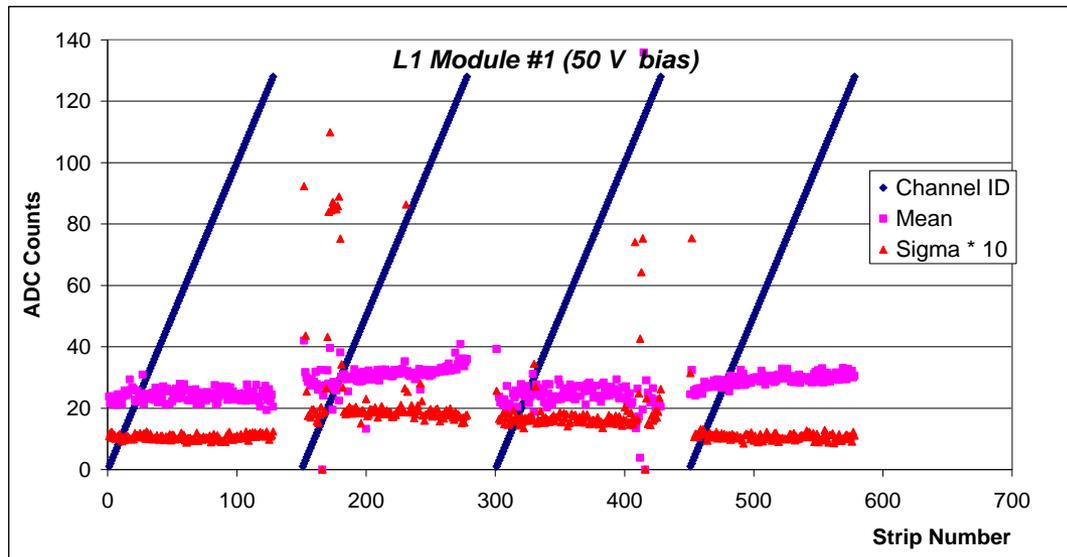
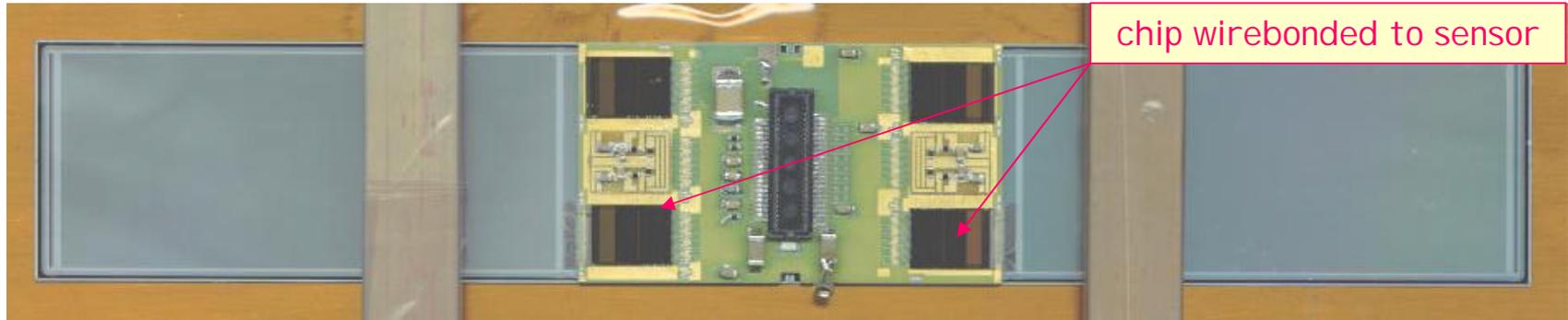
**Major success on many fronts !**

**Many kudos to the chip designers and testers and 'the troops in the field'**



# Layer 1 Readout Module

- Mount the hybrid on two Layer 1 ELMA sensors and try to read it out

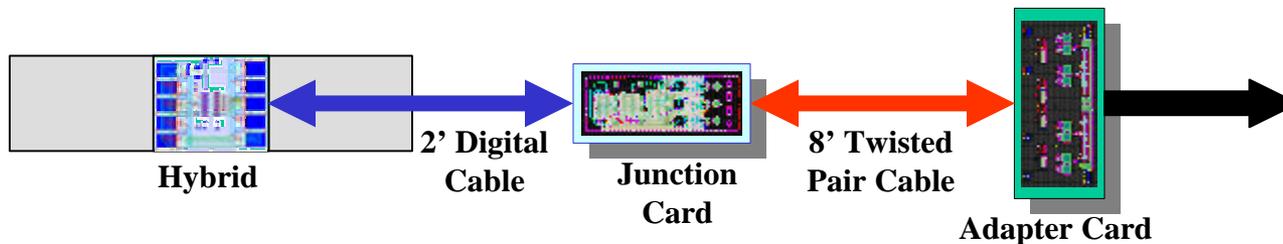


- ◆ Chip 2 and 3 wirebonded to sensor
- ◆ Detector biased to 50V
- ◆ Noise slightly higher for chip 2 and 3
- ◆ Sigma of pedestal  
~ 1 ADC count (no sensor)  
~ 1.8 ADC counts w/ sensor  
Meets spec.
- ◆ Proof of principle that SVX4 + Hybrid + Readout System work !
- ◆ Tests continue



# Near Term Plans for Hybrids

- 23 L2A hybrids received: 13 at FNAL, 10 at Fresno
- We are in the process of qualifying surface mount companies
  - ◆ Meltronix, COB and Promex (used in Run II a)
  - ◆ Have enough SVX4 chips on hand to be able to qualify vendors
- Three institutions responsible for hybrid testing and burn-in
  - ◆ Fresno (liaison with stuffing companies)
  - ◆ Kansas University
  - ◆ Fermilab
  - ◆ All institutions are gearing up for hybrid testing





# Digital Jumper Cable

- All layers use the same design done by KSU
  - 10-12 different lengths, max length ~ 1 m
  - Kapton substrate, total thickness 250  $\mu\text{m}$  for L0-1, 330  $\mu\text{m}$  for L2-5
  - HV on the same cable
  - AVX 50-pin connector on both sides
- Prototypes received from two vendors
  - Honeywell
  - Basic Electronics
  - All cables test ok
- Test Center being setup at Louisiana Tech
  - Impedance, Resistance, cross-talk

	L2-5			L0-1	
	50cm	100cm	35cm	50cm	100cm
Honeywell	10	20	10		
Basic Elc.	10			10	20

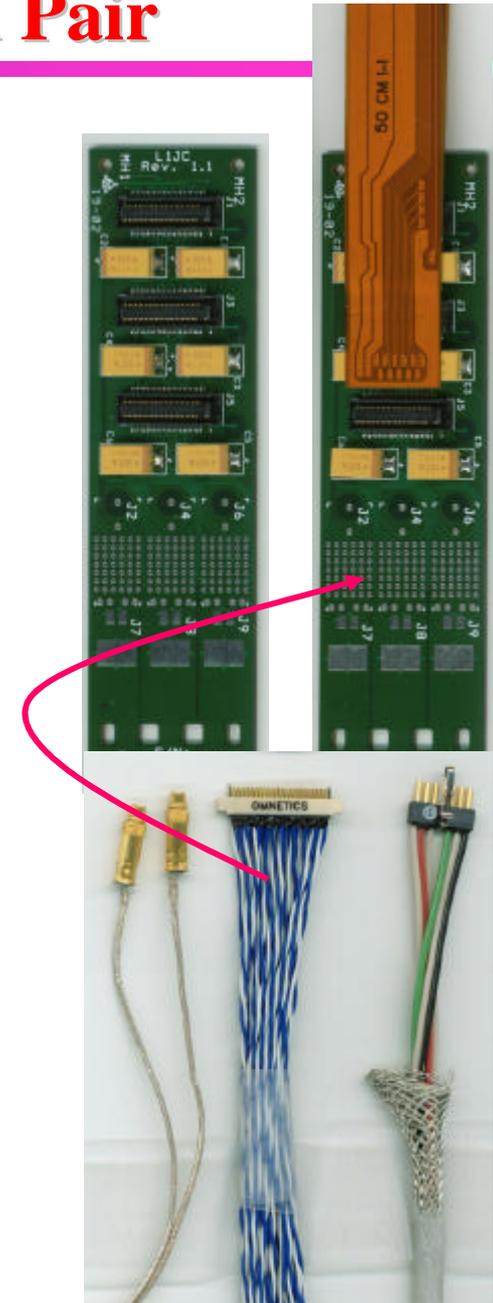
Pin #	Trace	Cable 1 Resistance	Cable 2 Resistance	Specified in dj_section_27 nov01
37	AVDD	0.133 $\Omega$	0.148 $\Omega$	0.168 $\Omega/\text{m}$
39	AVDD	0.133 $\Omega$	0.139 $\Omega$	0.168 $\Omega/\text{m}$
45	DVDD	0.125 $\Omega$	0.149 $\Omega$	0.144 $\Omega/\text{m}$
47	DVDD	0.126 $\Omega$	0.136 $\Omega$	0.144 $\Omega/\text{m}$
7	GND	0.0715 $\Omega$	0.0685 $\Omega$	0.068 $\Omega/\text{m}$





# Junction Card and Twisted Pair

- Two types of Junction cards
  - ◆ L0/1: 3 hybrids → 1 junction card
  - ◆ L2-5: 2 hybrids → 1 junction card
- Designed by KSU
  - ◆ Card has no active elements
  - ◆ Receiving: 50-pin AVX connector
  - ◆ Outgoing: soldered twisted pair cable bundle
- Twisted Pair (Fermilab)
  - ◆ Power & HV lines : 6-pin Omnetics connector
  - ◆ Signal pairs : 44-pin Omnetics connector
  - ◆ Coax cables for clock signals
  - ◆ 5 cables received
    - 3 kits sent to Novosibirsk for attachment
  - ◆ Vendors:
    - New England Wire and Omnetics
    - Considering Axon (France), Ecolab (Germany) (common with CDF)





# Adapter Card

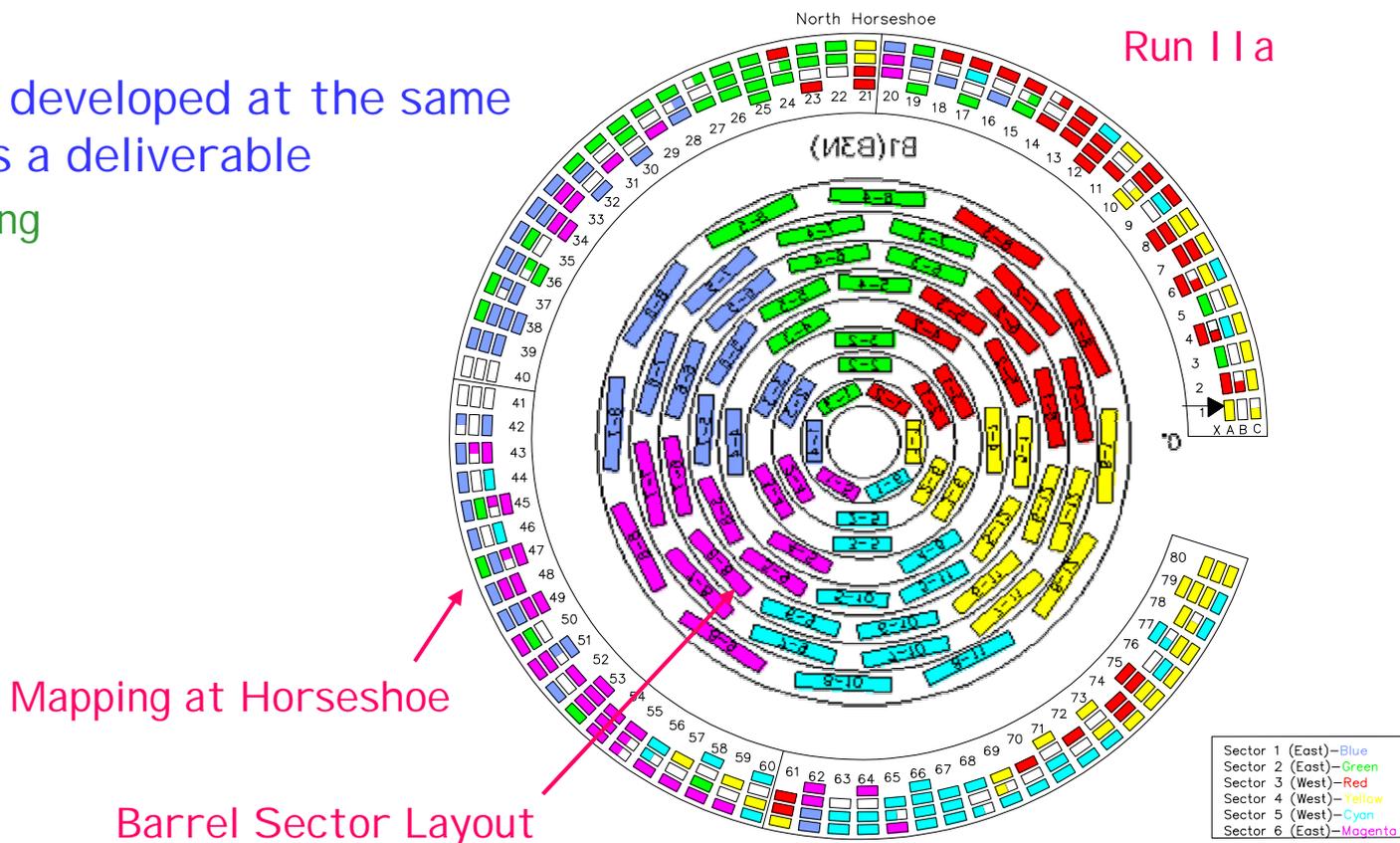
- Active Card, designed by KSU
  - ◆ Two voltage regulators per hybrid: analog and digital voltages
  - ◆ Differential-to-Single-Ended 2.5 to 5 V translation for SVX4 Data
  - ◆ 5 to 2.5 V translation for SVX4 Controls
  - ◆ Routing of Clock and HV
- Each adapter card has four or six channels
  - ◆ Input: twisted pair
  - ◆ Output 80-conductor 3M cable (existing)
  - ◆ 12 boards fabricated, one stuffed
  - ◆ Currently being tested
- Adapter Cards are mounted on face of calorimeter
  - ◆ Four rings of adapter cards (dubbed the “horseshoe”)
  - ◆ Now active element, needs cooling, ~700W per end
  - ◆ Cooling being studied





# Mapping and Software

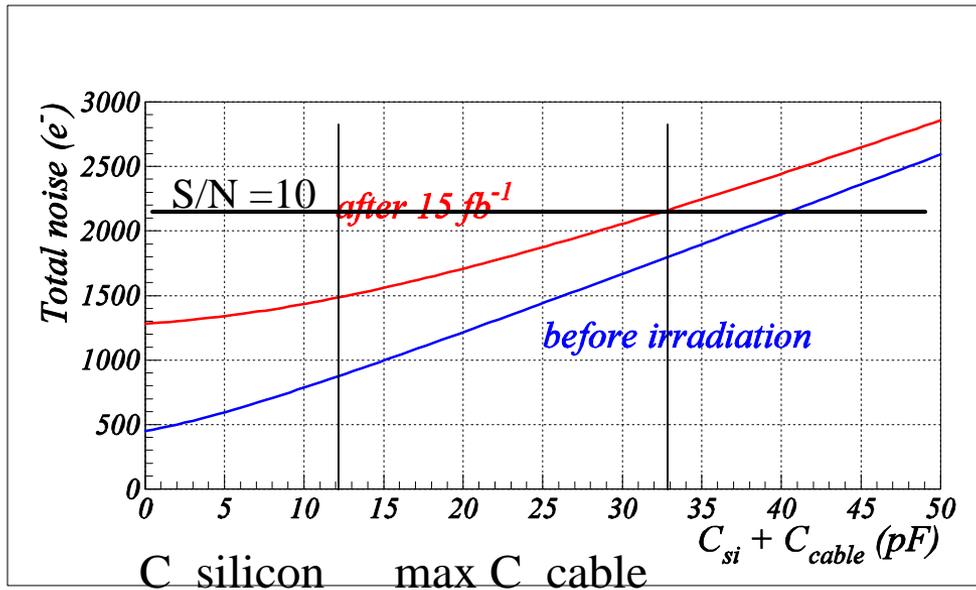
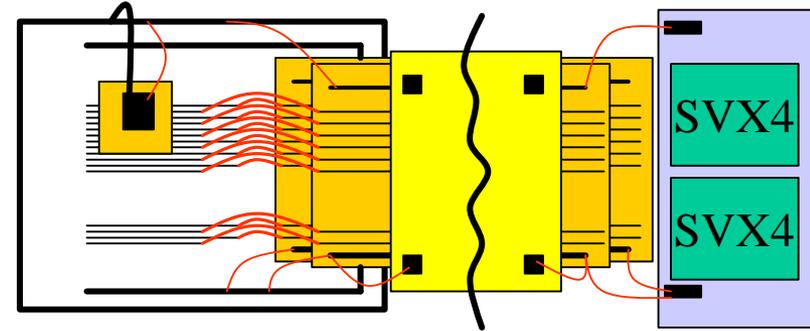
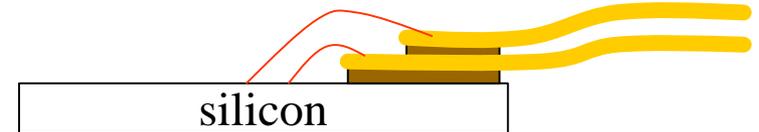
- The horseshoe is the junction of the new readout and the Run I I a readout
- Constraints:
  - ◆ Cannot move existing cable plant
  - ◆ Mapping has to satisfy Silicon Track Trigger
  - ◆ Mapping ought to 'make sense' for debugging purposes
- Software being developed at the same time, treated as a deliverable
  - ◆ Data Unpacking
  - ◆ Data analysis
  - ◆ Calibration
  - ◆ Monitoring





# Analogue Flex Cables

- For layer 0 need low mass, fine pitch flex cables to carry analogue signals to hybrids
  - ◆ Technically challenging
    - Trace width ~ 15 - 20  $\mu\text{m}$ , pitch 91  $\mu\text{m}$
    - 2 cables offset by 50  $\mu\text{m}$
  - ◆ Noise determined by capacitance
    - $C < 0.55 \text{ pF/cm}$
    - Dyconex (2<sup>nd</sup> prototype)
    - (Compunetics gave up)

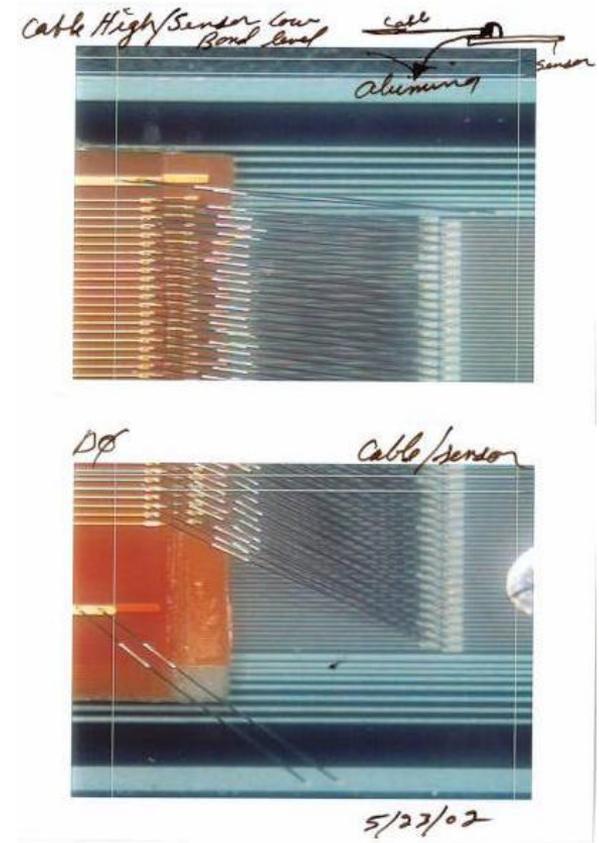
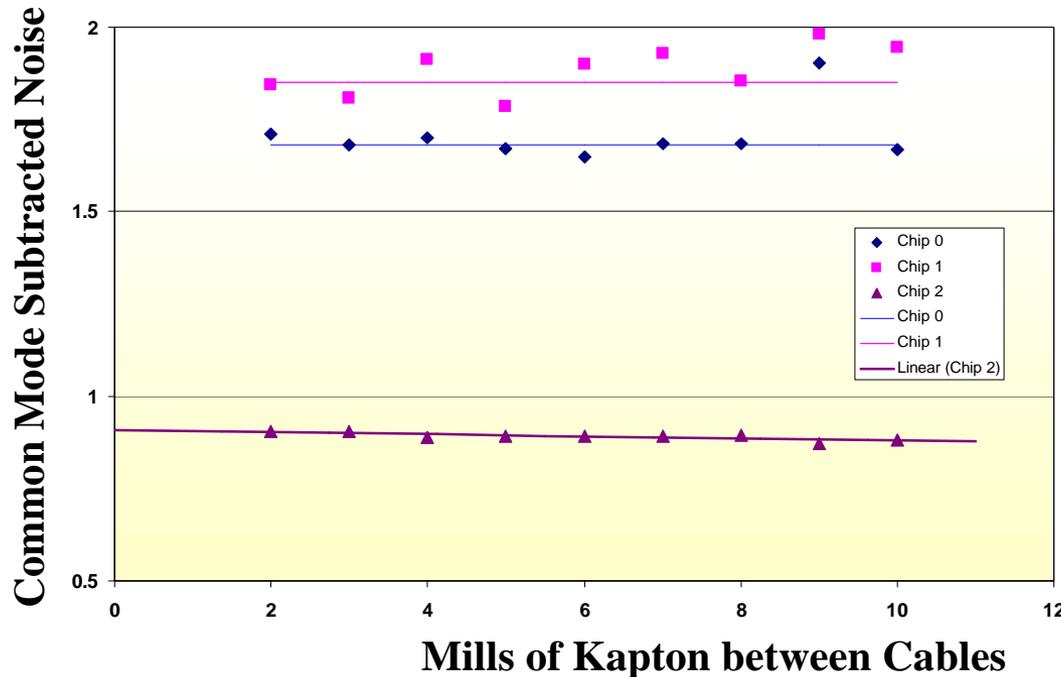


Based on FEA analysis:  
16  $\mu\text{m}$  trace width  $\rightarrow$  0.32 pF/cm



# Analogue Flex Cable Tests

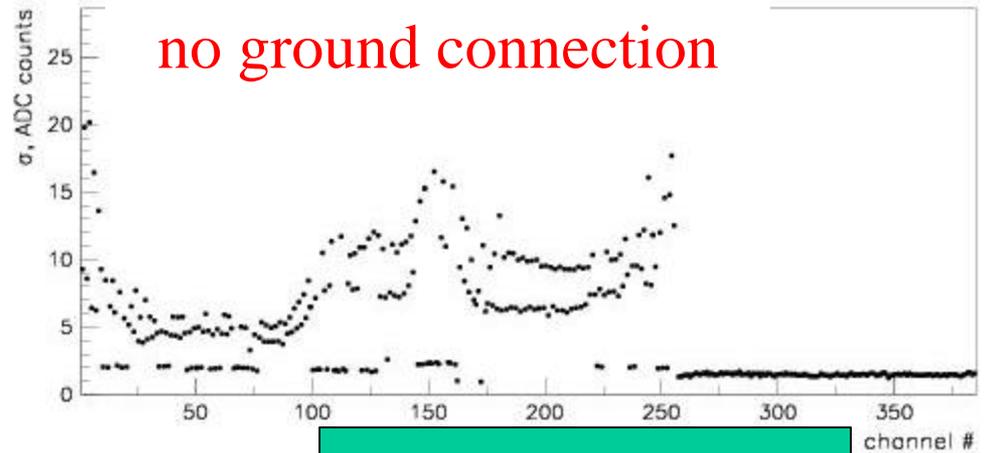
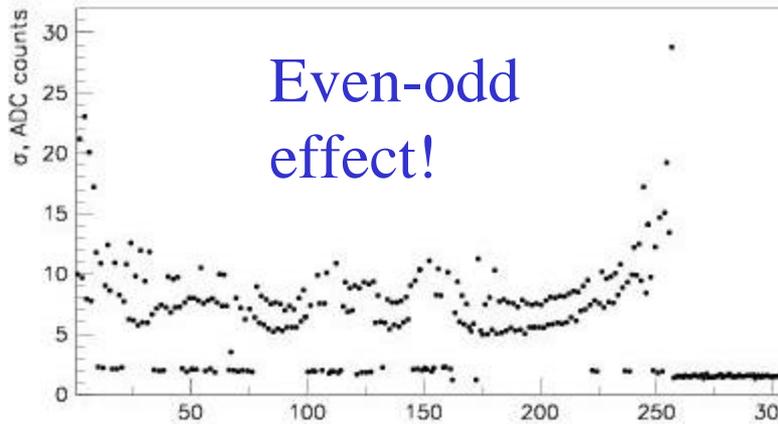
- Second prototype cables (Dyconex, Zürich)
  - ◆ First batch: 12 cables. Two had 2 open/shorts, remaining were good
  - ◆ Second batch: 27 cables; 16 perfect, 9 had 1 open, 2 = 2 open/short
- Build full Layer 0 module, with Run II a hybrid readout, 2 chips connected
- Study of noise with various shielding



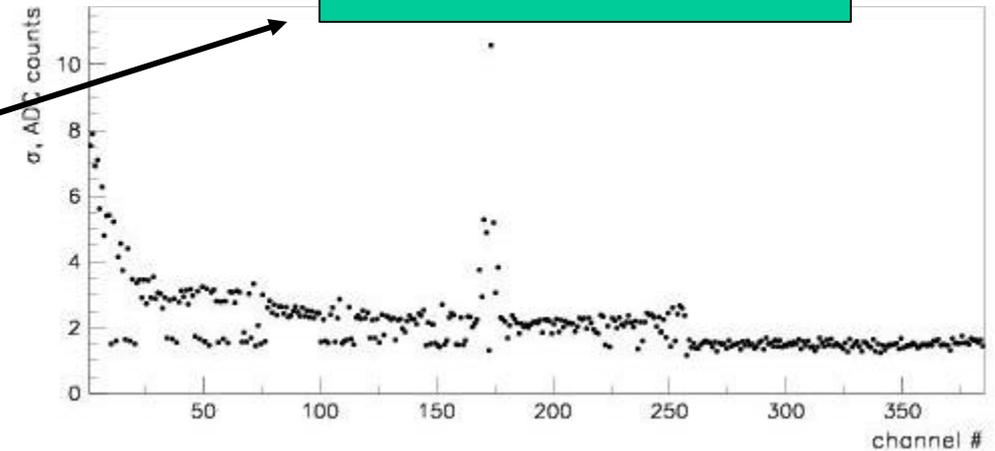


# Analogue Flex Cable Tests

- Shield with Al foil under the flex cable grounded or not grounded



Location of the aluminum foil



Recall cable is spliced

with ground connection



# Summary of Prototyping

Component	Vendor	First Prototype		Second Prototype		
		Design	Ordered	Delivered	Ordered	Delivered
L0 Sensors	ELMA	✓	✓	✓		
	HPK	✓				
L1 Sensors	ELMA	✓	✓	✓		
	HPK	✓	✓			
L2 Sensors		✓	✓			
Analogue Cable	Dycx	✓	✓	✓	✓	✓
L0 Hybrid		80%				
L1 Hybrid	CPT	✓	✓	✓		
L2A Hybrid	CPT	✓	✓			
	Amitr.	✓	✓	✓		
L2S Hybrid	CPT	✓	✓			
Digital Cable	Honey	✓	✓	✓	✓	✓
	Basic	✓	✓	✓	✓	
Junction Card		✓	✓	✓		
Twisted Pr. Cable		✓	✓	✓		
Adapter Card		✓	✓	✓		
Purple Card		✓	✓	✓	✓	
Test Stand Elctr.		✓	✓	✓		

- Except for HPK sensors and Layer 0 hybrids, have prototypes of all components in hand and no major issues have been encountered so far



# Other Tests Underway

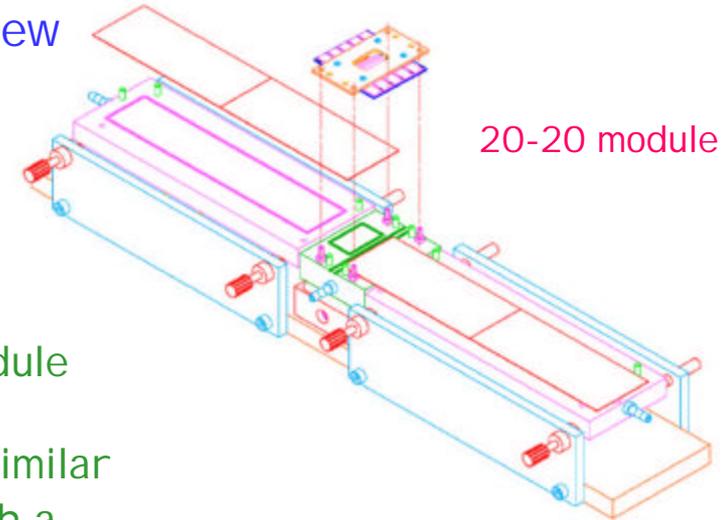
- Chain digital cable -> junction card -> twisted pair being tested
- Grounding of carbon fiber support structures being studied
  - ◆ carbon fiber is a conductor and needs to be grounded
  - ◆ embed 12  $\mu\text{m}$  thick Al foil in carbon fiber with about 10-20% coverage
  - ◆ foil is strips along crenellated structure extending into flat area
- Long Term Cooling Test of Cooling Tubes
  - ◆ Baseline for cooling tubes is carbon fiber prepreg
    - Four plies are likely in L2-L5. Grounding at hybrids is needed.
    - Studies of PEEK tubing are continuing with reduced emphasis to ensure there is a back-up solution.
    - Cross-sectional dimensions are approximately 2 mm x 10 mm.
  - ◆ Because reliability of the cooling tubes is essential, a long-term (6+ month) test of both types of cooling tubes setup by SiDet, common to both projects
    - Sub-atmospheric system
    - Ethylene-glycol cooling
- ...





# Tests Planned

- Mechanical stave will be built by Lehman Review
  - ◆ Will use dummy silicon (or CDF sensors)
  - ◆ Design of fixtures for module building far advanced
- Schedule calls for building electrical grade OL modules when sensors are available
  - ◆ We have already our first electrical grade module for Layer 1
  - ◆ Electrically, modules for Layers 2-5 are very similar
  - ◆ The basic readout unit is a readout module with a stave having four independent readout modules
- Electrical grade OL module production early next year, is immediately followed by stave prototyping on 3/6/03 with an electrical stave fully functional by 6/11/03
- Stave is then submitted to two readout functionality tests
  - ◆ Vertical Slice Integration test
    - Readout system identical to the readout in the experiment: Adapter Card, Interface Board, Sequencer, Sequencer Controller, VTM, VRB, VRB Controller, SBC, Level 3, offline
  - ◆ Stand-Alone Sequencer system
    - Used for burn-in of modules





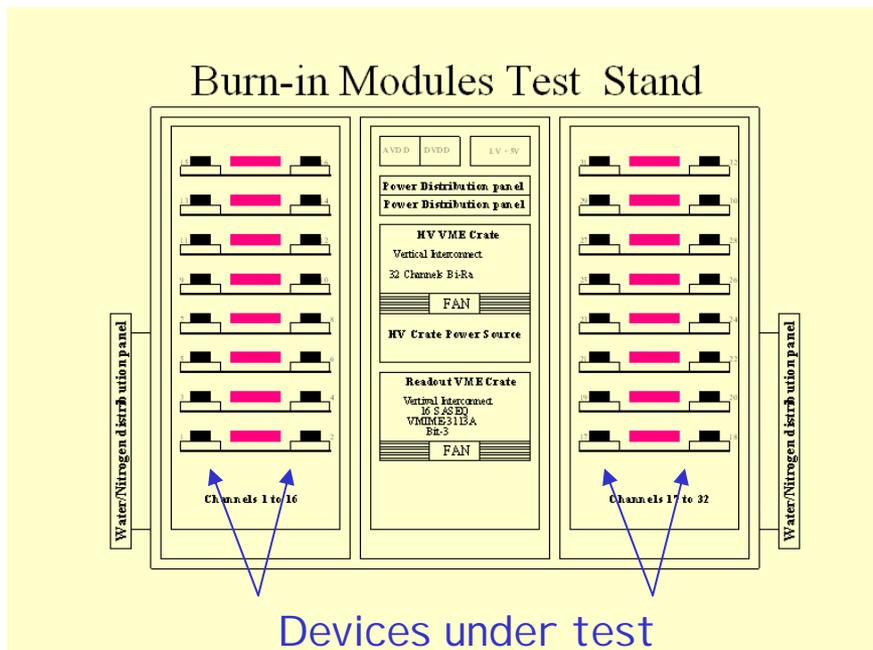
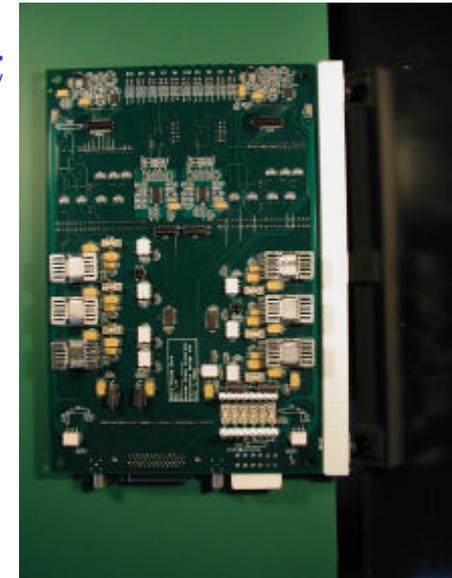
# Vertical Slice Tests

- Readout System at SiDet identical to the readout system used in the experiment; two systems will be erected:
- "1% Test"
  - ◆ For functionality test of individual components up to a total of 8
  - ◆ Will reside in burn-in area at SiDet; operational October '02
- "10% Test"
  - ◆ For functionality test of multiple components; operational spring '03
  - ◆ Will reside in the Lab C clean room as was done in Run I I a
  - ◆ Tests scheduled
    - Sector test of Layer 0
      - $3 \times 6 = 18$  hybrids, i.e. 3  $\phi$ -sectors; study noise with analogue cables
    - Sector test of Layer 1
      - $3 \times 6 = 18$  hybrids, i.e. 3  $\phi$ -sectors; study and monitor operating conditions
    - Full sector test
      - Minimum of 5 full staves readout, i.e. 20 hybrids
      - Combination of Layer 0, Layer 1 and Staves
- The 1% test is currently being setup at SiDet to study the SVX4 chip with the full readout system



# Burn-in and Purple Card

- Burn-in is performed with stand-alone sequencer system; UIC responsible for setup and running
  - ◆ The equivalent of the Adapter Card is a Purple Card
- Purple Card designed by KSU
  - ◆ Uses same components and schematic solutions as AC
  - ◆ Each card has 2 channels
  - ◆ 12 boards fabricated, (3) (being) stuffed, 2<sup>nd</sup> proto. Sept.
  - ◆ Note: L1 hybrid + readout module used this card



- Test stands for testing first components being setup at SiDet
  - ◆ Two hybrid burn-in test stands, 16 channels each
  - ◆ Two module burn-in test stands, 32 modules each
    - with associated cooling
  - ◆ Two burn-in cycles per week



# Production

- The detector is of significant size

- ◆ Sensors: 2184; Si area of 8.3 m<sup>2</sup>
- ◆ 888 hybrids, i.e readout cables
- ◆ 7440 SVX4 chips

- To build:

- ◆ 553 20cm gangs
- ◆ 888 modules
- ◆ 168 staves
- ◆ L0/1 assembly and mating
- ◆ L2-5 barrel assembly
- ◆ Inner + Outer barrel mating

- Plus the yield and spares

- Assumptions:

- ◆ Yield of 85% in module production + ~5% spares on the shelf
- ◆ Yield of 95% in stave assembly + 4 spares each of L2-3 and 4 L4-5 staves

	# Staves	# 10-10 Modules		# 10-20 Modules		# 20-20 Modules		Total # Modules
		A	S	A	S	A	S	
Orientation								
Layer 0								144
Layer 1								72
Layer 2	24	24	24	24	24			96
Layer 3	36	36	36	36	36			144
Layer 4	48	48	48			48	48	192
Layer 5	60	60	60			60	60	240
<b>Total L2-5</b>	<b>168</b>	<b>168</b>	<b>168</b>	<b>60</b>	<b>60</b>	<b>108</b>	<b>108</b>	<b>672</b>
<b>Total</b>								<b>888</b>



# Production Choreography

- Study the use of all available equipment during production and assembly
  - ◆ 9 CMM's available to the project at SiDet

	Date	8/4/03	11/17/03	1/26/04	3/29/04	7/19/04	5/30/05
Lab D	Z500 #1						
	Z500 #2						
	Z500 #3	20-20 gangs	20-20 gangs		OL modules	OL modules	
	Z500 #4						
	Z850-D						
Lab C	Z500-C			Layer 1 modules			
	LK				Layer 0/1 South	Layer 0/1 North	South
	B&S					Staves South	Staves North
	Z850-C					Staves South	Staves North

- Each cell corresponds to one week; breaks in production lines should not be interpreted as slack
- Production choreography is well understood. Exercise was very beneficial to understand full production line schedule.



# Summary and Conclusions

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- A lean and robust Silicon Tracker has been designed to pursue the physics goals for Run II b
- Project has already a fully working electrical module with SVX4 readout
- Project has prototyped all major components of the design (except LO hybrids and sensors) and nearly all meet our specifications
- Project has a strong technical team with a tight grip on all technical issues
- All L3 managers have a thorough understanding of the critical issues and the effort involved to succeed with this project; most are Run II a veterans
- Many university groups involved, all with clearly delineated responsibilities
- We are on the verge of moving beyond the prototyping stage