

## **D0 Responses to Questions from the Physics Advisory Committee**

June 4, 2002

Assembled on this web site are the responses to the questions posed to the D0 Experiment by the Physics Advisory Committee for discussion at their June meeting in Aspen. In addition to addressing the questions specifically targeted to the Run 2b silicon, trigger, and online upgrades, we have included a [brief status report on the Run 2a detector and trigger systems](#), accessible as a separate link on this web page. We note that our response to question 5 consists of a [summary report on our studies of the Silicon Track Trigger](#), which we include as a separate link on this page as well.

The Collaboration would like to take this opportunity to thank the Committee for their help and guidance as the experiment prepares its plan for extended running at the Tevatron. Present and projected budgetary constraints, coupled with the contracted time scales associated with Run 2b, put additional pressure on all of us as such new initiatives are considered. In recognition of this, we continue to work internally, as well as with the Laboratory and the CDF Experiment, to look for opportunities by which the resources required for mounting the Run 2b upgrade might best be contained. Our recent progress on this and many other fronts is summarized in the responses presented here.

### **Question 1: Overview of high-level project milestones.**

Our current schedules contain a total of approximately 135 milestones for the silicon project and 37 milestones for the trigger and online projects. Presented on the following pages are the 52 higher-level milestones that we have extracted for the silicon, and the 16 analogous ones for the Level 1 and Level 2 trigger projects and the online upgrade. We include these milestones in time-ordered form in tables and, to elucidate how these milestones are distributed in time, in Gantt form as well.

<b>Silicon Higher-Level Milestones</b>	<b>Date</b>
CD-0 Approve Mission Need	5/11/01
CD-1 Approve Preliminary Baseline Range	8/30/02
CD-3a Start Limited Construction	8/30/02
CD-2 Approve Baseline	10/28/02
CD-3b Continue Construction	10/28/02
L0 Hybrids Released For Production	3/12/03
L0 Flex Cables Released For Production	3/12/03
L2-L5 Sensors Released For Production	3/18/03
L1 Sensors Released For Production	3/31/03
SVX4 Released For Production	5/2/03
L1 Hybrids Released For Production	6/16/03
L2-L5 Hybrids Released For Production	7/18/03
L0 Flex Cable Production And Testing Complete	7/18/03
L0 Sensors Released For Production	9/25/03
Successful readout of full stave	9/29/03
All L1 Sensors Delivered And Tested	11/13/03
Beam Tube Accepted	1/21/04
L2-5 (10/10 South Axial) Module Production Begun	2/5/04
L1 Module Production Begun	2/26/04
L1 Hybrid Testing Complete	3/10/04
L0 Module Production Begun	3/12/04
All SVX4 Chips Produced And Tested	3/31/04
L0 Hybrid Testing Complete	4/28/04
All L0 Sensors Delivered And Tested	5/20/04
L1 Module Production Complete	5/27/04
L2-L5 Hybrid Testing Complete	7/1/04
L1 South Complete	7/6/04
L0 Module Production Complete	7/12/04
All L2-L5 Sensors Delivered And Tested	7/13/04
L1 Module Testing Complete	7/13/04

<b>Silicon Higher-Level Milestones</b>	<b>Date</b>
L0 South Complete	8/3/04
South Staves Complete	8/18/04
L0 Module Testing Complete	8/24/04
L0-L1 South Complete	8/24/04
L2-5 (10/10 North Stereo) Production Complete	9/3/04
Successful readout of multiple staves with all final components	9/23/04
L2-5 (10/10 North Stereo) Module Testing Complete	10/5/04
Layer 2-5 South Complete	10/14/04
South Silicon Complete	12/10/04
North Staves Complete	12/20/04
L0 North Complete	2/9/05
L1 North Complete	2/10/05
Layer 2-5 North Complete	2/22/05
L0-L1 North Complete	2/24/05
Shutdown for Installation Begins	4/4/05
North Silicon Complete	4/18/05
Downstream Readout Ready	5/27/05
Silicon Ready To Move To DAB	6/21/05
Detector Installed In Fiber Tracker	7/8/05
Ready To Begin Cabling And Commissioning Detector	8/24/05
Ready For Beam	11/17/05
CD-4 Start Operations (Proposed)	11/21/06

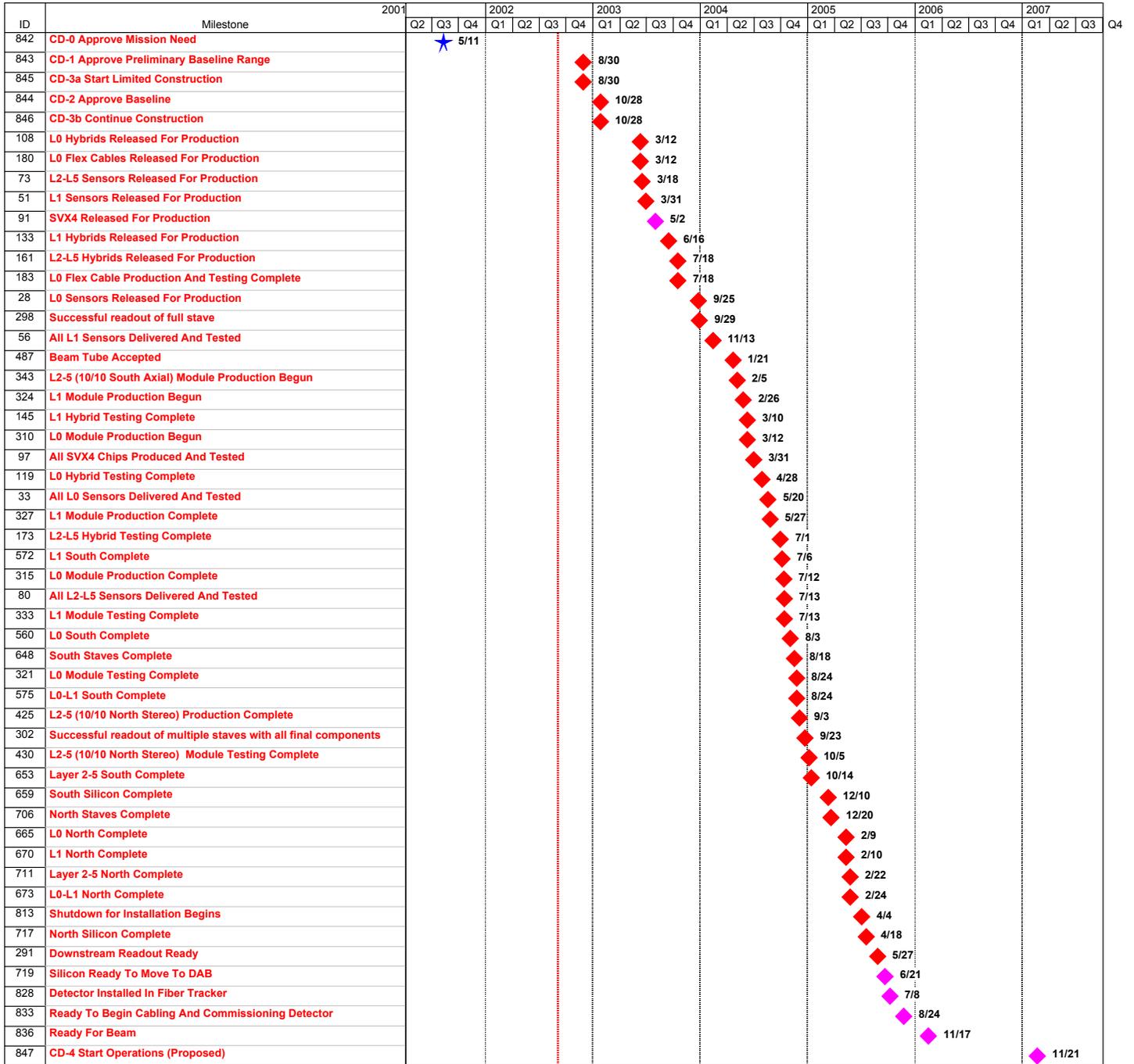
<b>Level 1 Trigger Higher-Level Milestones</b>	<b>Date</b>
L1 Cal ADF+Crate Prototype Complete	2/13/03
L1 Cal TAB/GAB Prototype Complete	4/18/03
L1 Cal/Track Match Production and Testing Completed	8/20/03
L1 Cal TAB/GAB Production Complete And Tested	6/17/04
L1 Cal ADF Production Complete And Tested	10/18/04
L1 Cal Production And Testing Complete	10/18/04

L1 CTT DFEA Production And Testing Complete	11/3/04
L1 Cal Trigger Installation Complete	7/5/05

<b>Level 2 Trigger Higher-Level Milestones</b>	<b>Date</b>
Begin Silicon Track Trigger Run 2b PCB Production	9/30/02
Level 2 Beta Prototype Testing Complete	8/27/04
Level 2 Beta Production Complete	1/21/05
Level 2 Beta Installed And Commissioned	2/18/05
Silicon Track Trigger Operational	8/9/05

<b>Online Milestones</b>	<b>Date</b>
New Disk System Array Commissioned	2/13/04
Primary File Server Commissioned	2/2/05
Production ORACLE System Commissioned	5/25/05

## Silicon Higher-Level Milestones



### Level 1 Trigger Higher-Level Milestones

ID	Milestone	2001				2002				2003				2004				2005				2006				2007						
		Q4	Q1	Q2	Q3																											
31	L1 Cal ADF+Crate Prototype Complete																															
56	L1 Cal TAB/GAB Prototype Complete																															
109	L1 Cal/Track Match Production and Testing Completed																															
59	L1 Cal TAB/GAB Production Complete And Tested																															
21	L1 Cal ADF Production Complete And Tested																															
66	L1 Cal Production And Testing Complete																															
141	L1 CTT DFEA Production And Testing Complete																															
74	L1 Cal Trigger Installation Complete																															

### Level 2 Trigger Higher-Level Milestones

ID	Milestone	2001				2002				2003				2004				2005				2006				2007						
		Q4	Q1	Q2	Q3																											
32	Begin Silicon Track Trigger Run 2b PCB Production																															
17	Level 2 Beta Prototype Testing Complete																															
24	Level 2 Beta Production Complete																															
29	Level 2 Beta Installed And Commissioned																															
114	Silicon Track Trigger Operational																															

### Online/DAQ Milestones

ID	Milestone	2001				2002				2003				2004				2005				2006				2007						
		Q4	Q1	Q2	Q3																											
86	New Disk System Array Commissioned																															
128	Primary File Server Commissioned																															
117	Production ORACLE System Commissioned																															

### **Question 2: Progress with respect to plans and milestones presented at the November 2001 PAC.**

After discussions with both the outgoing and incoming PAC chairmen, it was agreed that our response to this question should focus on our progress with respect to the schedule presented at the April 16-18, 2002 Temple Review. Most of the activities associated with the Run 2b Level 2 trigger (Silicon Track Trigger and Level 2 $\beta$  upgrade) and online upgrades are well in the future; we therefore present below progress reports only on the Run 2b silicon and Level 1 trigger systems. We also include status reports on the Level 2 $\beta$  trigger system for Run 2a and the SIFT chip replacement project, the latter required for 132 nsec running. We note that progress on the current data acquisition system and the Run 2a trigger systems is presented as a separate document on this web page.

- **Run 2b Silicon**

Substantial progress has been made on the silicon detector. We have successfully pushed a number of items through the phase associated with the procurement of prototype items. Unfortunately, this has exposed some shortcomings in the procurement process that have resulted in delays. This is probably unavoidable during the ramp-up of a project and we are working with the Laboratory to take steps to speed procurement, such as adding a dedicated expeditor. We have recently “statussed” the full Run 2b schedule, including the silicon portion. We summarize the status of the sub-project in the following paragraphs. While some items are ahead of schedule, others have slipped. Even though the project is not yet baselined, we take this seriously, and the relative maturity of our project tools has proved useful in identifying such problems at this early stage, when we can take steps to address them, as described below.

Since the Temple Review the biggest setback has been the delivery of the SVX4 chip. MOSIS has changed the delivery date for the TSMC run from May 23 to June 11, a delay of three weeks. Since the SVX4 chip defines the critical path, it has resulted in a three week overall slip in the schedule.

Two vendors are being pursued for the Layer 1 sensors, Hamamatsu in Japan, and ELMA in Russia. Procurement of the Hamamatsu sensors took longer than expected, for a variety of reasons. The order was placed in April and delivery is expected in September, about four weeks late. We expect the sensors from ELMA to be delivered to Fermilab during the month of June. Our schedule has delivery in early August, so we are a few weeks ahead of the schedule here. This item is not on the critical path.

Only Hamamatsu is being considered as vendor for the outer layer sensors. We are currently involved in what we expect to be the final discussions on exact specifications of the sensors before they will start production. This will result in delivery of pre-production sensors in October, approximately one month behind schedule. The collaboration was able to secure a sensor quote directly from Hamamatsu through the University of Tokyo. This had price advantages but Fermilab procurement felt that a new quotation was needed, which introduced the delay.

Substantial progress has been made on all parts of the readout electronics. The Layer 1 hybrids were ordered in February from CPT in Oceanside, California. Delivery was ahead of schedule. The hybrids were distributed to the various institutions to exercise their testing equipment. All possible mechanical and electrical tests have been run on these hybrids and they meet our specifications. We are currently waiting for the SVX4 chips to continue the testing.

The hybrids for the outer layers come in both axial and stereo versions. Axial hybrids have been ordered from Amitron in North Andover, Massachusetts and are expected back in July. This is about 4 weeks behind schedule, owing to our decision to implement a fingerless design to make the hybrids simpler. A second set of hybrids is also being ordered from CPT.

Progress on the technically challenging analog cables has been quite good, and we are currently ahead of schedule. We ordered the first set of prototype analog cables in July 2001 from Dyconex in Zurich, Switzerland, using the same design as the CDF Layer 00 cables. These cables did not meet our specifications and the design was changed to use a stack of two separate cables, each with a trace pitch of 100 $\mu$ m. The order for this second prototype was placed in February of this year and the prototypes were received in April. The prototypes meet our specifications. A prototype of the actual sensor, analog cable and hybrid assembly was made, assuring that the assembly will not present any problems. A second vendor, Compunetics, is now being qualified.

Development of the digital jumper cables is also ahead of schedule. The first set of prototypes was ordered from Honeywell in February of this year and the first cables were received in April, well ahead of the June schedule date. The cables meet all our specifications. A second vendor, Basic Electronics, is also being qualified. Cables from this vendor are in hand and are currently being tested.

The design of the junction cards was completed on schedule in March. Prototypes are in hand and were received in May, about a month ahead of schedule. Tests are being carried out with as many components of the final system as possible.

Twisted pair cables connect the junction card to the adapter card. The design of the cable is complete. The procurement, however, will slip by about 6 weeks. This is due to long lead times for the various parts.

The design of the adapter card is complete and has been submitted for production. The design of this card took a bit longer than anticipated, incurring a delay of a few weeks. Boards are expected in early July.

The work on the test stands is progressing well. The order for the additional sixty Stand-Alone Sequencers (SASEQs) has been submitted. This order was held up in the procurement office for more than two months. It is funded both by NSF MRI funds and Fermilab funds and the system was unable to handle this with the needed expediency. The sequencers are now scheduled to arrive at Fermilab in early August. This is a two-month delay with respect to the original schedule. We consider such delays to be unacceptable, although we note that this particular item does not impact the progress of the project in any way. We currently have about fifty Stand-Alone Sequencers, which can and will be used to test the first hybrids that we will receive. These additional sequencers are for the burn-in of hybrids and modules, which will not take place until fall of next year. We ordered these items now because it was a follow-on order to Run 2a components.

The design of the 'Purple Card', which is a test card for the testing of hybrids, is complete. We expect to have the boards in hand ahead of schedule.

The high voltage system for the silicon Run 2b project is being ordered by our Mexican collaborators. We expect the order to be placed within the next month, which is about one year ahead of schedule. Again, this is a duplicate of the system employed for the Run 2a silicon detector, so we can aggressively purchase early in the project.

Design of the structural support for Layers 0 and 1 is being developed in collaboration between the University of Washington and Fermilab, and is proceeding on schedule. Stave design and module fixturing is progressing as well. In order to insure that we make a properly informed decision, the choice of cooling channel technology has been deferred until accelerated aging studies can be completed. These tests are currently being prepared. The stave design and fixturing for stave assembly is proceeding, leaving open sufficient options to allow the accommodation of either cooling channel option.

- **Run 2b Level 1 Trigger, Other Upgrades**

**Level 1 Trigger:** Most of the work associated with the Level 1 trigger upgrade between now and this coming fall is related to prototype and algorithm design. Significant progress continues to be made. We summarize the status below.

For the Level 1 calorimeter trigger (L1Cal), we have designed an active splitter which will allow the new ADC/Digital Filter (ADF) prototypes to be tested *in situ* at DØ in a transparent manner, allowing data taking to continue as the tests are performed. The design for the splitters is complete, including a simulation in SPICE, and they are on track for installation during the October 2002 shutdown. Several possible mechanical layouts for the ADF crates have been investigated, with a preferred solution chosen. This consists of housing the ADF cards in a standard 6u VME crate, with the input cables fed through a transition backplane. The firmware design for one channel of the ADF is 80% complete. The effect of the size of the so-called “Regions of Interest” (RoIs), trigger tower clusters that are used to locate local energy deposition maxima, has been extensively studied in simulations of candidate algorithms for the Trigger Algorithm Board (TAB). Preliminary results suggest that an RoI consisting of 2X2 trigger towers is preferred. Preliminary specifications, based on ongoing simulations, are being developed for the output data format from the TAB/Global Algorithm Board (GAB) system to both the Level 2 trigger and the calorimeter/track match system.

Three algorithms are being studied in parallel in some detail for the Level 1 Central Track Trigger (CTT). The equation-based approach, as outlined in the Trigger TDR, utilizes different schemes for the various layers, depending on the  $p_T$  bin in question. The highest  $p_T$  bin utilizes the full complement of 16 singlets in order to maximize efficiency; the lowest  $p_T$  bins use a combination of singlets and doublets in the trigger. The remaining two algorithms being considered use a dynamic road equation for computational logic. These algorithms rely on the speed of the XC2V series of FPGAs for dynamically building the road in order to keep the processing time within the required time window. One of these schemes has been implemented in VHDL and simulated using the FPGA resource simulation tools. Preparations are underway to fully implement the other option as well. Our goal is to implement all three algorithms, comparing the

FPGA resources needed for each, as well as the speed of the algorithms using the FPGA simulation tools. Preliminary indications are that all of these algorithms will be able to be accommodated by the XC2V series FPGAs. In addition, a comparison of rejections and efficiencies for all three of the schemes is presently being carried out using the full trigger simulation. We are using events with 4 to 7.5 overlaid minimum bias Monte Carlo events for these studies. We will use a combination of information in order to select the best algorithm to pursue, including the matrix of efficiency vs. rejection, the processing speed, and the FPGA resources required.

**Other upgrades:** All of the tasks associated with the Level 2 $\beta$  and Level 2 STT upgrades are designed to exploit continually evolving enhancements in technology (processing power, etc.), and therefore occur in the future. In order to piggy-back on current Run 2a STT board production and other procurements, the STT upgrade requires some Run 2b-related purchases to be made during the summer. We are on schedule for these procurements. The online upgrade is also proceeding on schedule. Recent tasks associated with evaluations of the rate and other capabilities of the online LINUX system, as well as those for online and DAQ network switching, have occurred on schedule. There has been no observable slippage in any Run 2b-associated online activities.

- **Run 2a Level 2 $\beta$  system**

The Level 2 $\beta$  system has made very demonstrable and steady technical progress during this calendar year. The prototypes have been in hand since March, and have undergone extensive testing at Orsay, the University of Maryland, and the University of Virginia. Modifications required for the next pre-production cycle have recently been certified, and we anticipate pre-production boards that integrate these changes to be in hand for testing by mid-summer.

All I/O functionality of the boards has been successfully verified on the prototypes, and proper integration with the TTL-modified  $\alpha$ -processors and Magic Bus Transfer signals has been achieved. We have also verified what has been measured to be the vastly improved Direct Access Memory (DMA) performance of the Level 2 $\beta$  boards over their Level 2 $\alpha$  counterparts, critical for the additional bandwidth-handling capability of the  $\beta$ -system.

Software and firmware work remains to be completed before Level 2 $\beta$  boards can begin to be integrated into the trigger. Added attention to these efforts in recent months has provided substantial impetus here: we expect that these elements will be ready in about two months, coinciding with the delivery of the pre-production boards. The  $\beta$ -system has been designed to allow integration into the  $\alpha$ -system in a transparent manner, so as not to interrupt physics data taking. All indications to date are that this will be achievable. Preparations are underway to begin integration of the production Level 2 $\beta$  boards in the fall of this year. The overall project has slipped approximately two months since the November 2001 PAC meeting, due to the 8 week delay in the delivery of the prototype boards early this calendar year. The project has continued to hold to its schedule since that time.

- **SIFT replacement**

The SIFT replacement chip was submitted for fabrication along with the SVX4 submission in early April, with parts due back in early June. The joint SVX4-SIFT submission resulted in significant cost savings (potentially, \$200k), as it obviated the need for a separate production run for the SIFT. The chip designer simulated the chip quite extensively prior to submission with excellent results, raising expectations that this initial part will be fully functional. The need for an additional production run will be determined after this initial submission, and will depend on the chip functionality and the manufacturing yield.

The hardware for chip testing has been fabricated, and awaits the arrival of the first production run of chips. A small printed circuit board has been built to emulate a Multi-Chip Module (MCM) on which the SIFT chip is mounted, and a prototype Analog Front End (AFE) board has been modified to accept this PC board.

Our baseline plan consists of a full AFE replacement, placing packaged AFE SIFT replacement chips directly on the board. We continue to consider a backup option, which consists of building small PC boards that will emulate the existing MCMs, which will in turn be replaced on the existing AFE boards. While the latter introduces some technical risk, it obviates the need for a production run of a new, albeit far simpler, AFE board. The cost of these two options is nearly identical. The best path will depend greatly on the ability of either package to provide an adequate analog ground so that the noise requirements of the CFT trigger system can be met. The performance of the grounding in the baseline case will be determined after fabrication of AFE prototypes this summer. The risks associated with MCM replacement are being studied now; the grounding properties of this option will be studied during the summer.

**Question 3: Dates for decision to implement/descope trigger modifications.**

We have performed extensive simulation studies of the proposed Level 1 calorimeter and tracking trigger upgrades, and the major findings of these studies were presented at the April 2002 PAC meeting. Further details can be found in the D0 Run 2b Trigger and Online Upgrade Technical Design Report, which can be accessed electronically on the web site for the April 2002 Director's Review of the Run 2b Projects (see link on this page). The major open question following the April meeting was the needed scope of the Silicon Track Trigger upgrade, which we address in our response to question 5.

**Question 4: Report on cost-reduction/simplification efforts for silicon detectors.**

The design of the silicon detector as presented at the April PAC meeting had been quite stable, particularly with regard to major design decisions for the previous year. Much effort had already gone into minimizing the number of components. The physics performance of the detector, however, places clear requirements on the design. We have documented for the previous PAC meeting the effect of various scope reduction options

on the silicon detector (fewer layers, reduced length in  $|z|$ ). All of these options were shown to significantly reduce the physics reach for the Higgs boson.

The CDF and DØ designs for Run 2B use a similar number of sensors (2304 for CDF and 2184 for DØ) and cover similar volumes. The use of a common readout chip, SVX4, is definitely the best strategy to take given the boundary conditions that exist for both projects. In addition, given the financial and schedule constraints, it is best to retain as much of the existing readout infrastructure as possible for each of the two experiments. This last point has significant implications for the design, because it implies that DØ will operate the SVX4 chip in SVX2 mode, which incurs dead time. DØ is thus not in a position to daisy chain many readouts as CDF plans to do. This means that DØ will unavoidably need to employ a larger number of readouts than CDF.

Given these constraints, we believe our design is about as lean as could be conceived. Consequently, the efforts of the DØ silicon group have focused on minimizing the cost of the individual components in the system.

On advice from the Technical Review Committee, the silicon group has aggressively pursued a purchase of silicon sensors directly from Hamamatsu. With the help of an initial contact at the University of Tokyo, we were able to obtain a quote for a direct purchase of sensors from Hamamatsu at a substantially lower cost. The silicon project is looking at a cost savings of about \$400,000 compared to their initial estimate for sensor procurement.

The group has also vigorously pursued sources for high quality analog cables. The initial attempt was to obtain cables similar in layout to the CDF layer 00 cables from Dyconex, located in Zurich, Switzerland. To our knowledge, this is the only commercial company able to deliver cables with this particular layout that would meet our specifications. The initial batch of cables was unsatisfactory and a new design was conceived. This new, simpler - and thus less costly - layout of the cables has been submitted to two vendors, Dyconex and Compunetics, in Pennsylvania. Dyconex has already delivered cables that meet all our specifications. Studies on noise performance are in progress. We are optimistic that our current design will have acceptable noise characteristics.

The hybrid design was modified and now can be built using the silk-screening process. This allows for the use of larger vias, and a higher production yield. This has also opened up the possibility to use multiple vendors and has reduced the cost.

The collaboration has maintained an ongoing dialogue with CDF and the Silicon Task Force to allow use of common techniques. Through these efforts, and in close collaboration with the Fermilab Particle Physics Division, we are trying to achieve the most efficient way of using the labor resources available. For example, fixtures for module assembly are being developed in open communication with both collaborations so that duplicate efforts are minimized. Another example is the setup of a long-term cooling test, which is carried out in collaboration with CDF. Currently, DØ foresees using the exact same sensors as CDF for the innermost layer. A common purchase is

being pursued. In addition, there has been an initial discussion between the DØ and CDF silicon groups to explore the possibility of DØ producing the layer 0 support structure for the CDF silicon detector. We are continuously exploring ways to reduce both component and labor cost.

**Question 5: D0: Detailed evaluation of Silicon Track Trigger update options.**

Please see the relevant link on this web page.