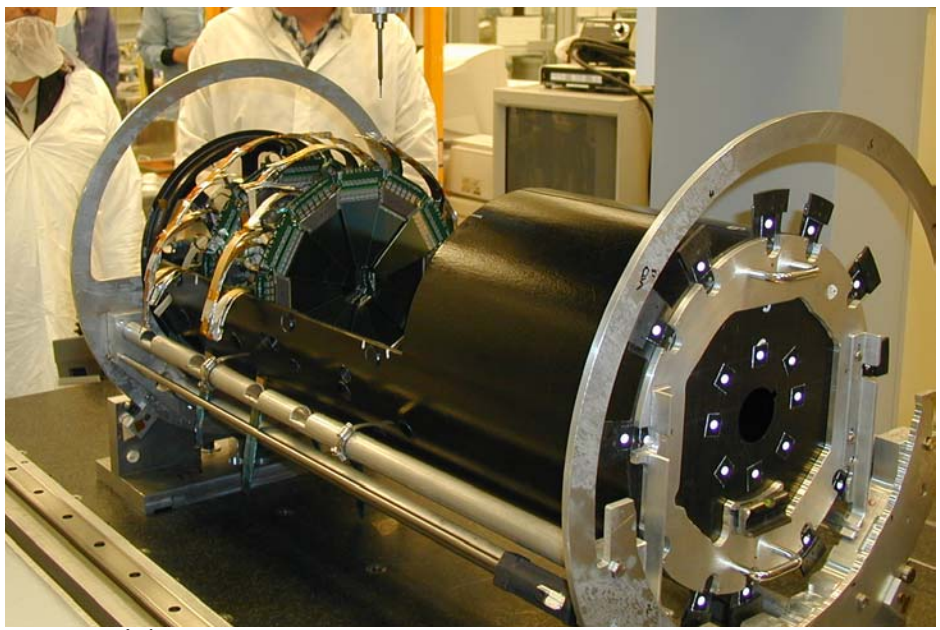
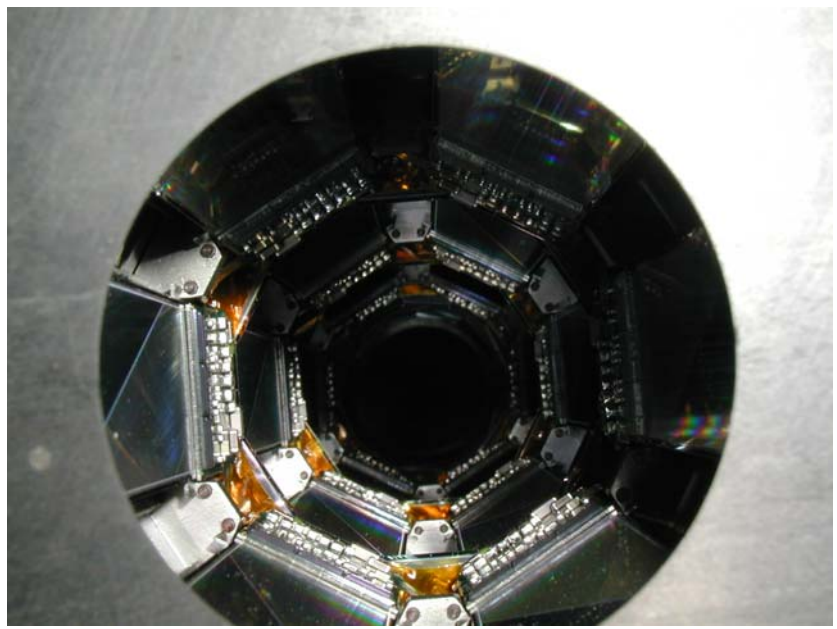
Layer 0 Proposal

Dzero proposes to install a detector inside the current inner layer. This detector will

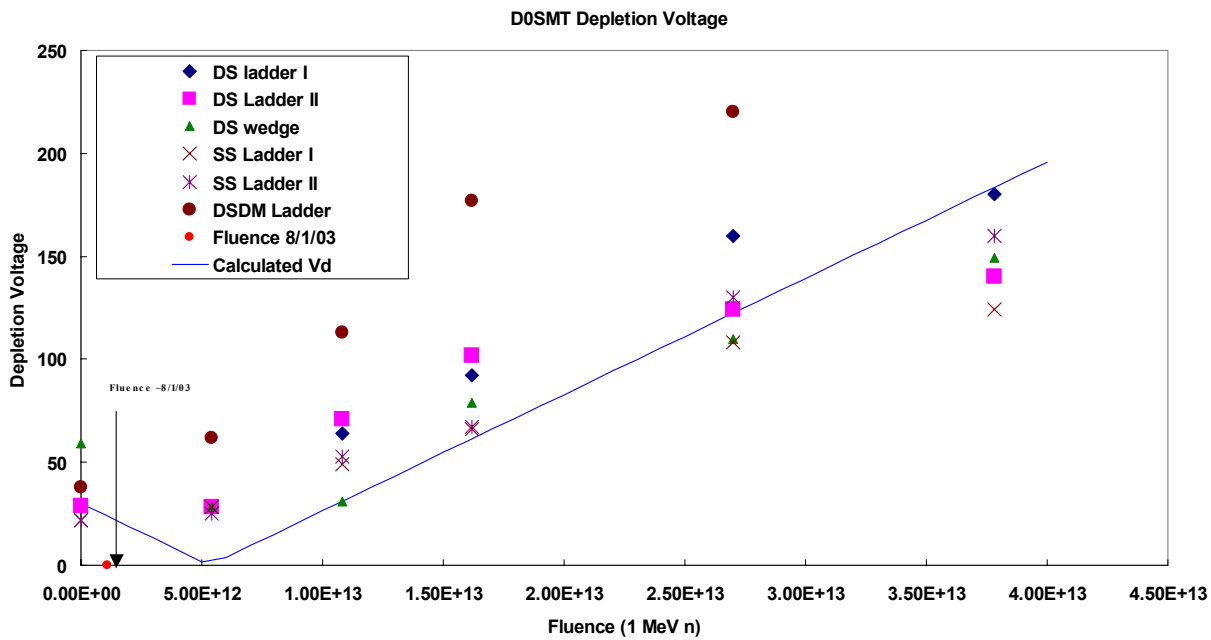
- Mitigate tracking losses due to radiation damage and detector failure
- Provide more robust tracking and pattern recognition for higher luminosities
- Provide better impact parameter resolution





Layer 0 Motivation

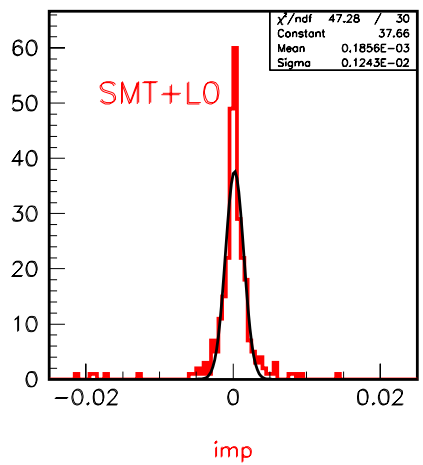
- We expect layer 1 Micron sensors to begin to fail at exposures of ~ 3-4 fb-1
- We are seeing continuing failures of readouts in the current detector (85% currently good)
  - Hard failures due to interior shorts/opens (1%)
  - SVX chip failures, readout problems (7%)
  - Bias or HV failures (1%)
  - Unstable HDIs – marginal timing and signal quality (6%) – many recoverable?
- Increased occupancy with higher luminosity, uneven TEV loading.

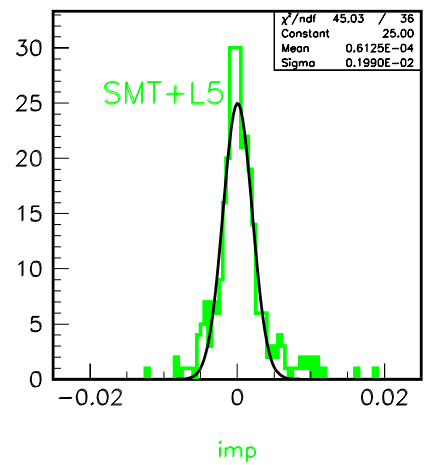


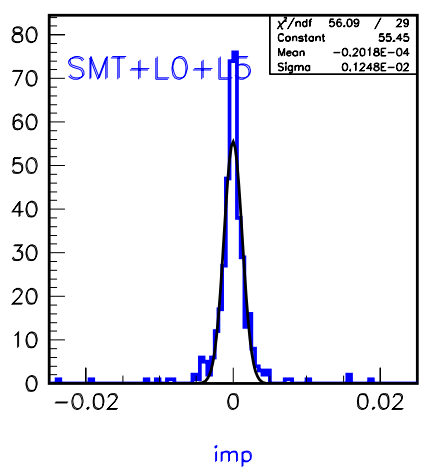
Ronald Lipton

Layer 0 Physics Motivation

Results from early Run2b design studies: Impact parameter resolution:top events







- SMT+ L0:
  $\sigma(IP) = 12.4\ \mu$
- SMT+ outer layer
  $\sigma(IP) = 20.0\ \mu$
- SMT + L0 + outer layer
  $\sigma(IP) = 12.5\ \mu$

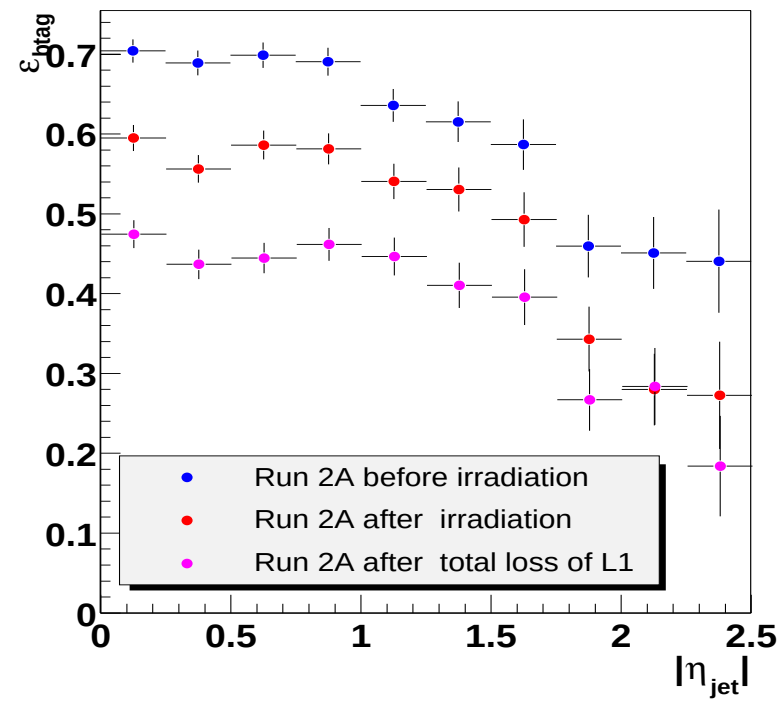
b-tagging efficiency per jet

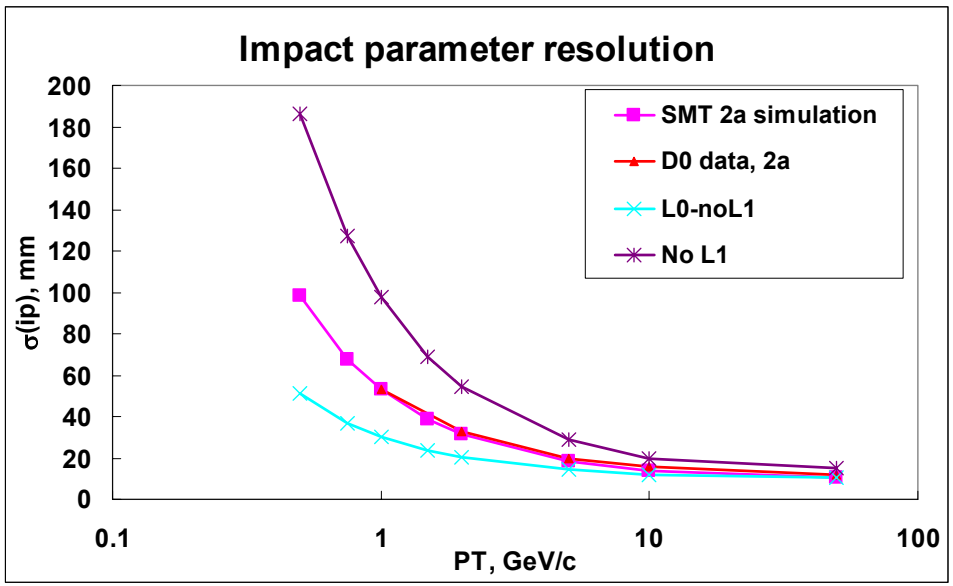
	L0	L5	L0+L5
ε	47%	41%	48%

Relative increase of b-tagging efficiency is 15%

Layer 0 Motivation

- "after irradiation" effect:
  a) 10% hits are lost in outer layers
  b) 50% hit loss in L1 and F-disks
- "total loss" – a) + 100% hit loss in L1 and 50% in F-disks
- Different (improved tagging algorithm)

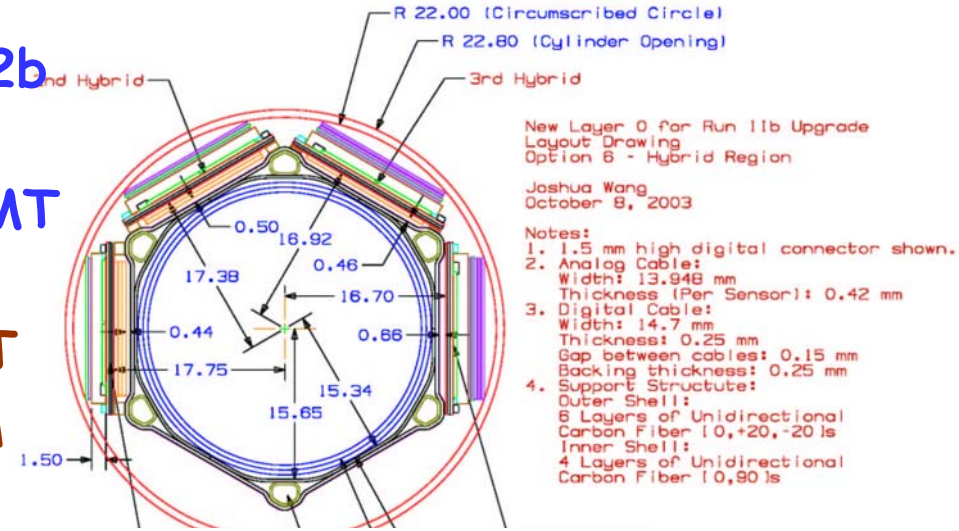


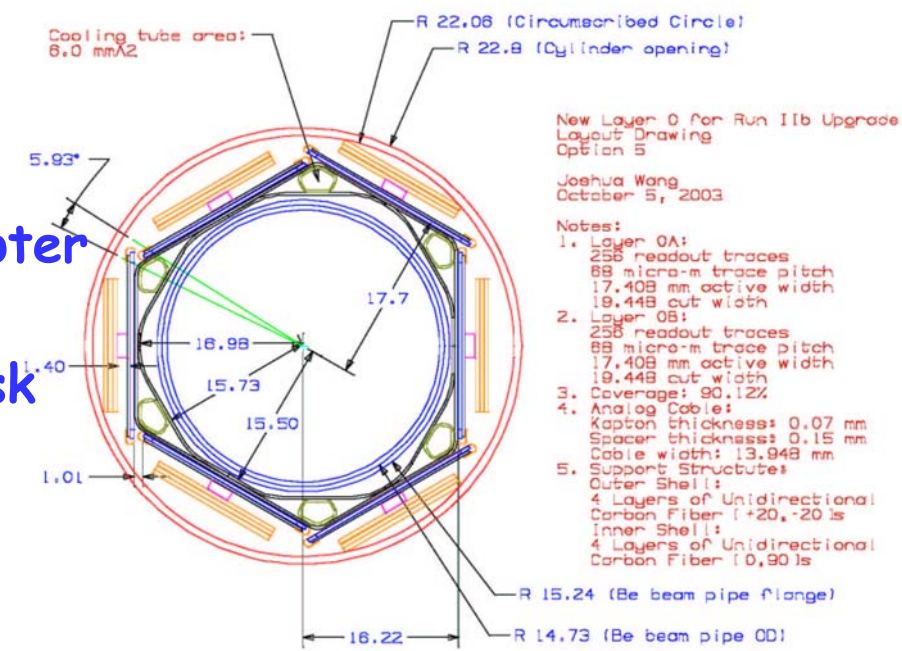


- **Improvement in IP resolution, especially at low momentum due to analog cables**

Layer 0 Design

- Design – use as much of the Run2b R&D as possible
- Detector must fit in 22.8 mm SMT support structure opening
  - Six phi segments – match STT
  - Eight z segments 2x7,2x12cm
  - Analog cables – low mass
  - 48 HDIs x 256 channels
  - SVX4 chips (96)
- Use 2b Hybrids
- Use 2a infrastructure (new adapter cards)
- Replace at least one outer H disk

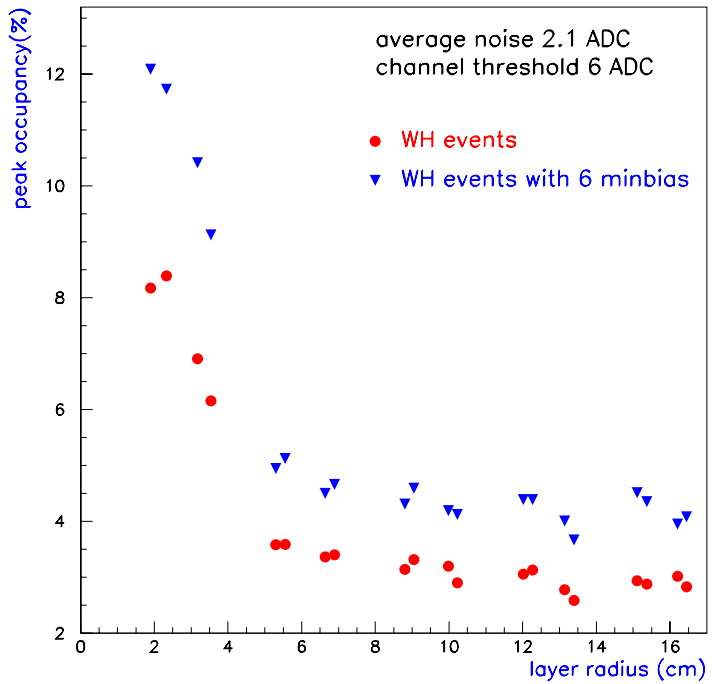




Layer 0 Performance

- Shorter than 2b detector- matches 2a
- Good signal/noise with shorter analog cables, detectors ~15:1
- Larger range of incident angles
  - Wide, small signal clusters
  - Minimum s/n = 6.7
- WH + 0 mb events: 7.0% shared clusters in L0
- WH + 7.5 mb events: 7.5% shared clusters in L0

	Z1	Z2	Z3	Z4
Detector length (cm)	7	7	12	12
Strip pitch (microns)	73	73	73	73
Active width (mm)	18.69	18.69	18.69	18.69
Radius (inner)	16.43	16.43	16.43	16.43
Max angle (radians)	0.52	0.52	0.52	0.52
L, effective (microns)	147.67	147.67	147.67	147.67
Analog cable length (cm	36	34	27	20
Total capacitance (pf)	21	20.3	23.85	21.4
Total noise(electrons)	1445	1414	1573	1463
S/N (normal inc)	15.9	16.3	14.6	15.7
S/N (edge)	7.3	7.5	6.7	7.3



Ronald Lipton

Layer 0 Status

COMPRESSED SCHEDULE:

Sept 25 – Design Workshop

Oct 9/10 – Presentation to collaboration/IB

Oct 14 – PMG review of L0 submit design document:

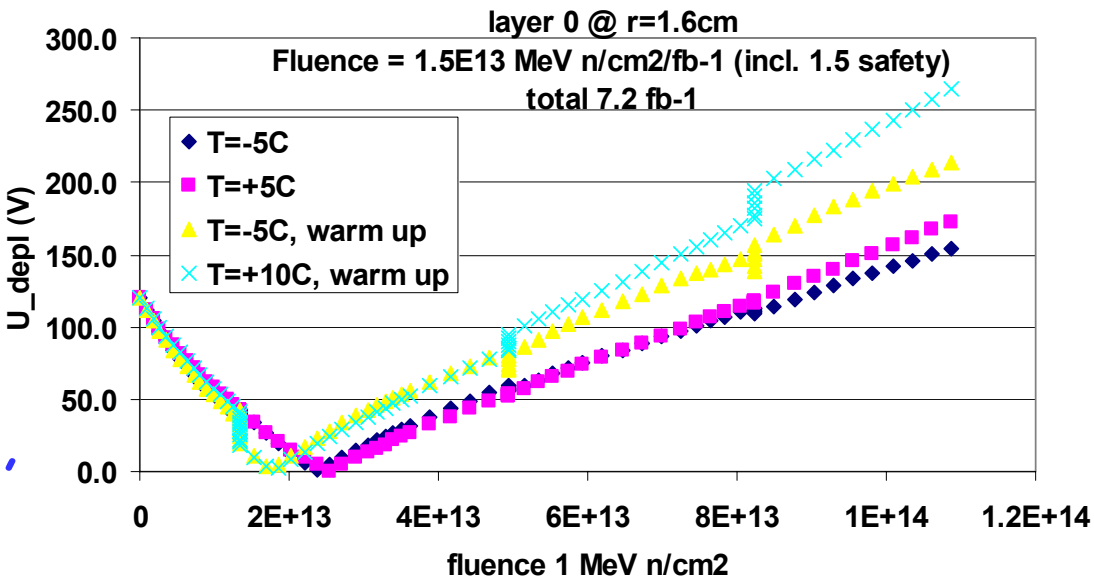
> "… provide a document that includes the motivation for layer 0, the design concept, some demonstration of the effectiveness, a first cost estimate and schedule, the feasibility of the installation plan, and a consideration of the risks. To make sure we are able to move through this process expeditiously, we would like such a document by about mid-October."

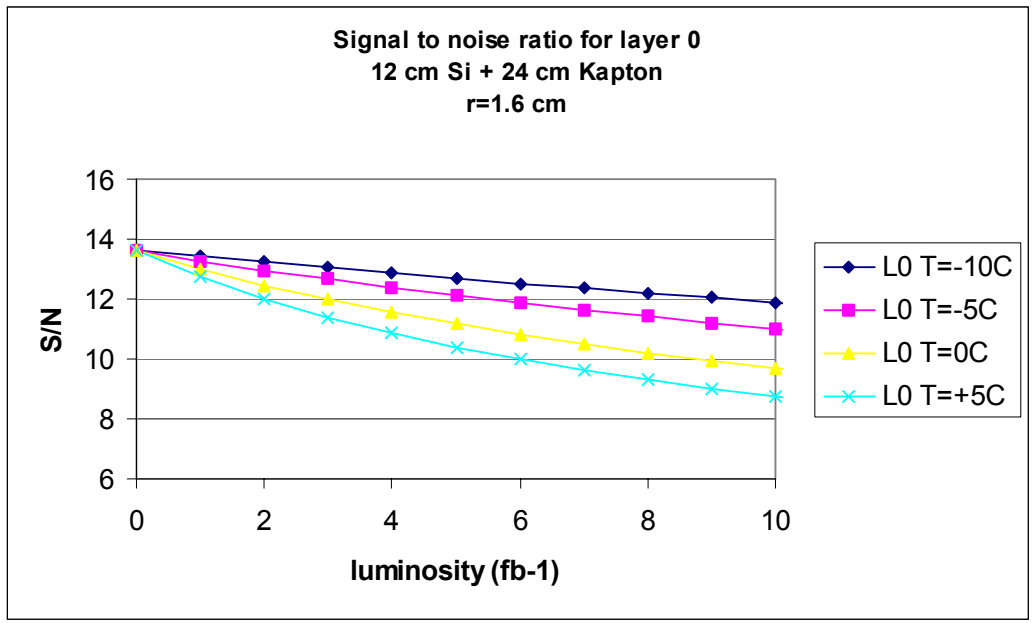
Nov 10 – Mini review

Nov 19 – Submission of revised baseline to DOE

Layer 0 Sensors

- Limited fluence – relaxed requirements on depletion voltage
- operating temperature<-5
- Should be able to design for Vmax of ~300V – can use existing infrastructure, smaller gaps between sensors
- Use Hammamatsu sensors similar to Run2b L0,1 design
- Prototypes probed and irradiated
- Passed Production readiness reviews





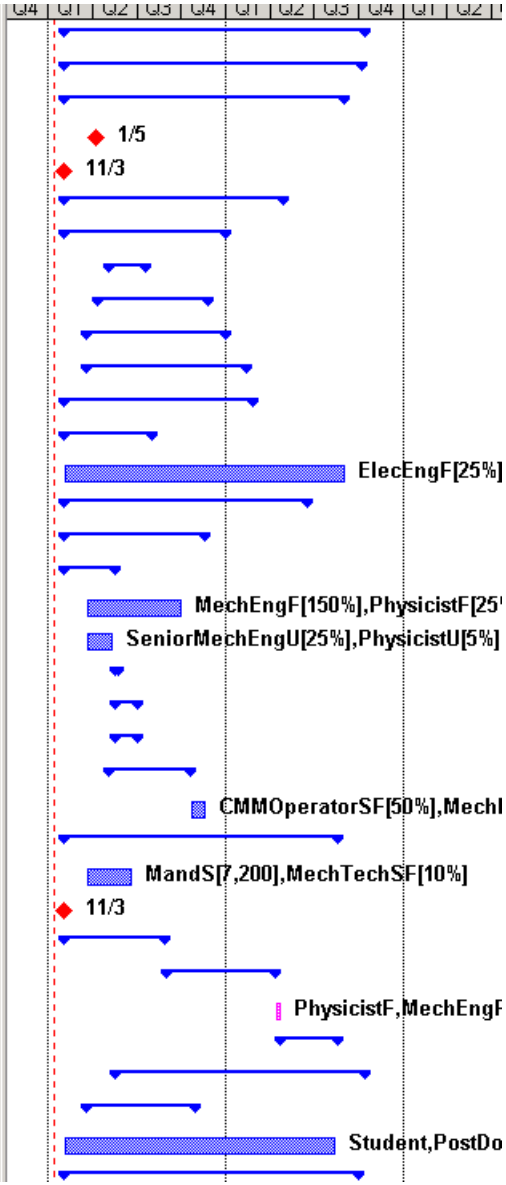
Ronald Lipton

Layer 0 uncertainties

- Will it fit
  - Yes … but there is not much margin.
  - How much margin do we allow?
    - Go from 8 to 6 z segments to reduce cable stack
    - Go to single ply analog cables to reduce stack
- How much coverage?
  - 90-95% in phi depending on detector spacing tolerances
- Conservative grounding scheme
  - Leave space between beam pipe and detector
  - Electrically isolate detector
  - Break N/S conductivity?
  - Isolate at adapter card

Schedule – Based on 2b schedule

1	Layer 0 Silicon Detector	84 w	Mon 11/3/03	Fri 7/15/05	
1.1	Sensors	83 w	Mon 11/3/03	Fri 7/8/05	
1.2	Readout Electronics	78 w	Mon 11/3/03	Thu 6/2/05	
1.2.1	SVX4 Chips Available	0 w	Mon 1/5/04	Mon 1/5/04	
1.2.2	SASEQ Test Stands Available	0 w	Mon 11/3/03	Mon 11/3/03	
1.2.3	Hybrids	60 w	Mon 11/3/03	Wed 1/26/05	
1.2.4	Analog Cables	45 w	Mon 11/3/03	Wed 9/29/04	
1.2.5	Flex Grounding Circuits	11 w	Mon 2/2/04	Fri 4/16/04	
1.2.6	Digital Cables	32 w	Fri 1/9/04	Tue 8/24/04	
1.2.7	Twisted-Pair Cables	39 w	Wed 12/17/03	Wed 9/29/04	
1.2.8	Junction Cards	45 w	Wed 12/17/03	Wed 11/10/04	
1.2.9	Adapter Cards	53 w	Mon 11/3/03	Wed 11/24/04	
1.2.10	High-Voltage System	24 w	Mon 11/3/03	Fri 4/30/04	
1.2.11	Readout Chain Integration	78 w	Mon 11/3/03	Thu 6/2/05	
1.2.12	Full Chain Tests	67 w	Mon 11/3/03	Wed 3/16/05	
1.3	Mechanical Design and Fabrication	39 w	Mon 11/3/03	Tue 8/17/04	
1.3.1	Support Structures Design	13 w	Mon 11/3/03	Fri 2/13/04	
1.3.2	Development and integration of design (FNAL)	26 w	Wed 12/17/03	Mon 6/28/04	11
1.3.3	Produce preproduction samples for testing	6 w	Wed 12/17/03	Fri 2/6/04	11
1.3.4	Production Readiness Review	1 w	Mon 2/16/04	Fri 2/20/04	
1.3.5	Final Fabrication Tooling	7 w	Mon 2/16/04	Fri 4/2/04	
1.3.6	Final Quality Assurance Tooling	7 w	Mon 2/16/04	Fri 4/2/04	
1.3.7	Final Support Structures Production	24 w	Mon 2/2/04	Tue 7/20/04	
1.3.8	Perform final article QA checks of support struc	4 w	Wed 7/21/04	Tue 8/17/04	13
1.4	Layer 0 Detector Modules	76 w	Mon 11/3/03	Wed 5/18/05	
1.4.1	Fabricate module boxes	12 w	Wed 12/17/03	Fri 3/19/04	11
1.4.2	Module Burn-in Stands Available	0 w	Mon 11/3/03	Mon 11/3/03	
1.4.3	Production Module Fixtures	28 w	Mon 11/3/03	Fri 5/28/04	
1.4.4	Preproduction Modules	30 w	Tue 6/1/04	Tue 1/11/05	
1.4.5	Conduct L0 module production readiness reviev	1 w	Wed 1/12/05	Wed 1/19/05	15
1.4.6	Module Production	17 w	Thu 1/20/05	Wed 5/18/05	
1.5	Final Detector Integration and Assembly	71 w	Mon 2/16/04	Fri 7/15/05	
1.6	Monitoring	30 w	Wed 12/17/03	Tue 7/27/04	
1.7	Software and Simulation	75 w	Mon 11/3/03	Wed 5/11/05	
1.8	Silicon Project Administration	82.2 w	Mon 11/3/03	Fri 7/1/05	



Ronald Lipton

Costs and Schedule

- Cost estimate – based on resource loaded schedule derived from Run2b project
- Assume 100% spares – small quantities
- Assume 50-100% contingency due to early phase – not yet in
- Expect ~ $600k available from NSF MRI grant
- ~1.5 year design/construction – Finish 7/17/2005

	FY 03 $ no G&A	M&S non-labor	M&S Labor	M&S Cost	FNAL Labor	l Cost (incl labor)
1	Layer 0 Silicon Detector	$630,695	$208,379	$839,074	$535,847	$1,374,921
1.1	Sensors	$163,000	$1,200	$164,200	$14,940	$179,140
1.2	Readout Electronics	$303,108	$117,840	$420,948	$198,629	$619,577
1.3	Mechanical Design and Fab	$49,686	$89,339	$139,025	$134,192	$273,217
1.4	Layer 0 Detector Modules	$16,711	$0	$16,711	$74,076	$90,787
1.5	Final Detector Integration	$25,700	$0	$25,700	$60,202	$85,902
1.6	Monitoring	$12,000	$0	$12,000	$0	$12,000
1.7	Software and Simulation	$0	$0	$0	$42,300	$42,300
1.8	Silicon Project Administrati	$60,490	$0	$60,490	$11,508	$71,998

Layer 0 conclusions

This is an opportunity for the experiment and collaborators to utilize work done for 2b. Most 2b participants have indicated interest and some commitment, many at a reduced level. There is commitment commensurate with the smaller scale of the project.

Nonetheless layer 0 will materially improve the performance of D0, may be crucial in recovering tracking as the 2a detector degrades.

We know how to do this, and have the resources and manpower – it is, as much as anything, a demonstration of the continued vitality of the experiment.