

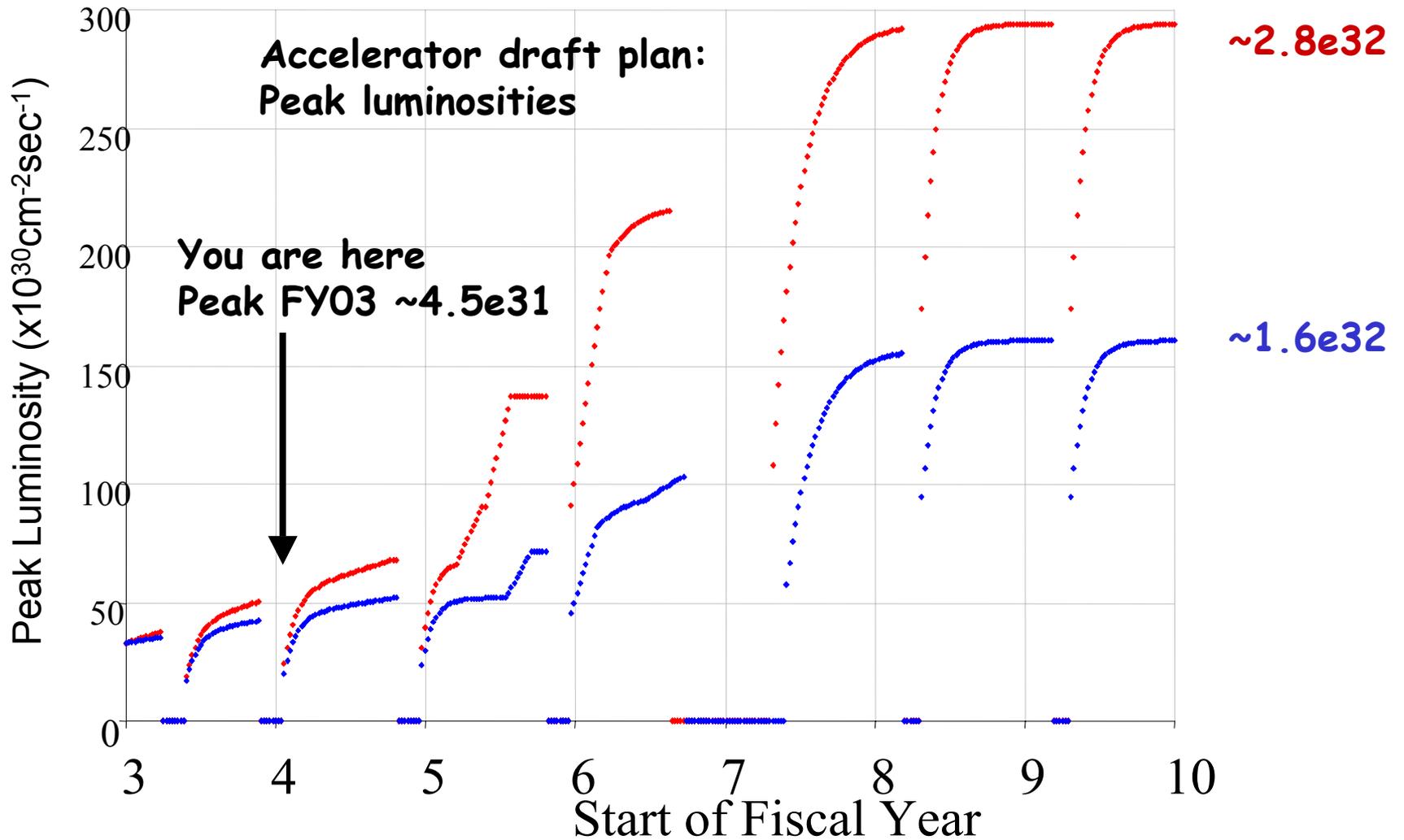


# DØ RunIIb Trigger Upgrade: Technical Progress

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for the DØ Trigger Upgrade Group



# Run IIb Luminosity Projections



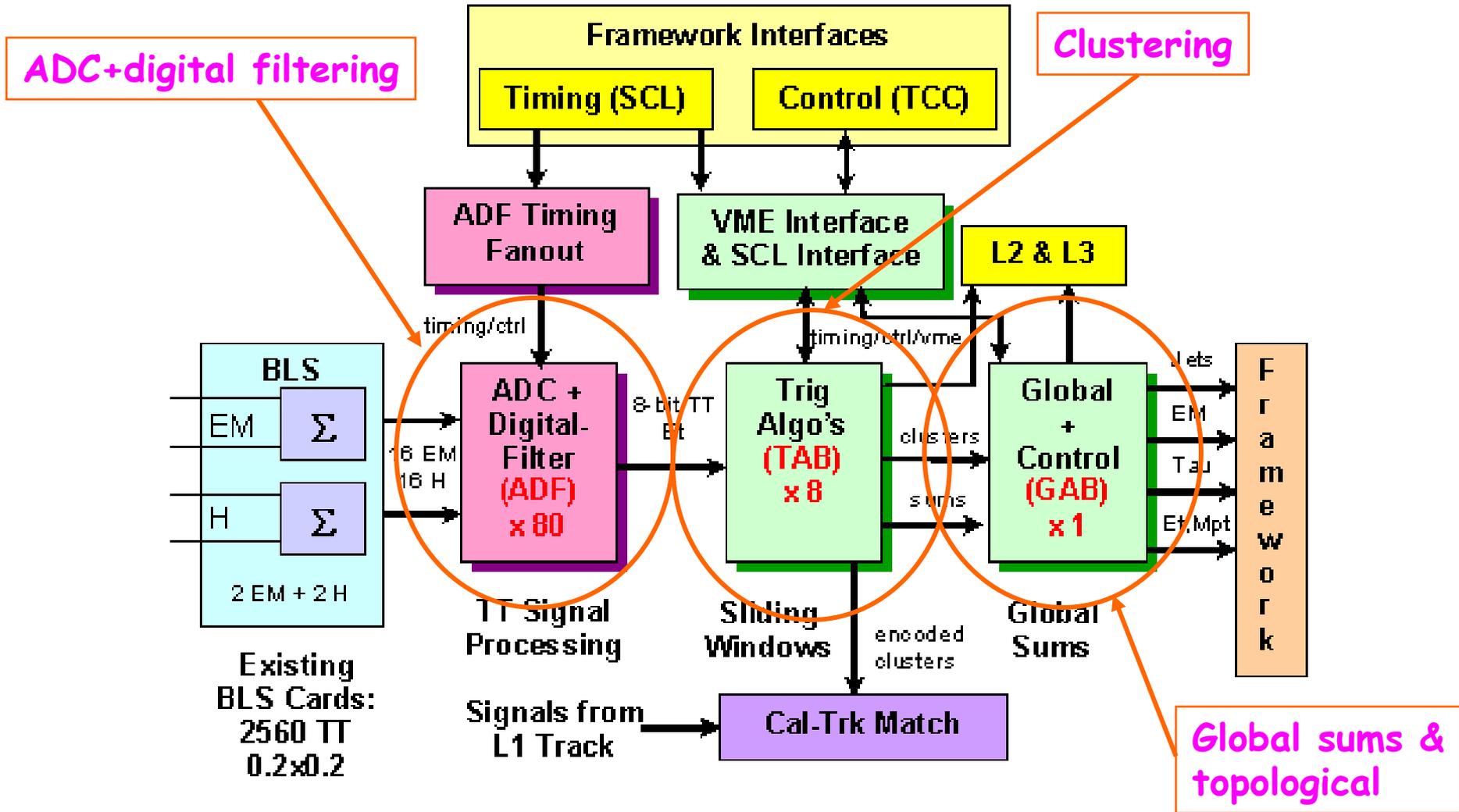


# Ingredients of the Trigger Upgrade

- Level 1
  - ◆ Calorimeter trigger upgrade
    - ▲ sharpens turn-on trigger thresholds
    - ▲ more topological cuts
  - ◆ Calorimeter track-match
    - ▲ fake EM rejection
    - ▲ tau trigger
  - ◆ L1 tracking trigger upgrade (CTT)
    - ▲ improved tracking rejection especially at higher occupancies
    - ▲ inputs to Calorimeter track-match
- Level 2
  - ◆ L2 Processor upgrades for more complex algorithms
  - ◆ Silicon Track Trigger expansion
    - ▲ More processing power
    - ▲ use trigger inputs from new silicon layer 0
- Upgrade/maintain DAQ/Online systems



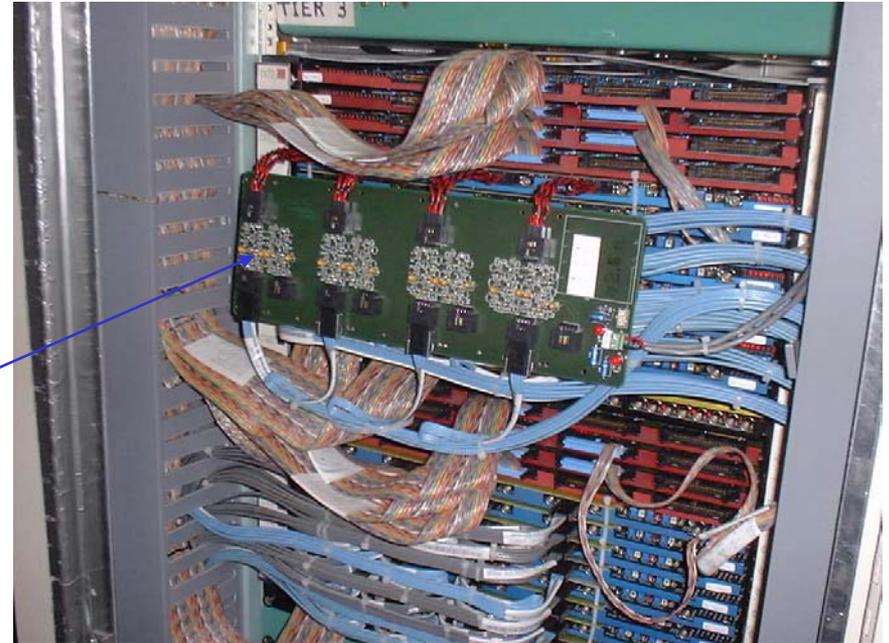
# Technical progress: L1Cal





# Signal Splitter

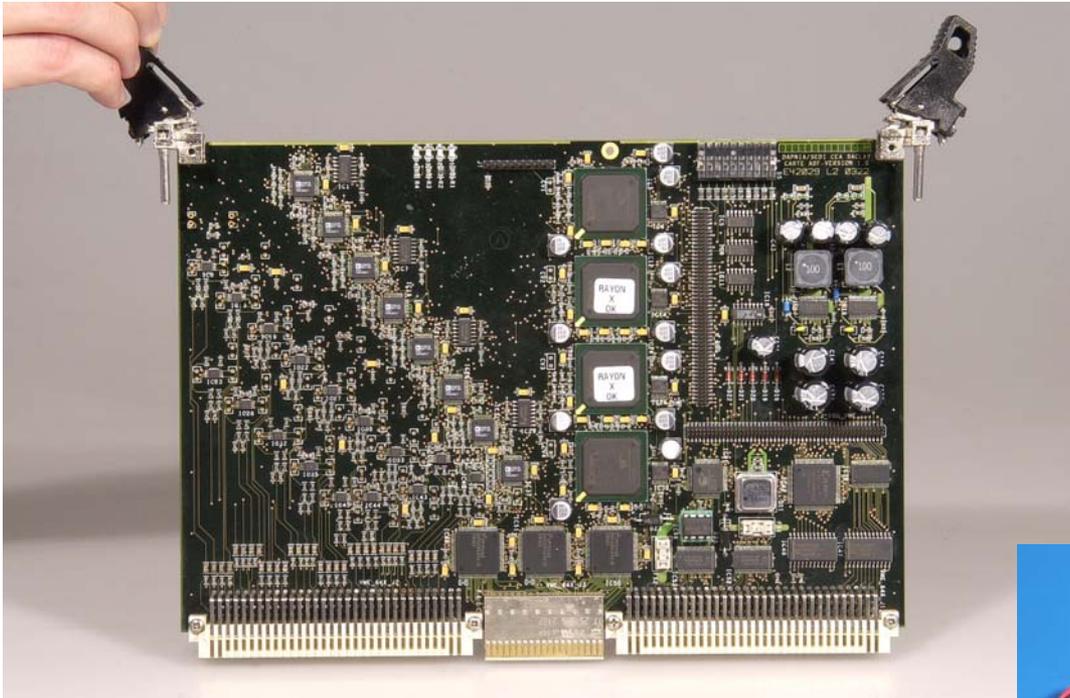
- Access to Real TT Data using "Splitter" Boards
  - ◆ designed/built by Saclay
  - ◆ active split of analog signals at CTFE input
  - ◆ 4 TTs per board
  - ◆ installed: Jan. 2003



- Splitter Data
  - ◆ no perturbation of Run IIa L1Cal signals
  - ◆ allows tests of digital filter algorithm with real data



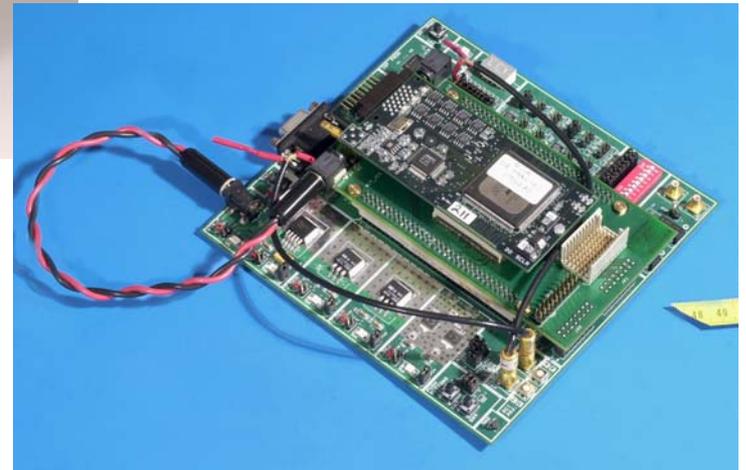
# ADF Prototype



ADF Prototype board

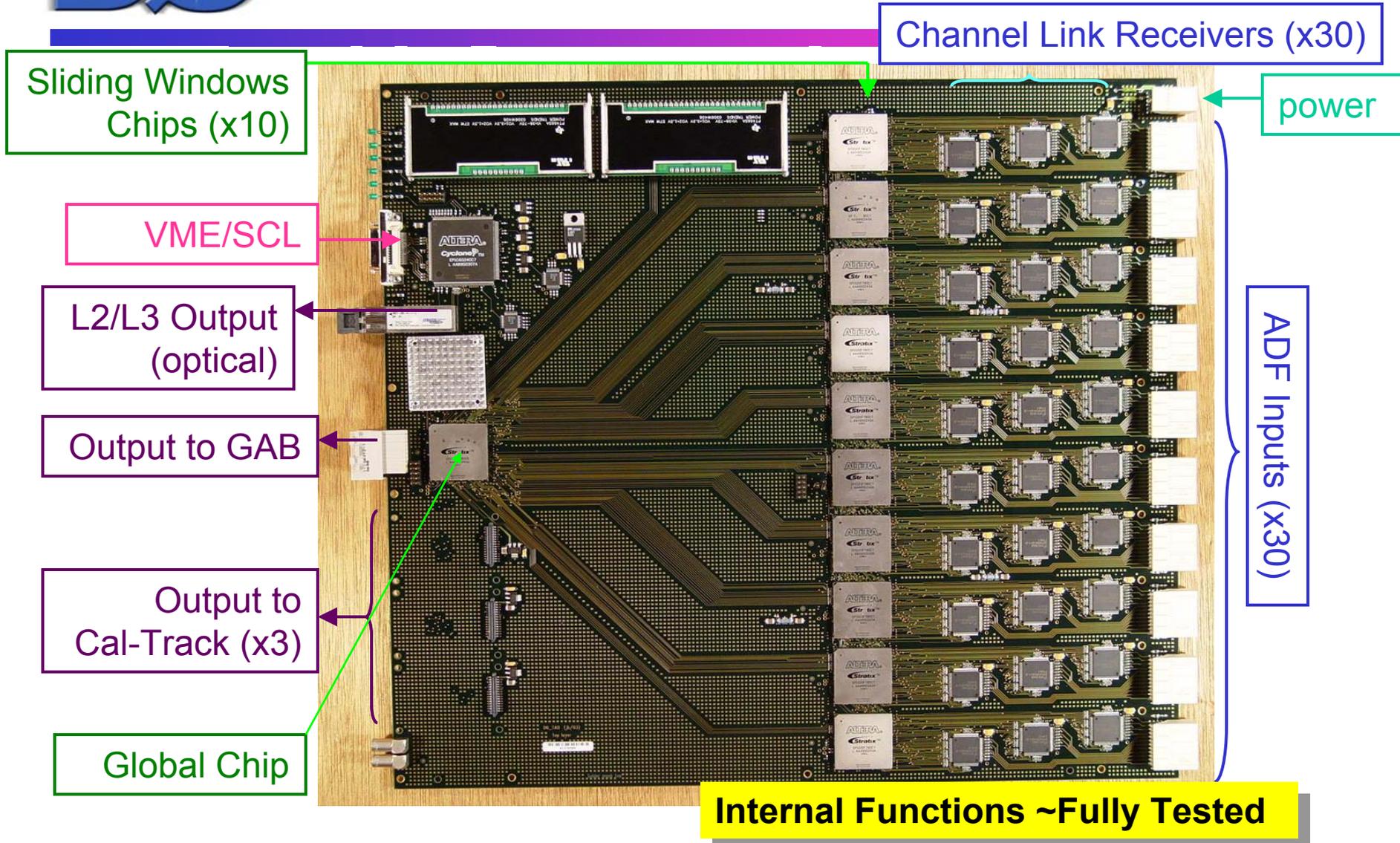
Now at Fermilab  
undergoing integration  
tests

Prototype ADF  
Timing Card





# TAB Prototype





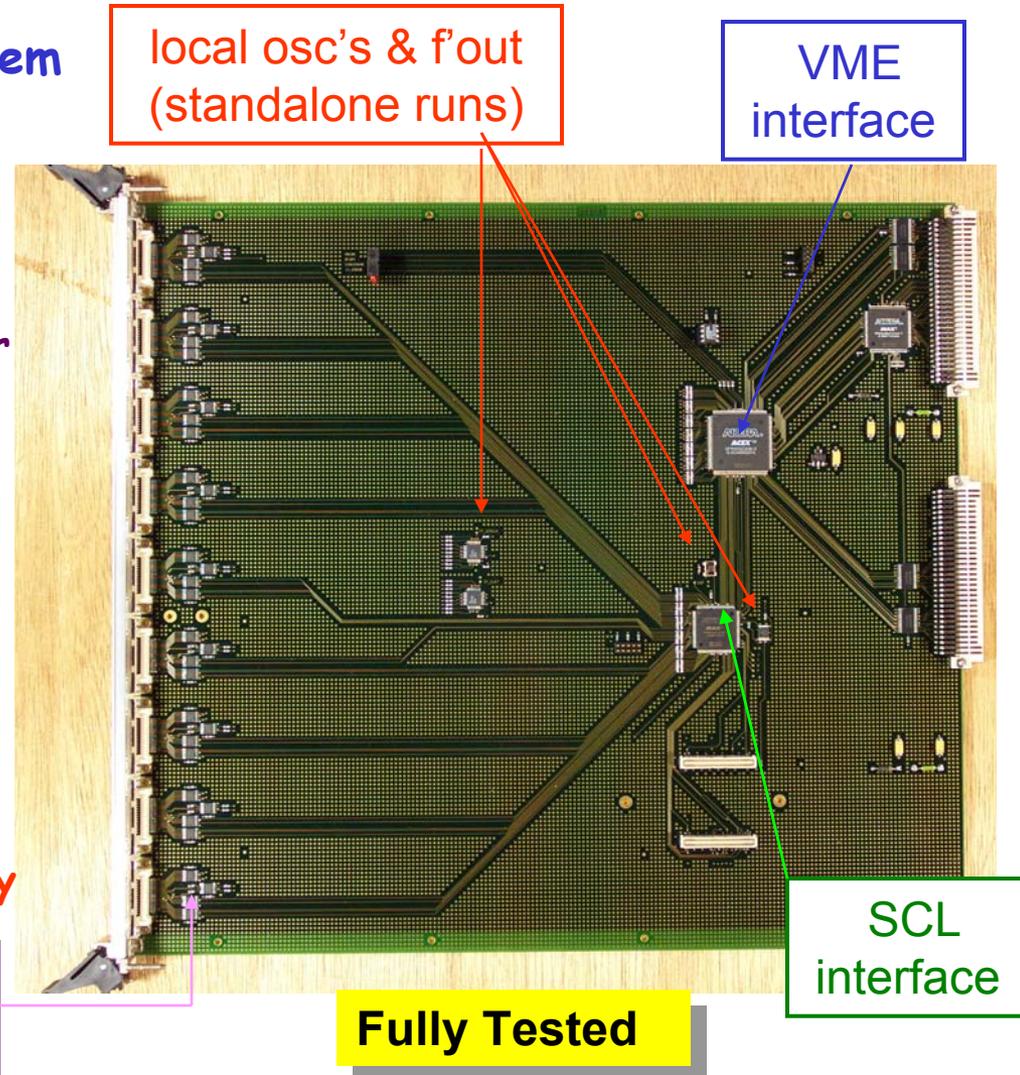
# ADF future plans

- Note that the Saclay group will not be able to participate in DØ beyond the prototyping phase
  - ◆ Thanks to Saclay to bringing the ADF this far
  - ◆ Thanks to MSU for agreeing to take over the ADF
- Next layout of the ADF will be done jointly by Saclay and MSU engineers. Once working, MSU takes ownership



# VME/SCL Board

- **New Comp. of TAB/GAB system**
  - ◆ proposed: Feb 03
  - ◆ change control: Mar 03
- **Interfaces to**
  - ◆ VME (custom protocol)
    - ▲ not enough space on TAB for standard VME
  - ◆ DØ Trigger Timing (SCL)
  - ◆ (previously part of GAB)
- **Why Split off from GAB**
  - ◆ simplifies system design & maintenance
  - ◆ allows speedy testing of prototype TAB
- **Prototype at Nevis: May 12**
  - ◆ main VME & SCL functionality tested & working





# TAB/GAB Test Card

## TAB/GAB Data Rates

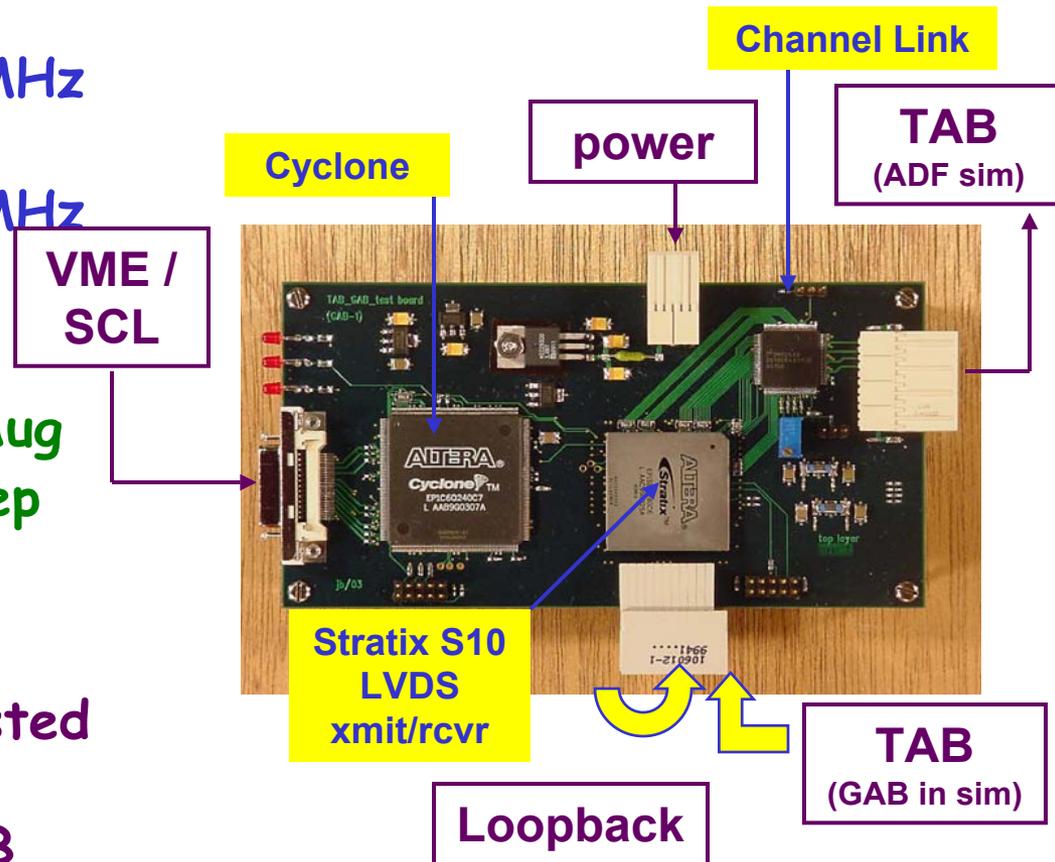
- ◆ TAB: LVDS 424 MHz
  - ▲ (channel link)
- ◆ GAB: LVDS 636 MHz
  - ▲ (stratix)

## Test Card at Nevis

- ◆ Start Design mid-Aug
- ◆ Board at Nevis 29-Sep
- ◆ Cost ~\$2K

## • Status

- ◆ ADF-to-TAB xmit tested before integration
- ◆ Will test TAB-to-GAB before sending out GAB for fabrication





# Prototype Integration Tests

- First test of SCL → TAB done in July
- Tests with ADF + TAB prototypes started last week
  - ◆ SCL → VME/SCL → TAB, ADF
  - ◆ BLS Data (split) → ADF → TAB
  - ◆ Flexible, staged schedule allows components to be included as they become available
- Set up semi-permanent Test Area (thanks to J. Anderson's group at FNAL)
  - ◆ outside of Movable Counting House
  - ◆ connection to SCL, split data signals
  - ◆ allows L1Cal tests without disturbing Run IIa data taking

Successful integration tests last week between

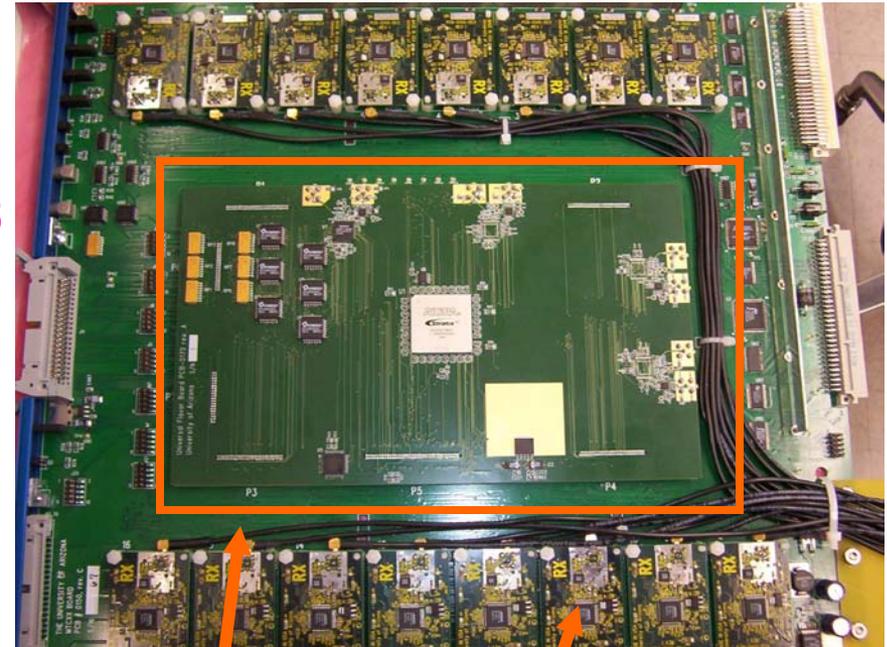
ADF → TAB

TAB → L1mu (L1cal-track surrogate)



# L1 cal-track: Hardware Progress

- **MTCxx (Trigger Cards)**
  - Preproduction design complete
  - Layout and final checks in progress
  - Goal is to submit in November 03
- **UFB (Flavor Board)**
  - Prototypes in hand
  - Boundary scan and downloading OK
  - Receiver/transmitter testing in progress
  - L1MU "05" algorithm implemented in Stratix EP1S20F780C7
    - (simulated but not tested)
  - $H \rightarrow \tau$  algorithm implementation in progress
- **MTCM (Crate Manger)**
  - Not started, but only minimal changes to the existing design



MTCxx (mother)  
Run IIa version

Universal Flavor board (daughter)  
Run IIb prototype



# L1CalTrack Status

- **Infrastructure**

- ◆ VME crates, processors, power supplies, cables in hand
- ◆ L1CTT to L1CalTrack cables installed last weekend (not terminated)
- ◆ Rack space in movable counting house identified

- **Commissioning**

- ◆ Plan is to use spare L1MU cards in L1CalTrack crates to establish communication with Trigger Framework and L3
- ◆ Replace spares with L1CalTrack cards as available

- **Simulator**

- ◆ Work has started writing the L1CalTrack package and integrating it into the DØ Trigger Simulator

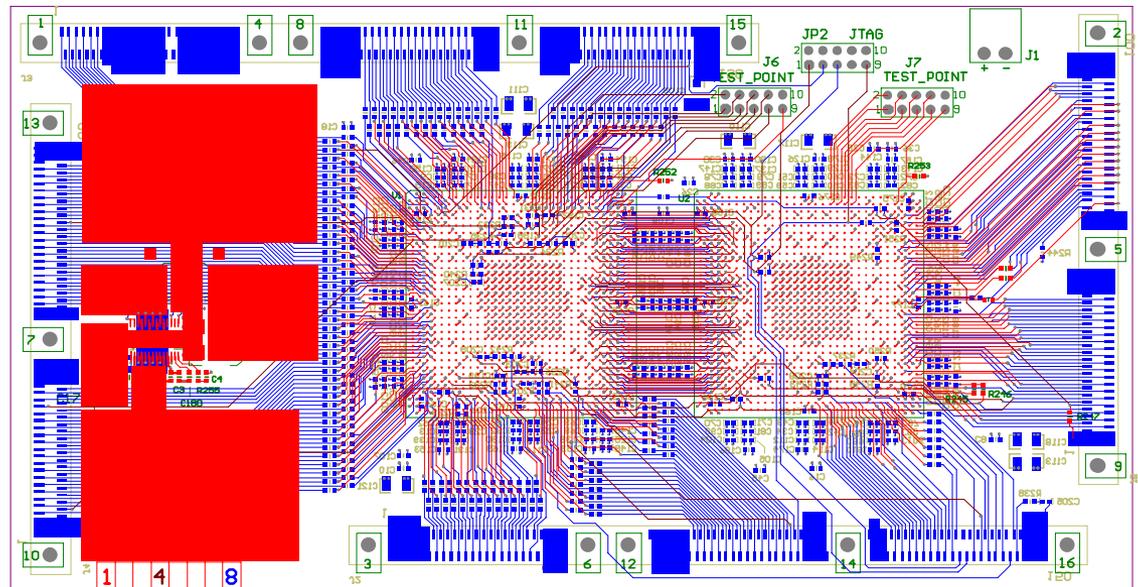


# L1 CTT Implementation

- Digital Front End Axial (DFEA) daughter cards get replaced with new layout with larger FPGA's (Xilinx Virtex-II XC2V6000)
  - ◆ Only 80 daughter cards get replaced;
  - ◆ rest of Run IIa system remains intact
- Implemented prototype firmware (Boston U)
  - ◆ Includes equation files from all 4 momentum bins
    - ▲  $p_T > 10 \text{ GeV}$ ,  $5 < p_T < 10 \text{ GeV}$ ,  $3 < p_T < 5 \text{ GeV}$ ,  $1.5 < p_T < 3 \text{ GeV}$
  - ◆ DFEA logic is implemented in two FPGAs

## Prototype DFEA:

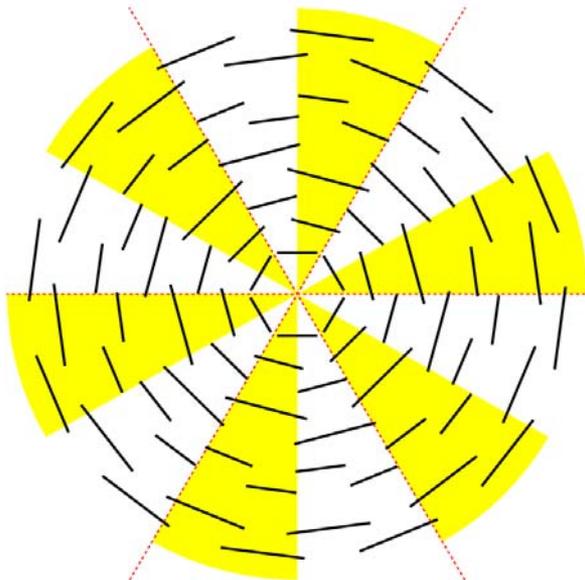
- 10/17/03 prototype PCB returned
- 10/31/03 first prototype assembled.
- 11/30/03 prototype fully tested





# Silicon Track Trigger for Run IIb

- STT upgrade needed to
  - ◆ accommodate new LO?
    - ▲ New LO fits within baseline Run IIb upgrade
    - ▲ even without LO, increase processing power for higher occupancy
  - ◆ Modest STT upgrade requires small quantity of same boards that are used in Run IIa.



## Technical Progress:

- VME Transition Modules procured
  - ◆ Concern about obsolescence
- Other procurements awaiting Layer 0 decision



# Trigger Workshop

- A Trigger Upgrade Workshop was held last Sat/Sun (11-12 Oct)
- Topics:
  - ◆ technical progress and schedule
  - ◆ Current and future Run II trigger lists
  - ◆ installation/commissioning strategies
- Summary
  - ◆ Very useful workshop with many details sorted out
  - ◆ Interesting conclusion: It looks like all parts of the trigger upgrade can be in place ~Sum/Fall '05



# Installation/Commissioning Strategies

- Plan to install/commission during planned accelerator shutdowns as much as possible
  - ◆ want to install as early as possible to get the most benefit
  - ◆ want to install during machine shutdowns
- 2 phases of commissioning
  - ◆ technical commissioning
    - ▲ testing inputs/outputs and integration
    - ▲ no beam necessary
  - ◆ physics commissioning
    - ▲ need beam for this
    - ▲ trigger verification/calibration
- can deliver a useful trigger even before it is fully calibrated



# Installation/Commissioning Plans

- L1 Cal trigger: Summer '05
  - ◆ L1 Cal trigger pretested on sidewalk
  - ◆ we can then install + technically commission L1 cal in 10 weeks (6 + 4)
  - ◆ useful L1 Cal trigger ~ 2 weeks after resumption of Tevatron
    - ▲ use 2 weeks with beam to verify trigger
  - ◆ fully calibrated will take longer, depending on reliability/luminosity of TeV (~1 month)
- L1cal-track
  - ◆ System commissioned with L1mu modules, then replaced with real L1cal-track modules
  - ◆ Ready in advance for L1cal inputs
- L2 STT
  - ▲ installed/technically commissioned during Layer 0 installation
- adiabatic installation of CTT (starting early '05)
  - ◆ replace modules while still running in run2a mode
- L3 $\beta$  can be upgraded earlier - whenever necessary



# Summary

- Trigger upgrade proceeding a full speed
- Prototypes in hand:
  - ◆ L1cal: splitter, TAB, VME/SCL, ADF
  - ◆ Cal-track: UFB
- Prototype in fabrication
  - ◆ L1CTT: DFEA preproduction I
- Major milestones achieved in integration tests
  - ◆ Run off of DØ timing signals
  - ◆ Data sent between ADF and TAB
  - ◆ Data sent between TAB and cal-track surrogate (L1mu) - generated triggers in DØ just as it was supposed to
- Plan to install in '05 with minimal downtime