



Agenda

Fermilab PMG

Draft DZero Run IIb Upgrade Baseline Change Proposal October 15, 2003

- Introductory remarks (Womersley - 5')
- BCP overview (Kotcher - 10')
- Trigger technical status (Wood - 15')
- Rebaselined project, BCP details (O'Dell - 30')

**Everything you will see today is in
DRAFT FORM**



Run IIb Project Organization

Oct '03

Silicon sub-project under reconsideration to accommodate Layer 0

DO Run IIb Project
 J. Kotcher, Project Manager
 V. O'Dell, Deputy (Trigger/DAQ); R. Lipton, Deputy (Silicon Layer 0)
 W. Freeman, Associate, M. Johnson, Technical Coordinator
 D. Knapp, Budget Officer; T. Erickson, Administration

WBS 1.1
 Silicon
 M. Demarteau
 G. Ginther

WBS 1.2
 Trigger
 P. Padley
 D. Wood

WBS 1.3
 DAQ/Online
 S. Fuess
 P. Slattery

WBS 1.4
 Project
 Administration

WBS 1.5
 Installation
 R. Smith

1.1.1 Sensors
 R. Demina, F. Lehner

1.1.2 Readout System
 A. Nomerotski, E. von Toerne

1.1.3, 1.1.5 Mechanics & Assembly
 W. Cooper, K. Krempetz

1.1.4 Production
 J. Fast

1.1.4 QA, Testing, & Burn-in
 C. Gerber

1.1.6 Monitoring
 M. Corcoran, S. de Jong

1.1.7 Software & Simulation
 D. Buchholz, E. Shabalina

1.1.8 Administration
 (M. Demarteau)

1.2.1 L1 Cal Upgrade
 M. Abolins, H. Evans,
 P. LeDu

1.2.2 L1 Cal/Track Match
 K. Johns

1.2.3 L1 Track Trigger
 M. Narain

1.2.4 L2β Upgrade
 R. Hirosky

1.2.5 Silicon Track Trigger
 U. Heintz

1.2.6 Simulation
 M. Hildreth, E. Perez

1.2.7 Administration
 (D. Wood)

1.3.1 Level 3 Systems
 D. Chapin, G. Watts

1.3.2 Network & Host
 Systems
 J. Fitzmaurice,
 S. Krzywdzinski

1.3.3 Control Systems
 F. Bartlett, G. Savage,
 V. Sirotenko

1.3.4 DAQ/Online
 Management
 (P. Slattery)

1.5.1 Silicon Installation
 Mechanical:
 H. Lubatti
 Electronics:
 L. Bagby, R. Sidwell

1.5.2 Trigger Installation
 D. Edmunds

Adjustments continue
 to be made...



DZero Run IIb Rebaselining

- We will present today our current (draft) estimates for:
 - ◆ Project costs to date
 - ◆ Silicon closeout costs
 - ◆ Updated costs for previously approved sub-projects
 - ◆ Cost estimates, status for new projects being put forward
 - ◆ Discussed as much as possible in terms of in kind, TEC, TPC, other relevant categories



DZero Run IIb Rebaselining

- All previously-approved trigger & DAQ/online sub-projects continue on as before
 - ◆ Technical progress excellent, commitment strong as ever, work continues unabated
 - ◆ Includes Silicon Track Trigger, which is needed to accommodate layer 0
 - ◆ Cost of trigger project has increased, largely due to labor needs:
 - ▲ SACLAY dropped out (L1 Cal ADF), effort was all in kind - picked up by MSU
 - ▲ Operations budget slashed, key support totally project-based at the moment (Edmunds, Laurens)
- Layer 0 proposal quite robust, assembled in record time by dedicated, very talented team
 - ◆ Technical design presented in detail yesterday, 137 pg CDR drafted
 - ◆ Critical mass is there - both Fermilab personnel and collaborating institutions (including silicon MRI institutions)
 - ◆ Total sub-project cost, including contingency, labor, escalation, & burdening, will be presented later today



DZero Run IIb Rebaselining

- We are putting forward an upgrade to the Fiber Tracker readout & triggering system
 - ◆ Maintain tracking capability in light of cancellation of silicon upgrade, especially at increased luminosity
 - ▲ considerably improved noise performance - lower thresholds, enhance triggering, efficiency
 - ▲ z-information from timing
 - ◆ New Analog Front-End Boards (AFE II) and trigger (TriP) chip
 - ▲ First version TriP chip submitted with SVX4
 - ▲ Designed, tested by Fermilab (PPD, Yarema)
 - ▲ Was major success out of the box
 - ▲ First full AFE II prototype being laid out now, expect back by year's end
 - ▲ System represents major simplification, likely performance upgrade



DZero Run IIb Rebaselining

- We feel it important to include the AFE II/TriP sub-project in the rebaselined plan - to board the train before it leaves the station
- Approximately 4-6 months work remain before project can be fully evaluated:
 - ◆ Full AFE II prototyping (in progress)
 - ◆ Additional TriP submission that includes timing capability (z-information)
 - ▲ Piggy-back off upcoming submissions, reduce setup charges
 - ◆ Conclude physics simulations on physics gains of integrating z-information in analyses (in progress)
- Propose that the cost of this sub-project be earmarked as a line item in the contingency of the rebaselined request. Timeline:
 - ◆ Internal DZero review of sub-project on Feb time scale
 - ◆ Provided we wish to go ahead, present to April PAC
 - ◆ Depending on outcome or if, after further study, we believe gains are not justified, funds are returned
 - ◆ Current estimate: ~ \$1M (see attached slides)



Note on Installation

- All major sub-projects, absent previous Run IIb silicon installation constraint, are converging on same time scale:
 - ◆ Ready for summer '05 shutdown
 - ◆ Duration ~ 6 weeks (including Layer 0)
 - ◆ Minimal interruption to complex, acquisition of useful luminosity

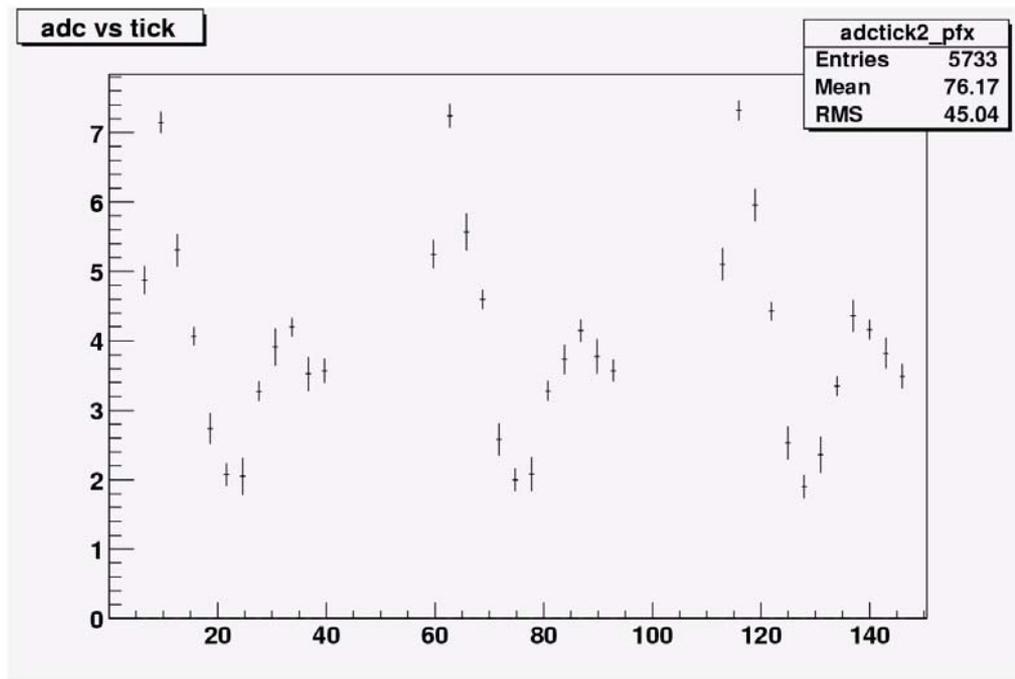


- **BACKUP SLIDES ON AFE II/Trip UPGRADE FOLLOW**



AFE II/Trip Upgrade

- Motivation to replace current analog front-end boards (AFE) for the CFT
 - ◆ Improvements in pedestal width and stability, uniformity
 - ▲ Tick-to-tick variations, and variations within a tick
 - ◆ Reduce data size
 - ▲ Eliminates currently-read-out unused SVX channels
 - ◆ Added capability: z-information from timing
- Pedestal variations produces effective cut in light yield
 - ◆ May be as much a 2 pe effect



ADC v. Tick
variation



AFE II/TriP Upgrade

- **AFE II:**

- ◆ **New set of boards**
- ◆ **Greatly simplified wrt current version: no SIFT, no SVX**
 - ▲ **TriP (or TriP \dagger)**
 - TriP chip submission very successful - meets spec.
 - Designed, tested by Fermilab (PPD, Yarema)
 - ▲ **Commercial Flash ADC**
 - ▲ **Otherwise integrates completely with existing system**
- ◆ **Prototype tests look very good**
- ◆ **Full board prototype schedule for fall, but has been delayed by shutdown**
- ◆ **Expect:**
 - ▲ **Improved reliability**
 - ▲ **Improved Ped dispersion and stability**
 - ▲ **Added Functionality with new submission of TriP Chip - TriP \dagger**
 - **z information from timing (2 ns resolution)**
 - Speeds track reco (Tests by G. Borissov indicated almost factor of 2)
 - May improve CFT hit clustering



AFE II

- **Cost M&S:**

- ◆ Production cost M&S are based on quotes for parts and labor - contingency estimate is grounds up:

Cost Element	Qty Reqd	Unit cost	Net cost
Bare AFE Boards	250	\$400	\$100,000
Parts Costs	250	\$800	\$200,000
Assembly Charges	250	\$600	\$150,000
packaging TRIP chips	5,000	\$5	\$25,000
Flash ADCs	5,000	\$8	\$40,000
Xilinx Spartan II	2,500	\$20	\$50,000
P/S parts (regulators)	2,500	\$20	\$50,000
CPLD cost adjustment	4,000	-\$10	-\$40,000
fifo cost adjustment	2,000	-\$10	-\$20,000
analog support adjustment	4,000	-\$10	-\$40,000
Develop TRIP test fixture	3	\$6,000	\$18,000
New Vicor Modules	17	\$300	\$5,100
BASE COST ESTIMATE			\$538,100
Contingency			\$107,620
NET COST ESTIMATE			\$645,720

Note: Parts costs come from AFE I calculation. AFE II does not use some parts, thus the cost adjustments (negative \$)

- ◆ This does not include our cost of a second submission of Trip chip (shared submission is assumed \approx \$100k)



AFE II

- **Cost Manpower**

- ◆ Manpower estimates are based on experience with AFE I and the assumption that the boards will be fully loaded by an outside vendor and tested (DC + basic functionality).
 - ▲ FTE technicians (electrical): 1.0 man-year
 - ▲ FTG engineer (electrical): 0.5 man-year
- ◆ It is assumed that physicists manning shifts will perform high-level testing at DAB test stand and will commission the electronics.

- **Schedule:**

- ◆ Our current estimate is 18-24 months depending on second submission of Trip - time-stamp version (Trip t)