

Responses to Layer 0 Questions and Comments November 4, 2003

- *The design choices (single sided, poly resistors, etc) seem quite reasonable and well grounded in existing experience. S/N estimates are quite low on the edges, and of course will fall as dark current rises, which is generally worrisome, and will eat into the btag efficiency, but appears to be an intrinsic cost associated with this compact design. In addition 23000 signal carriers assumed in the text is probably about 10% high, in part because of capacitive sharing, so even the starting values will probably be lower than what is quoted. One might wonder whether thicker silicon might help address this, but presumably this has already been considered and rejected on the grounds that the depletion voltage requirements are already driving the design?*

Hamamatsu is the preferred vendor for these devices. They have a stock of 320 micron thick silicon which was intended to be used for the Run2b sensors. We understand that they would like to use this material for any layer 0 sensors that are ordered. We are hesitant to make changes to the sensor materials and designs which have passed production readiness reviews beyond what is necessary to fit into the Layer 0 geometry.

Thicker silicon also has the potential disadvantages that it requires slightly more radial space, which is at a premium, and increases the number of radiation lengths. Starting with sensor pitches of 0.071 mm for the A layer and 0.081 mm for the B layer, increasing the silicon thickness from 0.32 mm to 0.50 mm leads to a reduction in A layer pitch from 0.071 mm to 0.0686 mm (not necessarily bad, in itself) and a reduction in azimuthal acceptance from 98.4% to 96.5%.

- *Breakdown voltage. The discussion of depletion voltage and the way it will rise with radiation dose suggests that an operating voltage in excess of ~300 volts will not be needed. However the projected sensor spec of 800 volts is mentioned in the CDR. Does this over specification put the procurement at risk?*

The 800V value in the CDR is in error. We expect to use the same 700v specification described in the layer0/layer1 production readiness review. These specifications can be found at:

http://www.physik.unizh.ch/~lehnerf/dzero/specs/silicon_spec_layer0_v1.2.pdf

All of these specifications have been discussed with the vendor and have reviewed in the August Layer 0/Layer 1 Production Readiness Review. Based on our prototype testing and interactions with Hamamatsu the 700 V specification should not be a problem. We are willing to relax this specification if this becomes an issue.

- *While all the clearances associated with a silicon detector are small, the methods used for positioning and assembly are matched to the job. Extensive use is made of precision fixturing and CMMs.*

The obvious concern in this instance is the radial clearance which is constrained by the

outer radius of the Beryllium beam pipe and the composite inner radius of the various inner apertures of the current Run Iia detector. Some ideas were thrown out during the discussions; while these particular ideas may have been impractical, the team might still find it profitable to search for further improvements in the installation procedures

Does the Be beam pipe have a longitudinal seam left over from Brush-Wellman construction techniques? With clearance being so difficult, this might have been mentioned somewhere, but it wasn't.

The beryllium beam pipe sections were machined from billets and have no longitudinal seams. Half-lap joints between sections are azimuthal, were made by electron beam brazing, and extend minimally, if at all, above the adjoining surfaces. Joints to stainless steel end flanges are azimuthal and lie within the transverse profiles of the flanges. This technique does not produce a longitudinal seam

- *It was observed that the fitting of the cable packages inside the Iia detector is confronted at the time of the insertion of the Layer 0 detector in the cylindrical carbon fiber sheath... And that this will be done on the assembly bench.*

We still expect to provide a protective sheath, but we are considering using material which is not electrically conductive. The sheath would be applied while L0 is supported from the granite of a coordinate measuring machine, which serves as an assembly bench. Dimensional checks would be repeated at that time.

- *Pre-installation testing. Further in this vein, it has been mentioned several times in previous phone/video meetings that the usefulness of testing the full package before installation, cannot be overemphasized. This would check for damage and for HV problems that could result from packing flex cables in a tiny volume. It is briefly referenced in section 4.4. The point to be made here is that the construction schedule should show adequate time for testing *and* reworking.*

We agree. Our current schedule provides time for testing before and after the sheath is installed. Each module is tested after installation and there is provision for a detector “garage” which will allow overnight burn-in of installed devices. The schedule also has a month of dedicated testing after installation of the sheath.

- *The spacing between elements of detector and readout cables controls capacitances and hence cross-talk and hence noise in the readout. The specification of the spacings depends on experience gained by CDF and D0 in the assembly and (difficult) operation of the Run Iia detectors.*

By now it is well known that there have been noise issues in Run Iia with both CDF and D0 detectors. Are the clearances in the Layer 0 design sufficiently conservative?? Again, the pre-installation testing may well be a most important element.

There has been extensive study of these issues for Run2b in D0. We have a comprehensive grounding plan that includes co-curing a kapton mesh grounding circuit in the carbon fiber support layup. We have studied noise and capacitance as a function of clearance and, in all cases, have specified clearance values well in excess of thresholds of observed effects (figure 1). A recent report on this work is available in the last section of an RD03 conference report:

<http://d0server1.fnal.gov/users/kazu/www/smt2b/d0smt2b.pdf> and in D0 note 4177.

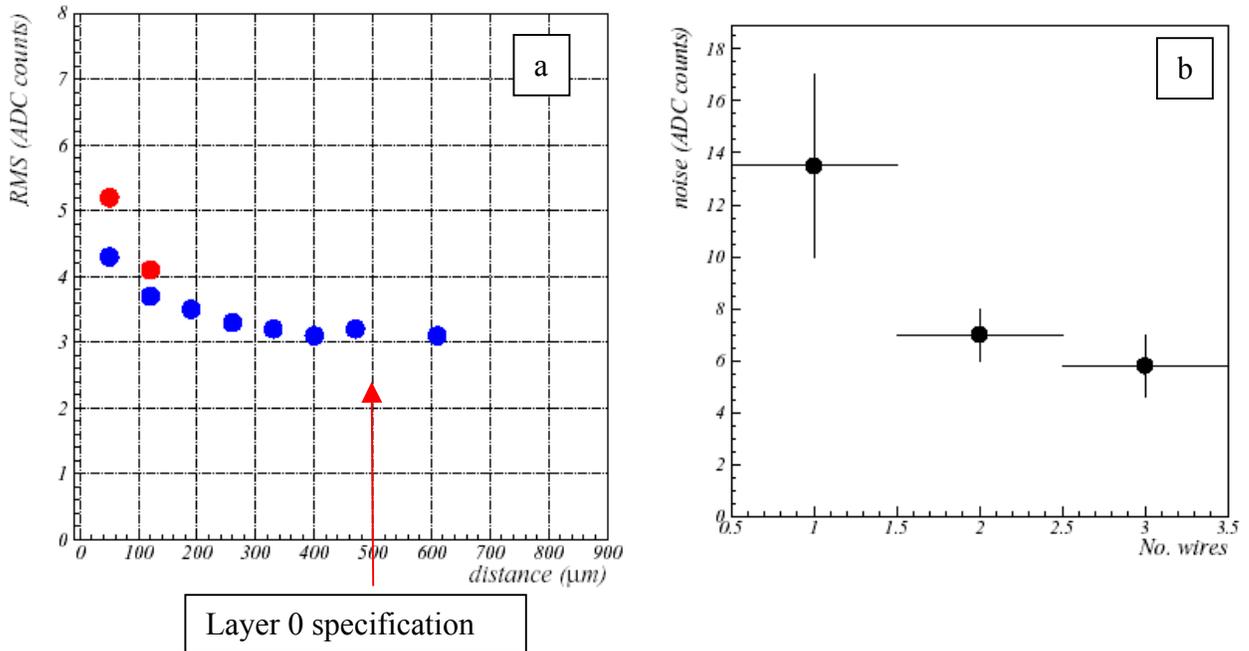


Figure 1. a) Noise measured as a function of analog cable to ground separation. The separation specified for layer 0 is 500 μm . b) Noise as a function of the number of 4'' wires used to ground the layer 0 hybrid demonstrating the effects of wire inductance.

We considered a single point grounding scheme but are concerned that the complex nature of the system and small distances will make parasitic AC grounds and associated ground loops impossible to avoid. Instead we make low inductance connections from the cocured carbon fiber/kapton to both the sensor and hybrid grounds. This provides a solid reference ground for both the sensors and SVX4 chips.

We have also been concerned with noise pickup from the beam pipe and possible ground loops between the North and South readout electronics. To reduce pickup carbon fiber components are spaced as far as practical from the beam pipe. This leads to a polygonal, rather than circular, cross section for the inner pipe. This design provides an average separation of 0.95mm, corresponding to a $\sim 10 \Omega$ resistance, which we believe is adequate. Ground loops will be avoided by providing ground isolation in the redesigned adapter cards.

- *There is no space in the readout for the Layer 0 detector to be completely add-on. That means that the introduction of the adaptor cards to allow use of the SVX4 readout chips is in fact a replacement. We believe that there will just need to be 24 cards to be replaced or modified. Is that correct?*

Each adapter card handles two channels – so only 24 cards will need to be replaced. We have identified cards associated with the H disks on the outer adapter card ring. Changing the outer ring cards will allow the maximum installation space and minimize the impact on the existing cable plant.

- *At the time of presentation the issue of active cooling for the modified adaptor cards seemed to be unclear?*

This continues to need study. We hope to be able to rely on passive cooling but the design has not evolved sufficiently to make a definitive statement.

- *Some or all of the channel count needed for the new detector will be obtained by robbing the existing H-disk system. It appears that the view is taken that the H-disks are less valuable. Does the Layer 0 plan leave all the detector readout except for H-disk elements undisturbed? If not, it would be useful to clarify which elements are modified.*

Only the H disks will be affected by Layer 0. We will need to remove all four H disks for layer 0 installation but should be able to reinstall the inner set of disks. The installation includes the time for reinstallation and recabling of the H disks

As with all silicon projects there is concern about the schedule, both construction and installation. While off-project we would like to know in what state is the installation schedule?

An installation schedule exists which requires seven weeks from start of shutdown to the time D0 is ready for resumption of Tevatron operation. This has been reviewed by the principles and, while it is still subject to change, we believe the overall time scale is correct. The major components of this schedule and associated times are:

- Removal of the existing beam pipe and H disks (2.2 w)
- Survey of the available clearances (0.8 w)
- Installation, survey, and alignment of the layer 0 detector (0.8 w)
- Reinstallation of inner H disks (0.4w)
- Cabling of H disks and layer 0 including installation of adapter and junction cards (1.8 w)

3	1.5.1.1	Silicon Ready To Move To DAB	7/21/05	7/21/05	0 w
4	1.5.1.2	Shutdown for Installation Begins	6/30/05	6/30/05	0 w
16	1.5.1.3.11	Silicon Infrastructure Prepared	5/3/05	5/3/05	0 w
25	1.5.1.4.8	Detector Open and Ready for Access	7/11/05	7/11/05	0 w
31	1.5.1.5.5	Run IIa Beampipe & Silicon H-Disks Removed	7/18/05	7/18/05	0 w
37	1.5.1.6.5	L0 Silicon Detector Installed In RunIIa Silicon	7/29/05	7/29/05	0 w
43	1.5.1.7.5	L0 Silicon Cable-up Complete	8/11/05	8/11/05	0 w
47	1.5.1.8.2	Run IIb Beam Tube Installed	8/18/05	8/18/05	0 w
50	1.5.1.10	Silicon Ready for Resumption of Tevatron Operation	8/18/05	8/18/05	0 w
54	1.5.1.12	Silicon System Ready for Physics Commissioning	9/8/05	9/8/05	0 w

Table 1. Installation schedule.

It is recognised that the time for simulation has been tight and that "old" studies were heavily leveraged. There was some concern that the studies, as described in the presentation, did not address how L0 performed in the presence of a deteriorating Layer 1. That seems to be addressed in the proposal. Nevertheless, we would appreciate receiving any updated writeup of the performance studies you may complete during the next few weeks.

We have no new studies to present at this time. We believe that the most important issues to understand are related to the low efficiency and high noise that CDF has experienced. We would like to use our own data as much as possible to understand these effects over the next few weeks.